ST7580 presentation

Workshop on Powerline Communication

October 28th, 2014
• ST7580 product overview
  • Device Architecture
  • Protocol stack
  • Host Interface

• ST7580 Reference Design Overview

• ST7580 comparison with ST7540

• ST7580 Open discussion
ST7580

Device Architecture
Analog Front End: Reception path

- Modulated Signal received on RX_IN pin
- Gain Adjustment performed by PGA block
- Digital conversion through $\Delta\Sigma$ - ADC
- Digital signal filtered around the two frequencies
- Demodulation by DSP engine
Analog Front End: Transmission path

- FSK/PSK waveforms generated by the DSP
- Band-pass filter around selected frequency
- Gain attenuation: logarithmic scale, 32 steps
- TX_OUT pin for modulated signal transmission
Analog Front End: Power Amplifier (1)

- **Integrated Power Amplifier**
  - 8 to 18V supply
  - 14Vpp max output
  - Up to 1Arms
Analog Front End: Power Amplifier (2)

- Power Amplifier pins externally available to build an active filter
- Gain set through the external network
Analog Front End: Output Voltage

- Output voltage (Vpp): \[ V_{OUT} = V_{DAC} \cdot TX_{GAIN} \cdot PA_{GAIN} \]
  
  (where \( V_{DAC} = 4.8\text{Vpp typ.} \))
A fraction \(\frac{1}{83}\) of output \(I_{PA}\) current is mirrored on CL pin.

Voltage value on CL pin is monitored to be below a fixed threshold.

Output gain is decreased if the threshold is overpassed.
Two external power supply voltages required:
- VCC (8V to 18V) for analog parts, max input current: 500 mA
- VDDIO (3.3V to 5V) for digital sections, input current: 40 mA

Internal regulators generating 5V and 1.8V

Internal regulators externally available for filtering purpose only
Clock Management

- 8MHz clock to be provided by external source:
  - Crystal through XIN and XOUT pins
  - External clock (on XIN pin)

- Load capacitance (32pF) integrated in pins

- Internal clock trees:
  - 28MHz: Microcontroller
  - 56MHz: DSP
ST7580

Protocol Stack
ST7580 Protocol Stack

- PHY and DL layers with framing services
- MIB to store configuration and information objects

Host Interface to manage communication with an external host
## Modulation schemes

<table>
<thead>
<tr>
<th></th>
<th>Baudrate</th>
<th>Mode</th>
<th>Bitrate</th>
<th>Carrier</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PSK</strong></td>
<td>9600 bps</td>
<td>B-PSK</td>
<td>9600 bps</td>
<td>Selectable (CENELEC A, B, D band)</td>
</tr>
<tr>
<td></td>
<td>9600 bps</td>
<td>B-PSK Coded</td>
<td>4800 bps</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>9600 bps</td>
<td>Q-PSK</td>
<td>19200 bps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9600 bps</td>
<td>Q-PSK Coded</td>
<td>9600 bps</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>9600 bps</td>
<td>8-PSK</td>
<td>28800 bps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9600 bps</td>
<td>B-PSK Coded PNA</td>
<td>2400 bps</td>
<td></td>
</tr>
</tbody>
</table>

| **B-FSK** | 1200 bps | B-FSK           | same as baudrate | Selectable (CENELEC A, B, D band) |
| 15         | 2400 bps |                 |                  |                                  |
| 15         | 4800 bps |                 |                  |                                  |
| 15         | 9600 bps |                 |                  |                                  |
Channel selection

- **Transmission**
  - centered around a selectable frequency
  - performed through a selectable mode

- **Reception**
  - Two channels selectable through dedicated registers
  - Single (high) or Dual Channel mode
  - Only modulation type (PSK or FSK) over a single channel

<table>
<thead>
<tr>
<th>Reception mode</th>
<th>High Channel</th>
<th>Low Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single channel</strong></td>
<td>Any PSK</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Selected FSK</td>
<td>-</td>
</tr>
<tr>
<td><strong>Dual channel</strong></td>
<td>Any PSK</td>
<td>Any PSK</td>
</tr>
<tr>
<td></td>
<td>Selected FSK (≤ 2400 baud)</td>
<td>Any PSK</td>
</tr>
<tr>
<td></td>
<td>Any PSK</td>
<td>Selected FSK (≤ 2400 baud)</td>
</tr>
</tbody>
</table>
Physical frame

- Preamble for bit synchronization
- Unique Word for symbol synchronization
- Length field (handled by the device)

**PSK frame**: further byte for mode

- **FSK frame**:
DataLink frame

- Selectable CRC (length and algorithm)
- Length up to 254 bytes
- Security Services option: Payload Encryption
  - AES algorithm
  - Programmable Key
Transmission and reception settings

- **Transmission**: frame built in accordance with one of the 3 modes (PHY, DL, SS) selectable at each request

- **Reception**: only one mode, selectable and stored internally
  - Process begins after PRE+UW sequence detection
  - DL and SS frames: fields check
  - Sniffer option: notification of malformed or wrong DL, SS frames
ST7580
Host Interface
• Local port is an UART interface
• ST7580 is the communication master
• Communication handled through 5 digital pins:
  • **TXD**: Transmitting Output Data
  • **RXD**: Receiving Input Data
  • **T_REQ**: Arbitration Signal
  • **BR0/TXP/TXD**:
  • **BR1/RXP/RXD**:

**Baudrate settings**

<table>
<thead>
<tr>
<th>BR1</th>
<th>BR0</th>
<th>Baudrate (bps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>9600</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>19200</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>38400</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>57600</td>
</tr>
</tbody>
</table>
Physical Data Transfer

- UART Serial Interface
- Half Duplex mode
- Physical frame: start bit, 8 data bits, stop bit
- NRZ Coding

**Endianness: lsb first**

<table>
<thead>
<tr>
<th>IDLE state (mark)</th>
<th>LSB</th>
<th>MSB</th>
<th>IDLE state (mark)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Bit</td>
<td>D0</td>
<td>D1</td>
<td>D2</td>
</tr>
</tbody>
</table>

8 data bits

1 character
**UART Uplink (ST7580 to external Host)**

- ST7580 is the communication master and can transmit at any time
- ACK/NACK awaited within $T_{ACK}$
- **New/Repeated Transmission after $T_{WBC}$**
The External Host is the communication slave. It must ask for permission by setting T_REQ low.

Frame transmission by host within T_SR (after T_REQ high).

ACK/NACK returned by ST7580 after reception.
Host Interface Messages

• **ACK and NACK**
  - Sent by both ST7580 and host
  - 1 Byte long
  - Codes: **06h** (ACK) **15h** (NACK)

• **Status Message**
  - Sent by ST7580 after a transmission request by host
  - 2 Bytes long
  - Codes:
    - **3Fh** for byte 0
    - Depending on ST7580 settings for byte 1
Local Frame

- Sent by both ST7580 and host

<table>
<thead>
<tr>
<th>STX</th>
<th>Length</th>
<th>Command Code</th>
<th>DATA</th>
<th>Checksum</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Byte</td>
<td>1 Byte</td>
<td>1 Byte</td>
<td>0 .. 255 Bytes</td>
<td>2 Bytes</td>
</tr>
</tbody>
</table>

- **STX**: Start of text delimiter
- **Length**: byte length of data field
- **Command Code**: Command Type
- **Data**: Data to be sent
- **Checksum**: calculated on length, code, data
UART Data Flow: uplink messages

- Solicited messages from Host to ST7580:
  - Request command
  - Confirm command

- Total data flow:
  - T_REQ low
  - Status Message
  - Request Command
  - ACK
  - Confirm Command
  - ACK
UART Data Flow: downlink messages

- Unsolicited messages from Host to ST7580:

  - Indication command from ST7580 to HOST

- Total data flow:

  - Indication Command from HOST to ST7580
  - ACK from ST7580 to HOST
Example: Data transmission
Example: data reception

**Diagram:**
- **LINE**
- **T_REQ**
- **TXD**
- **RXD**

- **PL Frame**
- **Data indication**
- **ACK**

- **Time intervals:**
  - $b_1$
  - $a_1$
  - $b_2$
  - $c_1$
  - $b_3$
<table>
<thead>
<tr>
<th>Group</th>
<th>Command</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>BIO_ResetRequest</td>
<td>3Ch</td>
</tr>
<tr>
<td></td>
<td>BIO_ResetConfirm</td>
<td>3Dh</td>
</tr>
<tr>
<td>MIB</td>
<td>MIB_WriteRequest</td>
<td>08h</td>
</tr>
<tr>
<td></td>
<td>MIB_ReadRequest</td>
<td>0Ch</td>
</tr>
<tr>
<td></td>
<td>MIB_EraseRequest</td>
<td>10h</td>
</tr>
<tr>
<td></td>
<td>MIB_WriteConfirm</td>
<td>09h</td>
</tr>
<tr>
<td></td>
<td>MIB_ReadConfirm</td>
<td>0Dh</td>
</tr>
<tr>
<td></td>
<td>MIB_EraseConfirm</td>
<td>11h</td>
</tr>
<tr>
<td>Data</td>
<td>PHY_DataRequest</td>
<td>24h</td>
</tr>
<tr>
<td></td>
<td>DL_DataRequest</td>
<td>50h</td>
</tr>
<tr>
<td></td>
<td>SS_DataRequest</td>
<td>54h</td>
</tr>
<tr>
<td></td>
<td>PHY_DataConfirm</td>
<td>25h</td>
</tr>
<tr>
<td></td>
<td>DL_DataConfirm</td>
<td>51h</td>
</tr>
<tr>
<td></td>
<td>SS_DataConfirm</td>
<td>55h</td>
</tr>
<tr>
<td></td>
<td>PHY_DataIndication</td>
<td>26h</td>
</tr>
<tr>
<td></td>
<td>DL_DataIndication</td>
<td>53h</td>
</tr>
<tr>
<td></td>
<td>SS_DataIndication</td>
<td>57h</td>
</tr>
<tr>
<td>Index</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>-------------------------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>00h</td>
<td>Modem Configuration</td>
<td>Reception Mode, CRC</td>
</tr>
<tr>
<td>01h</td>
<td>PHY Configuration</td>
<td>Operating Frequencies, Reception channels, Modulation settings</td>
</tr>
<tr>
<td>02h</td>
<td>SS Key</td>
<td>Key to encrypt/decrypt SS frames</td>
</tr>
<tr>
<td>03h</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>04h</td>
<td>Last Data Indication</td>
<td>Information about last received data</td>
</tr>
<tr>
<td>05h</td>
<td>Last TX Confirm</td>
<td>Information about last transmitted data</td>
</tr>
<tr>
<td>06h</td>
<td>PHY_Data</td>
<td>Counters of PHY mode</td>
</tr>
<tr>
<td>07h</td>
<td>DL_Data</td>
<td>Counters of DL mode</td>
</tr>
<tr>
<td>08h</td>
<td>SS_Data</td>
<td>Counters of SS mode</td>
</tr>
<tr>
<td>09h</td>
<td>Host Interface Timeout</td>
<td>Max value for Host Interface Timeouts</td>
</tr>
<tr>
<td>0Ah</td>
<td>Firmware Version</td>
<td>Firmware version</td>
</tr>
</tbody>
</table>
ST7580
Reference Design Overview
Reference Design – Main sections

• Supply voltages

• Interfaces to STM32

• Power Line Interface
  • Transmission filter
  • Reception filter
  • Line coupling
  • Zero Crossing coupling

• Layout guidelines
Supply voltages

- The **ST7580** device operate from **two external supply voltages**:
  - **VCC** (8 to 18 V) as the main power supply;
  - **VDDIO** (3.3 or 5 V) for the I/O and digital sections.

- **Two internal linear regulators**:
  - 5 V (used by the AFE), generated from VCC and connected to **VCCA** pin;
  - 1.8 V (DSP and microcontroller cores, digital blocks, PLL and oscillator), generated from VDDIO and connected to **VDD_REG_1V8** and **VDD** pin.

- **VDD_PLL** externally connected to **VDD**

- **Internal regulators connected to VDD_REG_1V8 and VDDIO** are externally accessible for filtering purpose only
  - ➔ no loads allowed in the application circuit!
Supply scheme

- One 100nF capacitor close to each supply pin
- One 10uF capacitor per each supply voltage
- IMPORTANT: Pay attention to the correct supply-ground association!
- Ferrites used to block high-frequency disturbances
Interfaces to STM32

- UART
  - TXD
  - RXD
  - T_REQ
- RESETN
- PL_TX_ON and PL_RX_ON indications
- 8 MHz oscillator output
  - Sparing one 8 MHz quartz crystal
- PA_OUT and CL monitoring
Power Line coupling – TX and RX filters

• Transmission active filter
  - 3° order low-pass filter to reduce conducted disturbances
  - Designed to transfer the whole signal BW with < 1 dB in-band ripple

• Reception passive filter
  - Simple RLC band-pass filter
  - Designed with Q and BW in accordance with the signal BW
Power Line coupling: AC line coupling

- **AC Line Coupling circuit**
  - Protection from AC voltage and high-energy disturbances from the line
  - Band-pass behavior for impedance adapting

TX active filter + AC Line coupling

\[ Z_{load} = EN50065-1 LISN \]
**Power Line coupling – DC line coupling**

- **Configurable coupling circuit for DC applications:**
  - PV in DC series configuration
  - PV in HV-DC parallel configuration
  - 12, 24 or 48 V DC bus
  - ...
Power Line coupling - ZC coupling

**Isolated Zero Crossing circuit**
- Required for some solutions
- Higher safety but higher consumption
- Higher and more variable delay
- Critical for application lifetime

**Alternative: Non-isolated Zero Crossing circuit**
- Very simple and effective solution
- Gives a stable delay between the mains zero crossing and the ZC_IN as low as 20 μs
- Suitable for non-isolated design, such as metering applications
Layout guidelines - 1

• The Exposed pad has the purpose to guarantee very good thermal dissipation
  - VSSA plane below used as dissipating copper area
  - A number of open vias is required for cooling through air convection

• To avoid soldering issues about the Exposed pad, the solder paste quantity on the PCB top layer pad should be controlled

• A good solder paste distribution can be achieved with several small stencil openings:
• Extend the GND ground plane under the crystal

• Use large routes (≥ 12 mils) for VCC and PA_OUT (high-current lines)

• Keep the bypass capacitors close to each relative supply pin

• Keep supply and ground loops as short as possible to improve radiated disturbance immunity

• Keep good connection between top and bottom layers using several vias all around the PCB
ST7580 Status

• Product Webpage: [here](#)
  • Full documentation (DS, UM, AN) available

• Evaluation board available
  • Webpage: [here](#)
  • Documentation and SW available

• Mass production, ST7580 Lead Time: 18 wks
ST7580

Comparison with ST7540
### ST7540 vs. ST7580 (1)

<table>
<thead>
<tr>
<th>Feature</th>
<th>ST7540</th>
<th>ST7580</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier frequency value</td>
<td>To be selected among 8 values</td>
<td>Any value (1 Hz resolution) between 9 kHz and 250 kHz</td>
</tr>
<tr>
<td>Channel reception</td>
<td>Single</td>
<td>Dual (2400 bps max)</td>
</tr>
<tr>
<td>PSK max. bitrate</td>
<td>Not supported</td>
<td>28800 bps</td>
</tr>
<tr>
<td>FSK max. bitrate</td>
<td>4800 bps</td>
<td>9600 bps</td>
</tr>
<tr>
<td>Powerline frame format</td>
<td>Selectable composition</td>
<td>Fixed composition</td>
</tr>
<tr>
<td>Powerline frame length</td>
<td>Selectable (bits)</td>
<td>Selectable (bytes)</td>
</tr>
<tr>
<td>Host interface</td>
<td>SPI</td>
<td>UART</td>
</tr>
<tr>
<td>Host interface dataflow</td>
<td>Bitstream</td>
<td>Frame syntax</td>
</tr>
<tr>
<td>Host interface max. bitrate</td>
<td>4800 bps</td>
<td>57600 bps</td>
</tr>
<tr>
<td>Host interface delays</td>
<td>Fixed</td>
<td>Depending on processing</td>
</tr>
</tbody>
</table>
## ST7538 vs. ST7580 (2)

<table>
<thead>
<tr>
<th></th>
<th><strong>ST7540</strong></th>
<th><strong>ST7580</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Zero-Crossing synch</strong></td>
<td>Optional</td>
<td>Optional</td>
</tr>
<tr>
<td><strong>Embedded Power Amplifier</strong></td>
<td>Up to 500 mArms – 8 Vpp single ended output</td>
<td>Up to 1Arms-14 Vpp single ended output with advanced thermal protection</td>
</tr>
<tr>
<td><strong>Receiver sensitivity</strong></td>
<td>54 dBµV</td>
<td>35 dBµV</td>
</tr>
<tr>
<td><strong>Power supply</strong></td>
<td>Single:</td>
<td>Dual:</td>
</tr>
<tr>
<td></td>
<td>• from 7.5 V to 12.5 V</td>
<td>• Analog part: from 8 V to 18 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Digital part: 3.3 V (or 5 V)</td>
</tr>
<tr>
<td><strong>Idle mode consumption</strong></td>
<td>5 mA</td>
<td>• Analog part: 6 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Digital part: 40 mA</td>
</tr>
<tr>
<td><strong>External clock frequency</strong></td>
<td>16 MHz</td>
<td>8 MHz</td>
</tr>
<tr>
<td><strong>Collision detection</strong></td>
<td>BU (Band-in-Use) pin signaling communication frequency occupancy</td>
<td>Digital output pins (TX_ON, RX_ON) signaling effective powerline communication</td>
</tr>
</tbody>
</table>
Powerline frame format

- **ST7580 frame (PHY layer):**
  ```
<table>
<thead>
<tr>
<th>Preamble (PRE)</th>
<th>Unique Word (UW)</th>
<th>Length</th>
<th>Payload</th>
</tr>
</thead>
<tbody>
<tr>
<td>from 2 up to 5 bytes</td>
<td>1 or 2 bytes</td>
<td>1 byte</td>
<td>from 0 up to 254 bytes</td>
</tr>
</tbody>
</table>
  ```

- **ST7540 frame (Header recognition):**
  ```
<table>
<thead>
<tr>
<th>Preamble (PRE)</th>
<th>Header</th>
<th>Payload</th>
</tr>
</thead>
<tbody>
<tr>
<td>variable</td>
<td>1 or 2 bytes</td>
<td>bitstream</td>
</tr>
</tbody>
</table>
  ```
## Powerline frame

<table>
<thead>
<tr>
<th></th>
<th><strong>Direction</strong></th>
<th><strong>ST7540</strong></th>
<th><strong>ST7580</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Preamble</strong></td>
<td>TX</td>
<td>To be added from Host</td>
<td>Automatically built</td>
</tr>
<tr>
<td></td>
<td>RX</td>
<td>Automatically handled</td>
<td>Automatically handled</td>
</tr>
<tr>
<td><strong>Header/UW</strong></td>
<td>TX</td>
<td>To be added from Host</td>
<td>Automatically built</td>
</tr>
<tr>
<td></td>
<td>RX</td>
<td>Automatically handled</td>
<td>Automatically handled</td>
</tr>
<tr>
<td><strong>Length</strong></td>
<td>TX</td>
<td>To be added from Host</td>
<td>Automatically built</td>
</tr>
<tr>
<td></td>
<td>RX</td>
<td>To be handled from Host</td>
<td>Automatically handled</td>
</tr>
<tr>
<td><strong>Payload</strong></td>
<td>TX/RX</td>
<td>Bit stream</td>
<td>Byte sort (254 max)</td>
</tr>
<tr>
<td><strong>CRC</strong></td>
<td>TX/RX</td>
<td>To be handled from Host</td>
<td>Eventually add DL layer</td>
</tr>
<tr>
<td><strong>Bit order</strong></td>
<td>TX/RX</td>
<td>Bit-to-bit (msb first)</td>
<td>Byte-to-byte (lsb first)</td>
</tr>
<tr>
<td><strong>UW order</strong></td>
<td>TX/RX</td>
<td>Msb</td>
<td>16-bit word, lsb first</td>
</tr>
</tbody>
</table>
ST7580 Open Discussion

Questions and answers