ST7580 presentation

Workshop on Powerline Communication

October 28th, 2014

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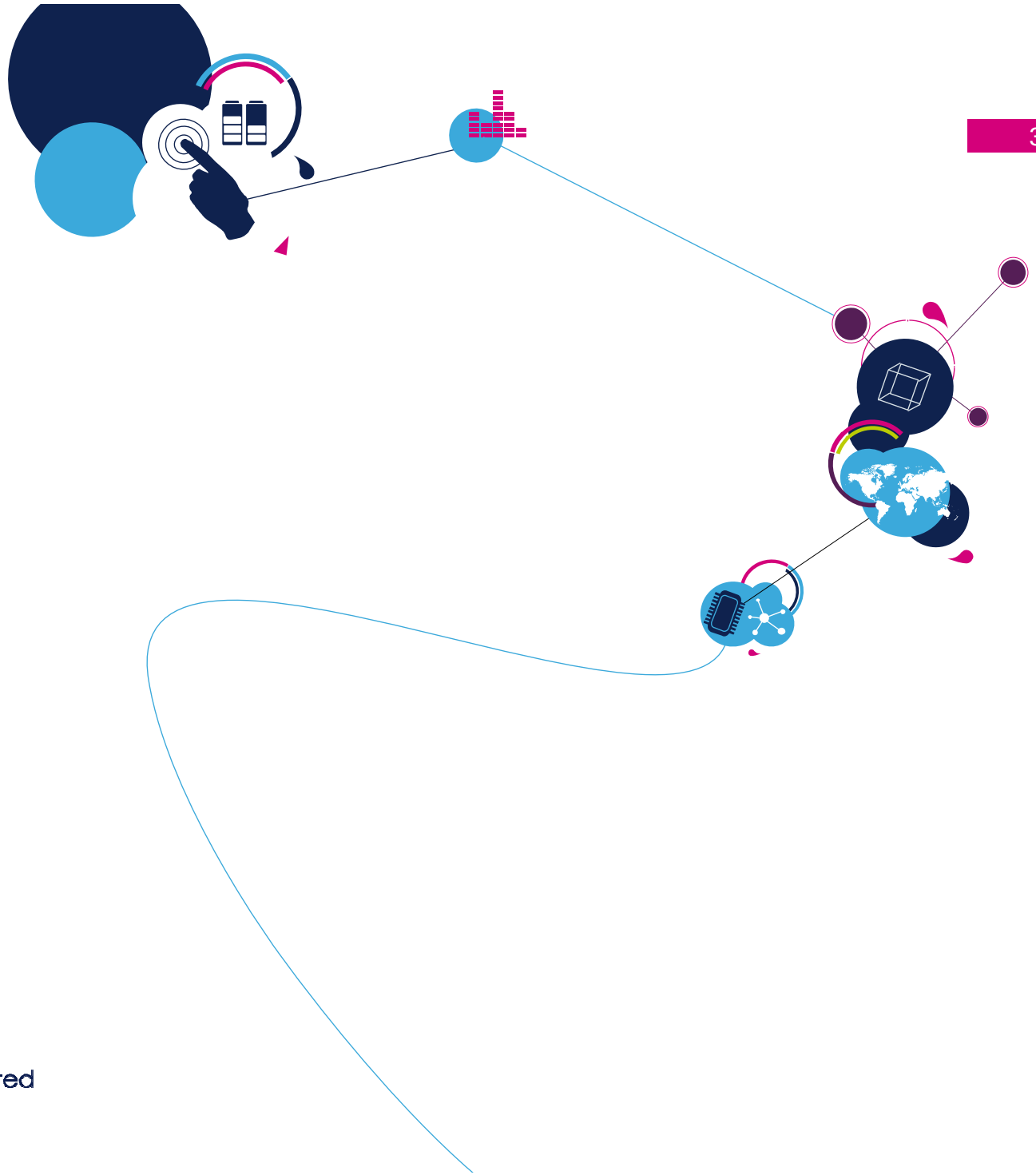
Agenda

- ST7580 product overview
  - Device Architecture
  - Protocol stack
  - Host Interface
- ST7580 Reference Design Overview
- ST7580 comparison with ST7540
- ST7580 Open discussion



ST7580

Device Architecture

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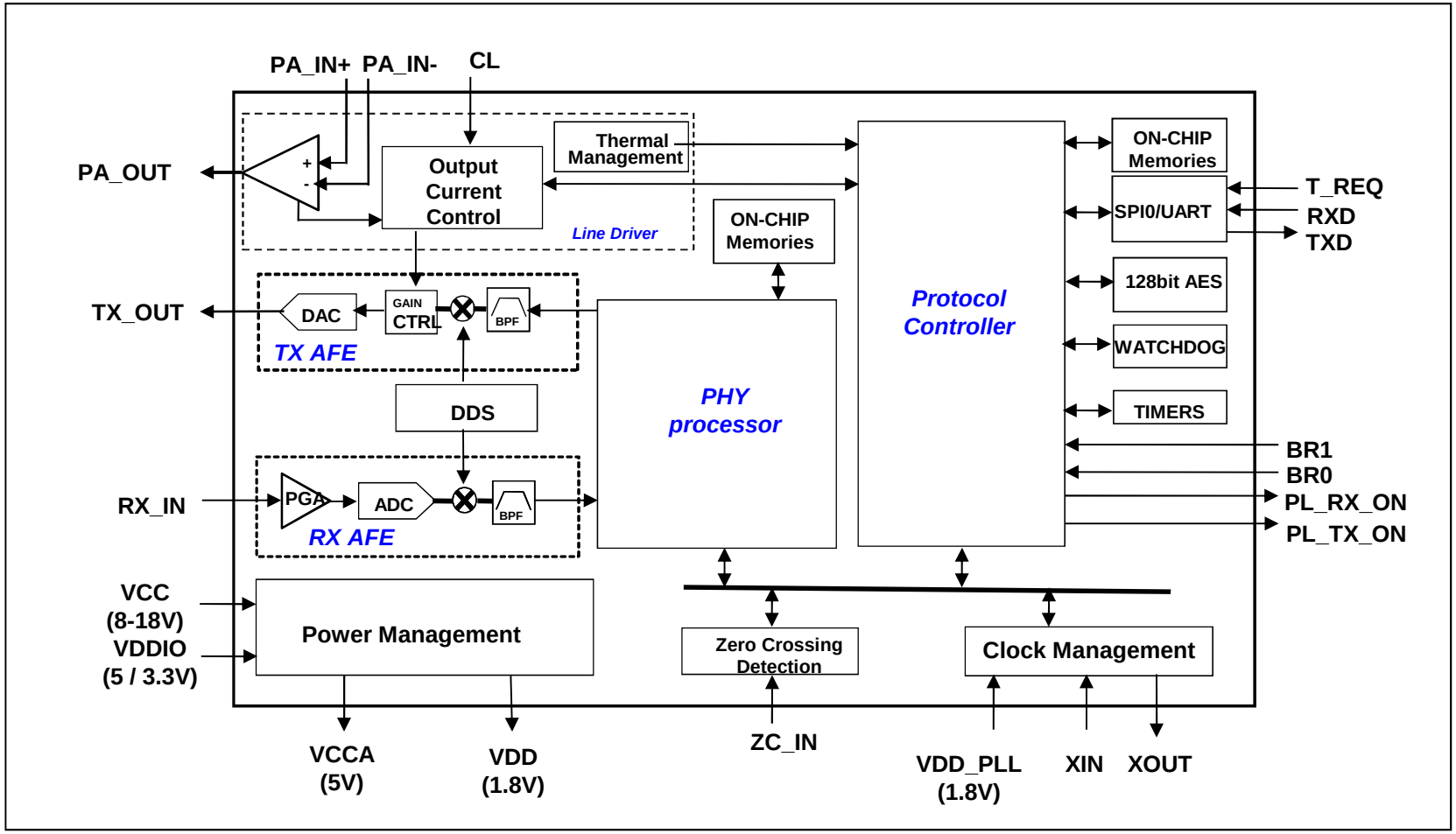
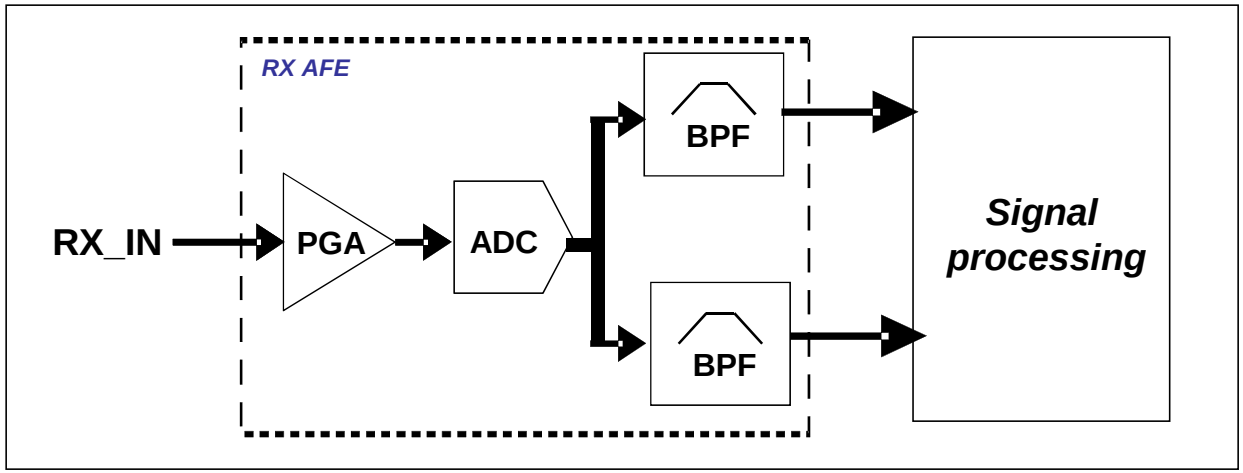
Block Diagram

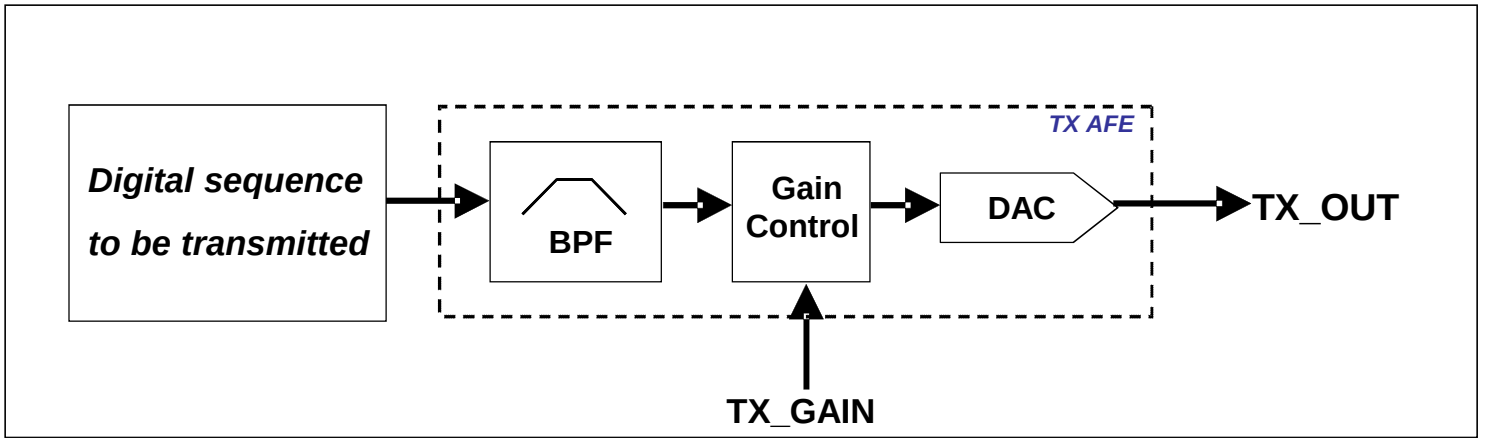


Analog Front End: Reception path



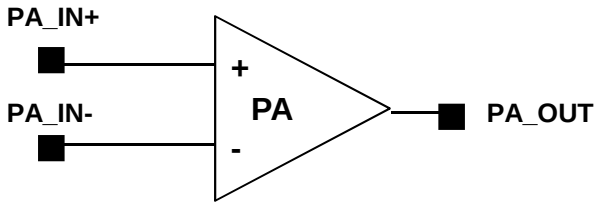
- Modulated Signal received on RX_IN pin
- Gain Adjustment performed by PGA block
- Digital conversion through $\Delta\sum$ - ADC
- Digital signal filtered around the two frequencies
- Demodulation by DSP engine

Analog Front End: Transmission path



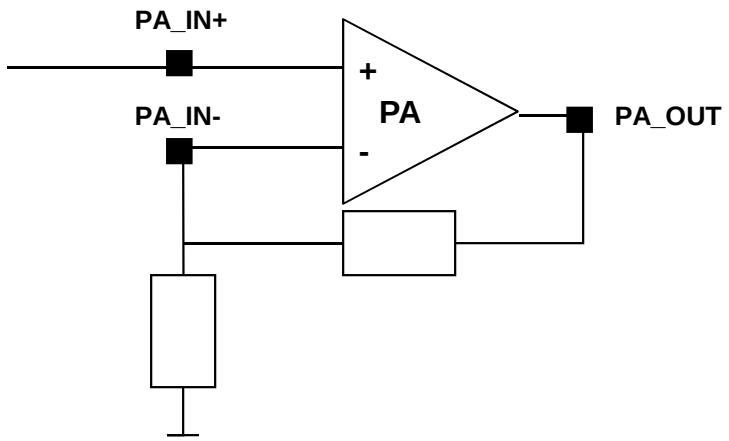
- FSK/PSK waveforms generated by the DSP
- Band-pass filter around selected frequency
- Gain attenuation: logarithmic scale, 32 steps
- TX_OUT pin for modulated signal transmission

Analog Front End: Power Amplifier (1)



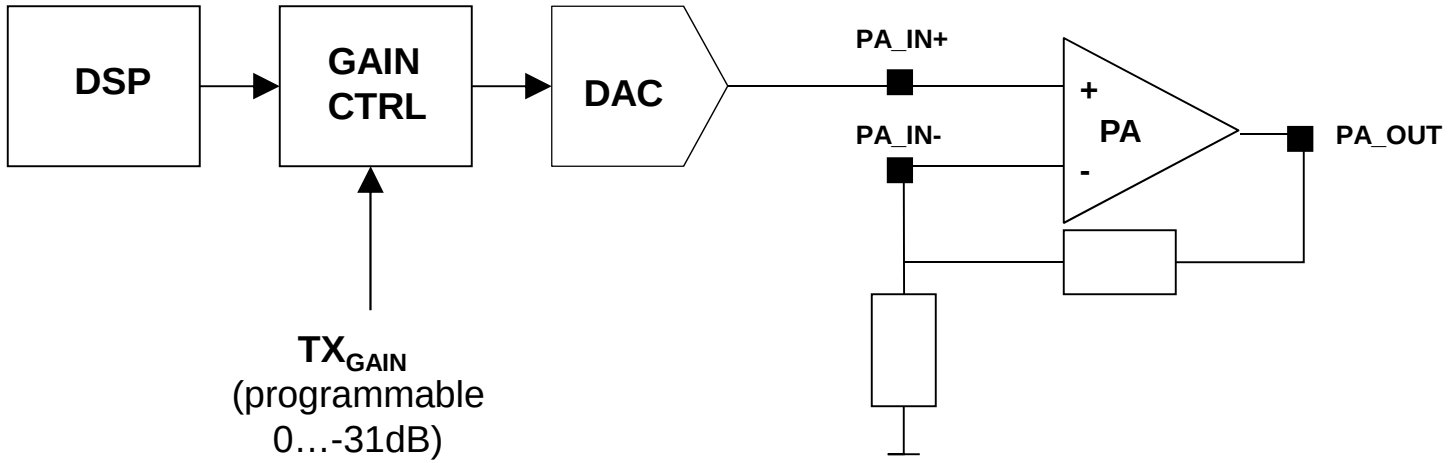
- Integrated Power Amplifier
  - 8 to 18V supply
  - 14Vpp max output
  - Up to 1Arms

Analog Front End: Power Amplifier (2)



- Power Amplifier pins externally available to build an active filter
- Gain set through the external network

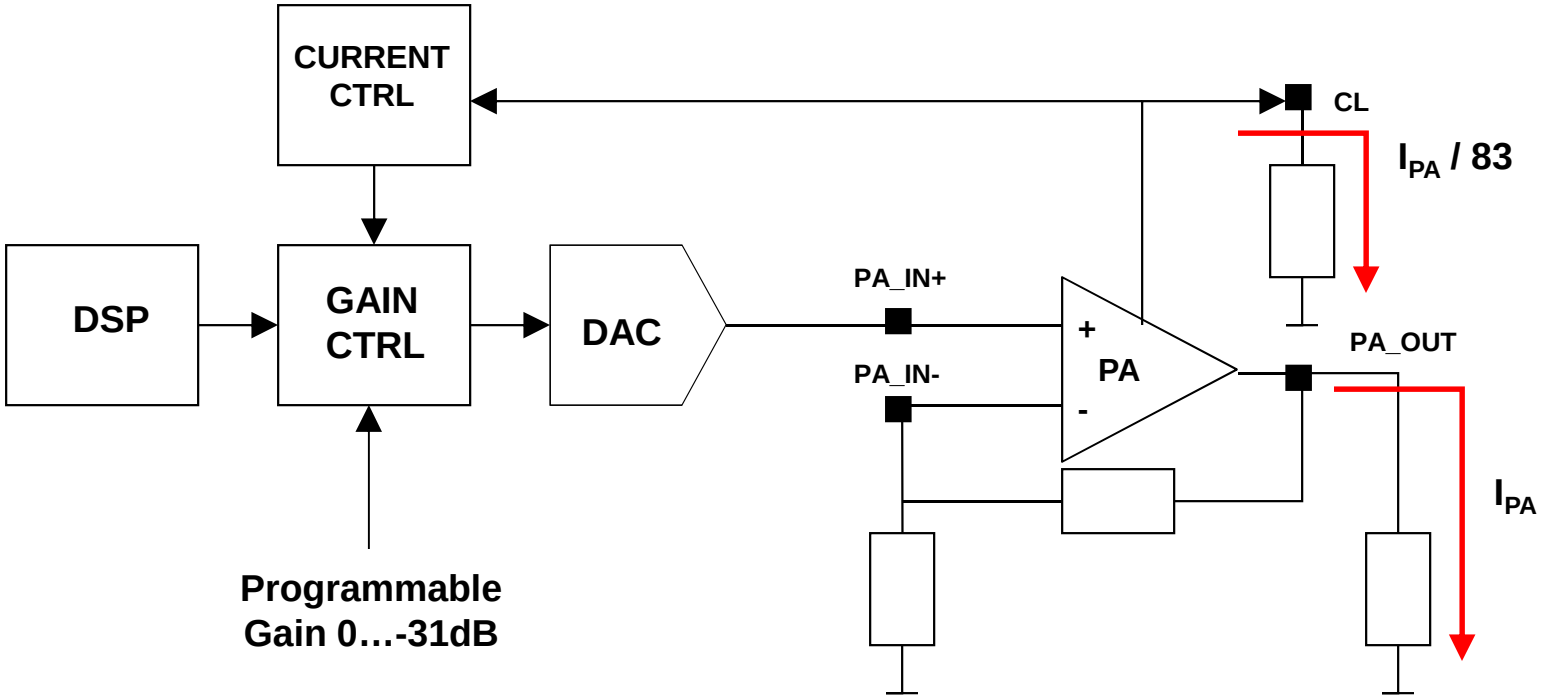
Analog Front End: Output Voltage



- Output voltage (Vpp): $V_{OUT} = V_{DAC} \cdot TX_{GAIN} \cdot PA_{GAIN}$

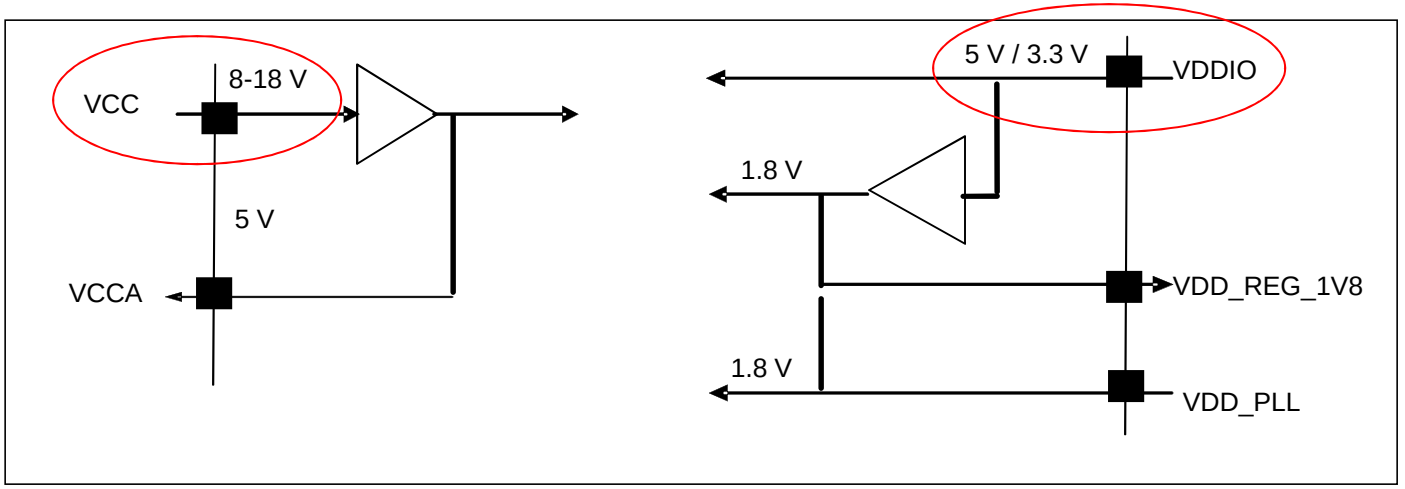
(where V_{DAC} = 4.8Vpp typ.)

Analog Front End: Current Limit



- A fraction (1/83) of output I_{PA} current is mirrored on CL pin
- Voltage value on CL pin is monitored to be below a fixed threshold
- Output gain is decreased if the threshold is overpassed

Power Management



- Two external power supply voltages required:
  - VCC (8V to 18V) for analog parts, max input current: 500 mA
  - VDDIO (3.3V to 5V) for digital sections, input current: 40 mA
- Internal regulators generating 5V and 1.8V
- Internal regulators externally available for filtering purpose only

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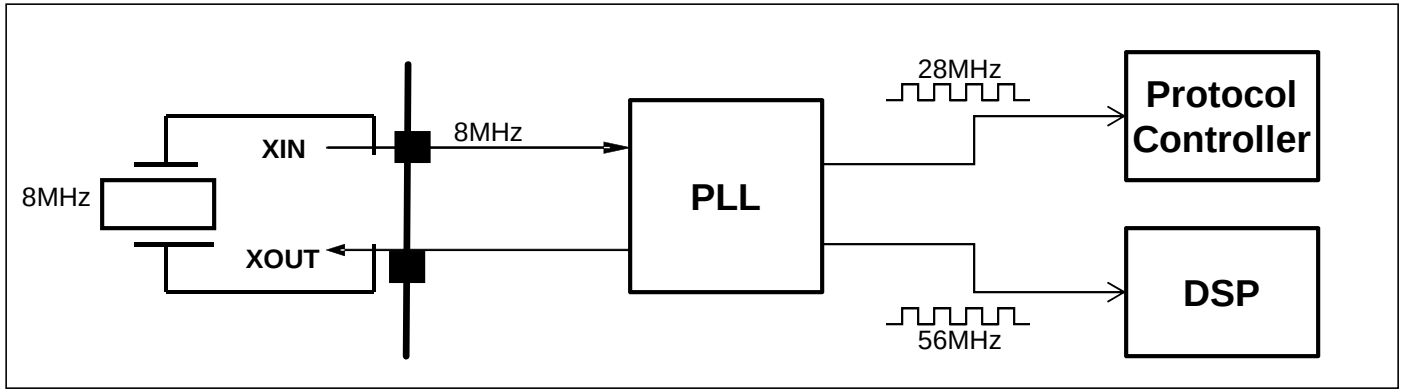
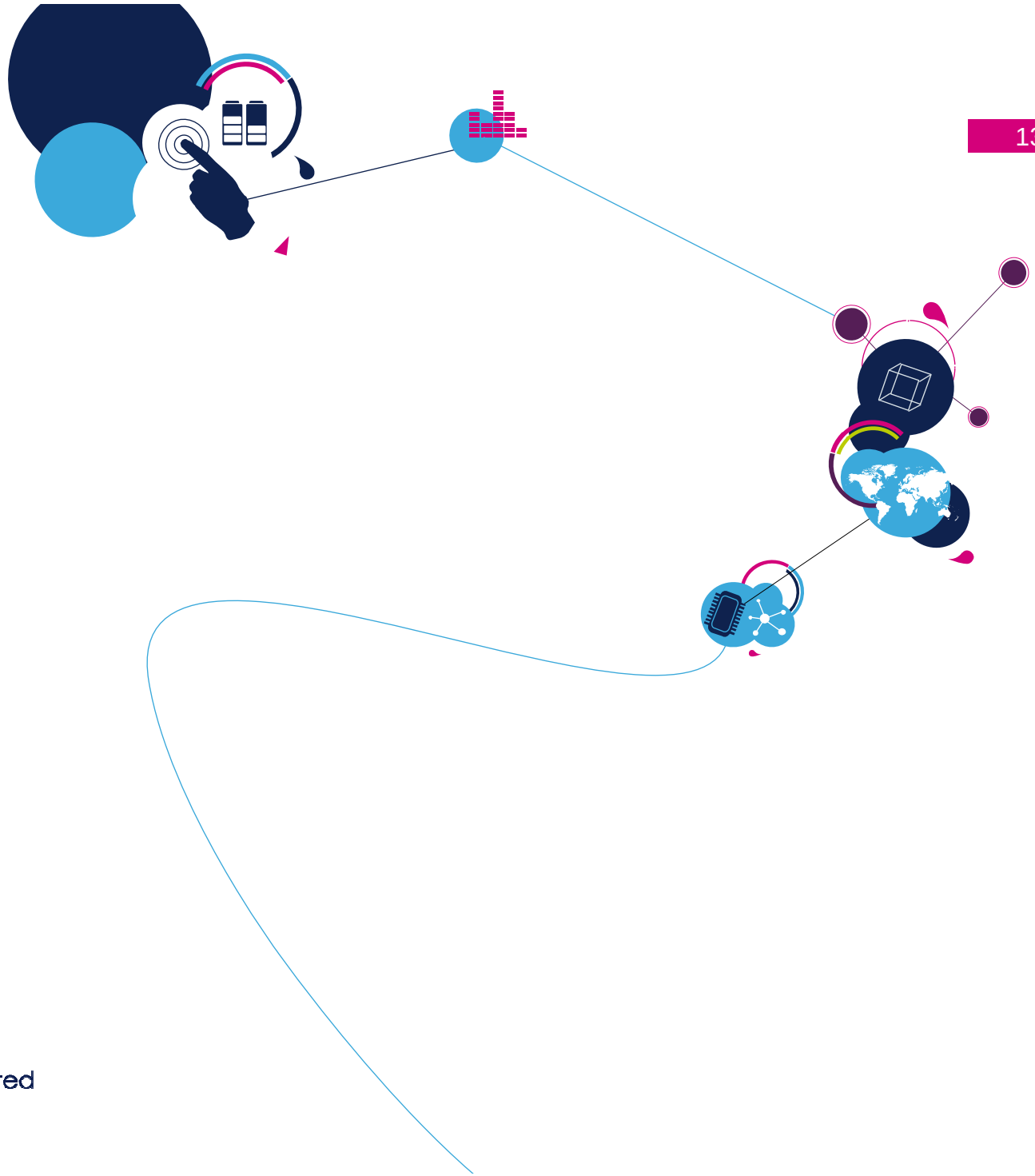
Clock Management



- 8MHz clock to be provided by external source:
  - Crystal through XIN and XOUT pins
  - External clock (on XIN pin)
- Load capacitance (32pF) integrated in pins
- Internal clock trees:
  - 28MHz: Microcontroller
  - 56MHz: DSP



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Protocol Stack

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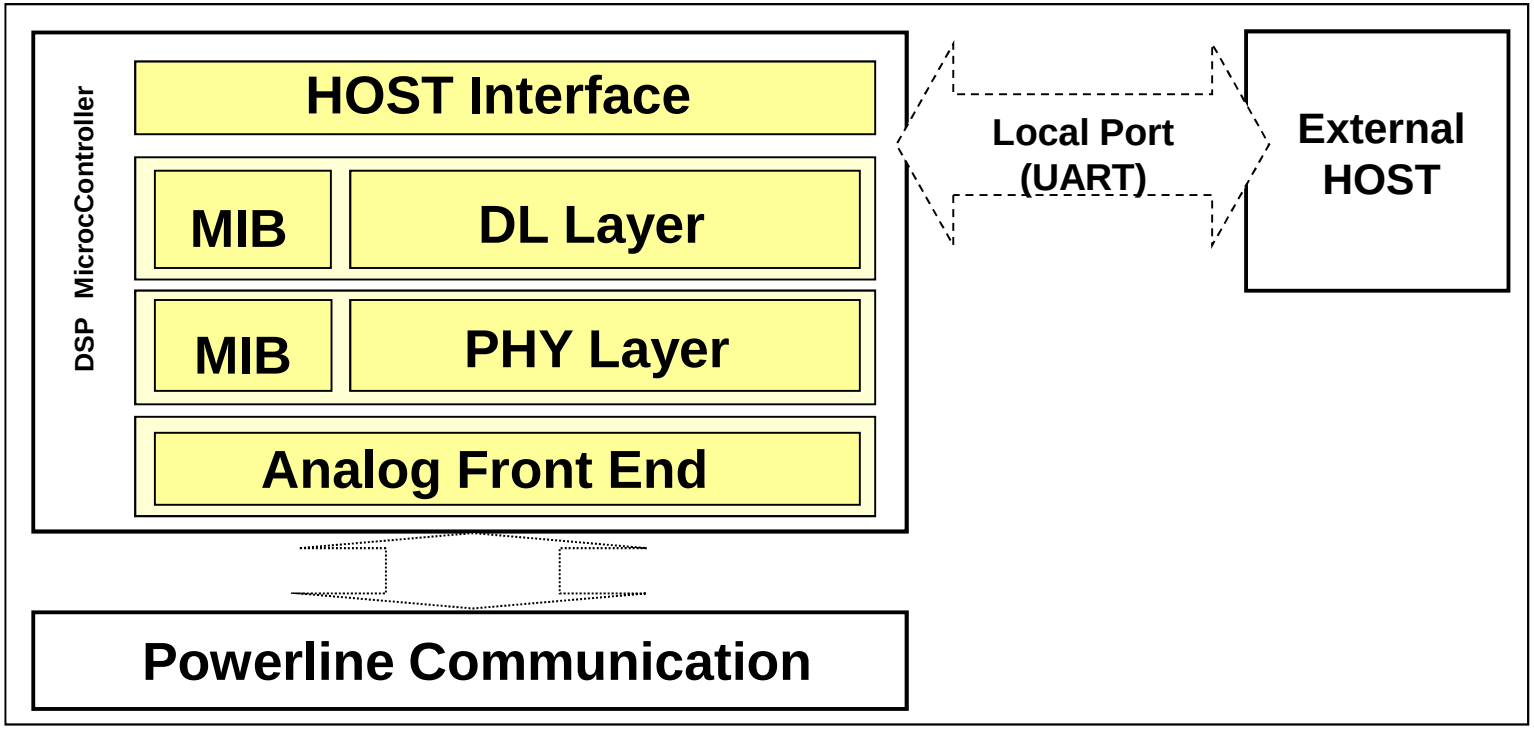
ST7580 Protocol Stack



- PHY and DL layers with framing services
- MIB to store configuration and information objects
- Host Interface to manage communication with an external host

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Modulation schemes

	Baudrate	Mode	Bitrate	Carrier
PSK	9600 bps	B-PSK	9600 bps	Selectable (CENELEC A, B, D band)
		B-PSK Coded	4800 bps	
		Q-PSK	19200 bps	
		Q-PSK Coded	9600 bps	
		8-PSK	28800 bps	
		B-PSK Coded PNA	2400 bps	
B-FSK	1200 bps	B-FSK	same as baudrate	Selectable (CENELEC A, B, D band)
	2400 bps			
	4800 bps			
	9600 bps			

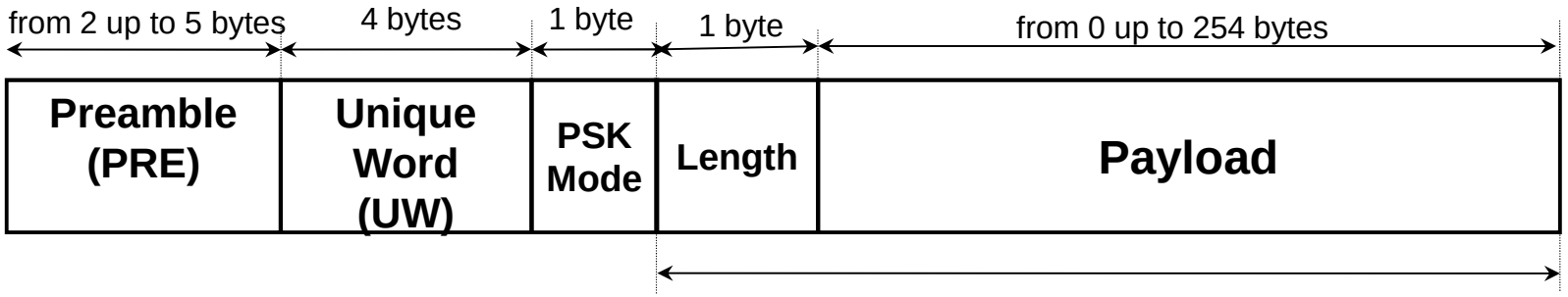
Channel selection

- Transmission
  - centered around a selectable frequency
  - performed through a selectable mode
- Reception
  - Two channels selectable through dedicated registers
  - Single (high) or Dual Channel mode
  - Only modulation type (PSK or FSK) over a single channel

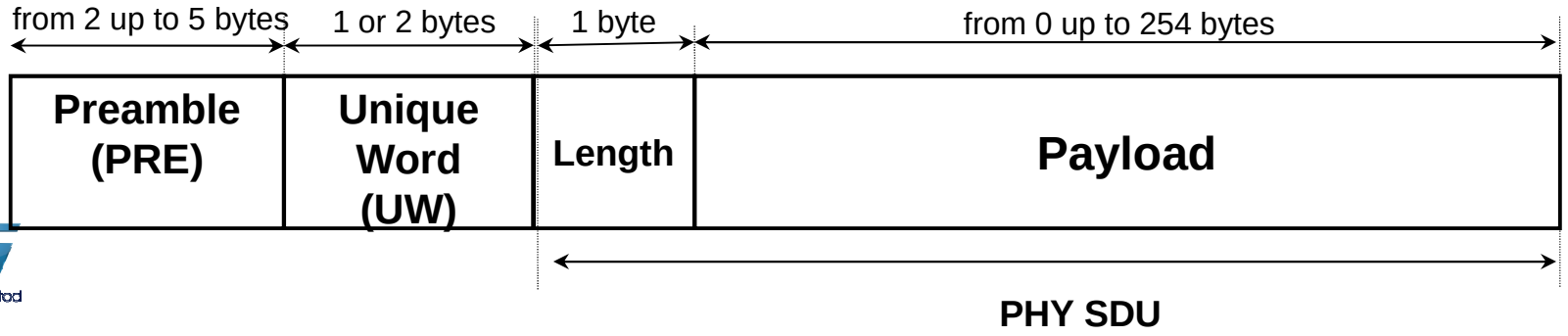
Reception mode	High Channel	Low Channel
Single channel	Any PSK	-
	Selected FSK	-
Dual channel	Any PSK	Any PSK
	Selected FSK (≤ 2400 baud)	Any PSK
	Any PSK	Selected FSK (≤ 2400 baud)

Physical frame

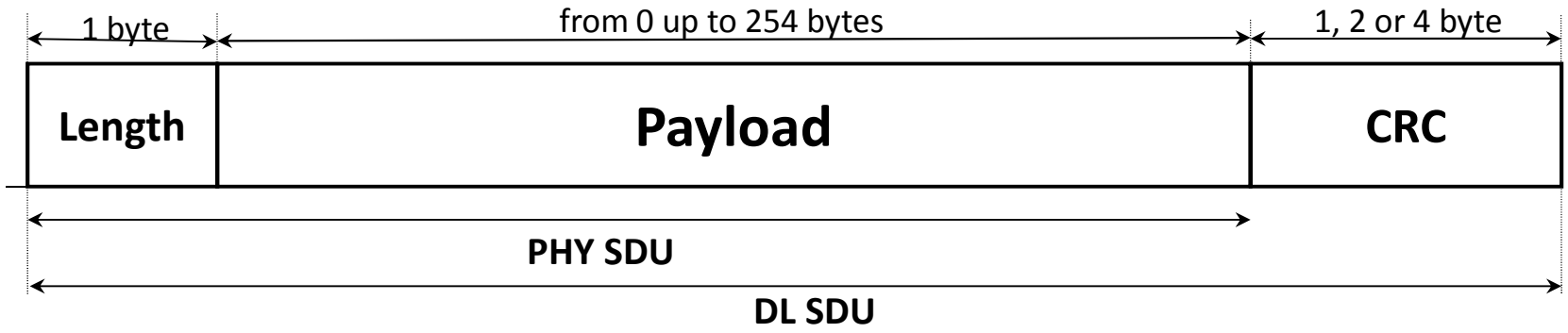
- Preamble for bit synchronization
- Unique Word for symbol synchronization
- Length field (handled by the device)
- PSK frame: further byte for mode



- FSK frame:



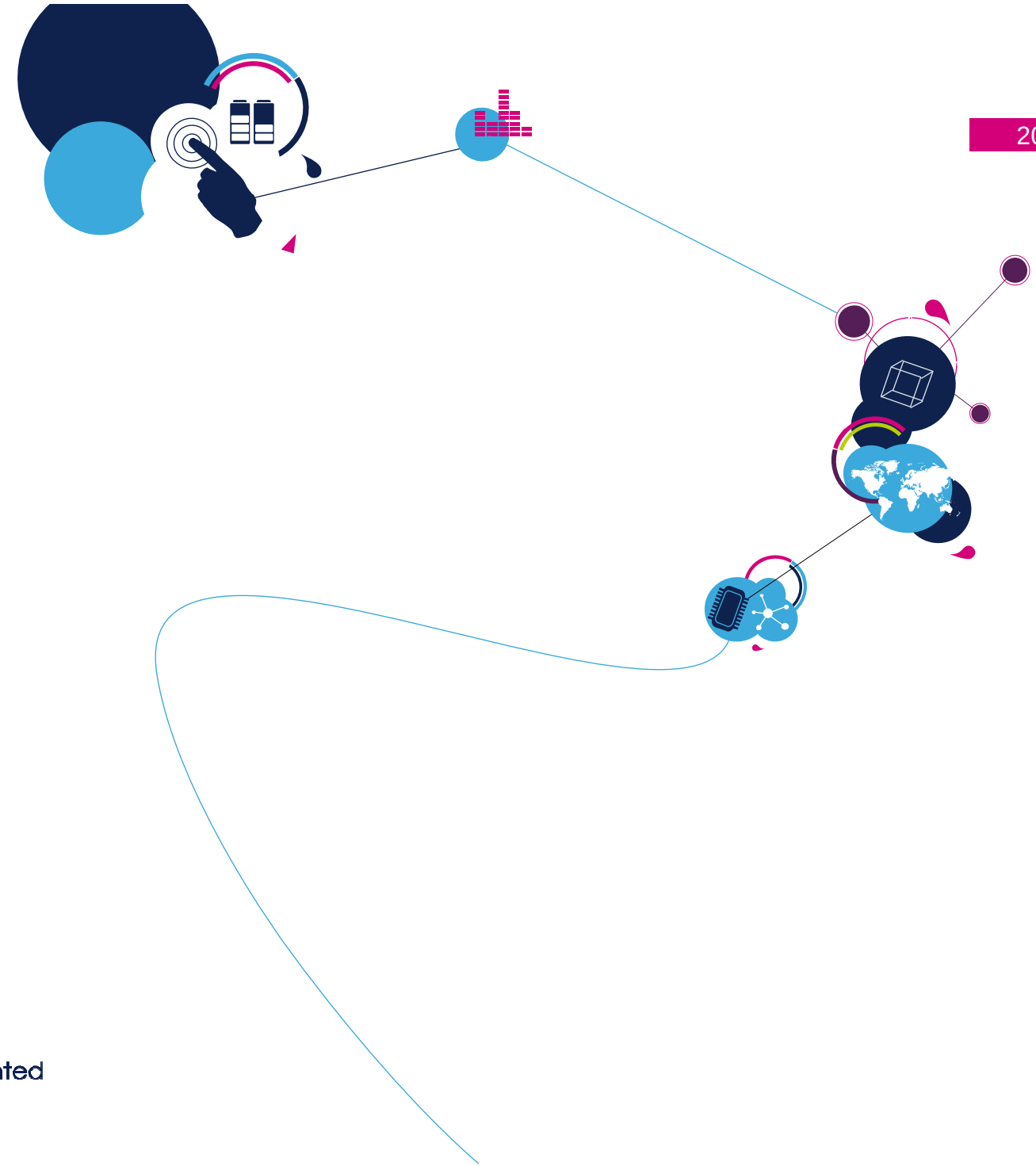
DataLink frame



- Selectable CRC (length and algorithm)
- Length up to 254 bytes
- Security Services option: Payload Encryption
  - AES algorithm
  - Programmable Key

Transmission and reception settings

- Transmission: frame built in accordance with one of the 3 modes (PHY, DL, SS) selectable at each request
- Reception: only one mode, selectable and stored internally
  - Process begins after PRE+UW sequence detection
  - DL and SS frames: fields check
  - Sniffer option: notification of malformed or wrong DL, SS frames



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Host Interface

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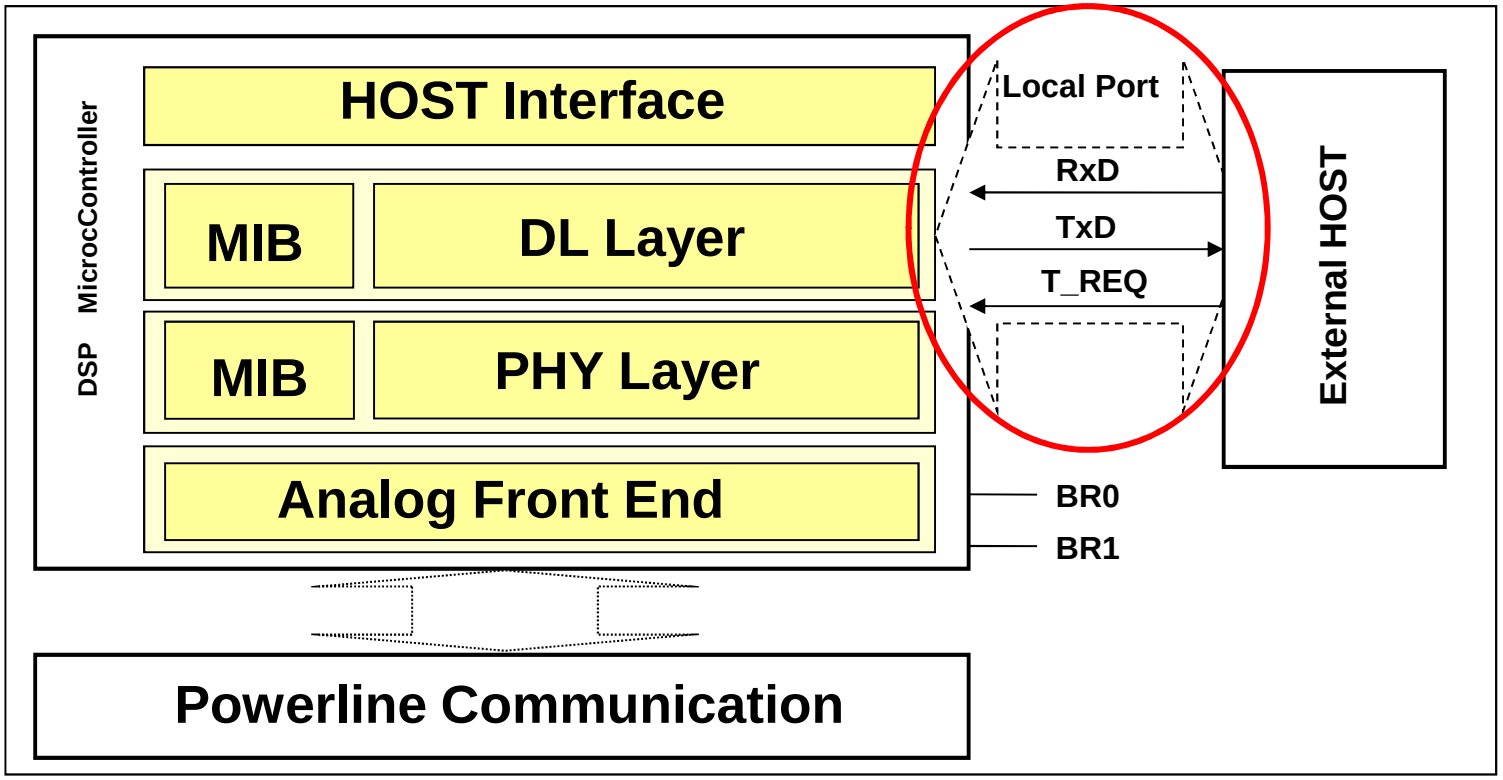
ST7580 Host Interface



- Local port is an UART interface
- ST7580 is the communication master

Local Port

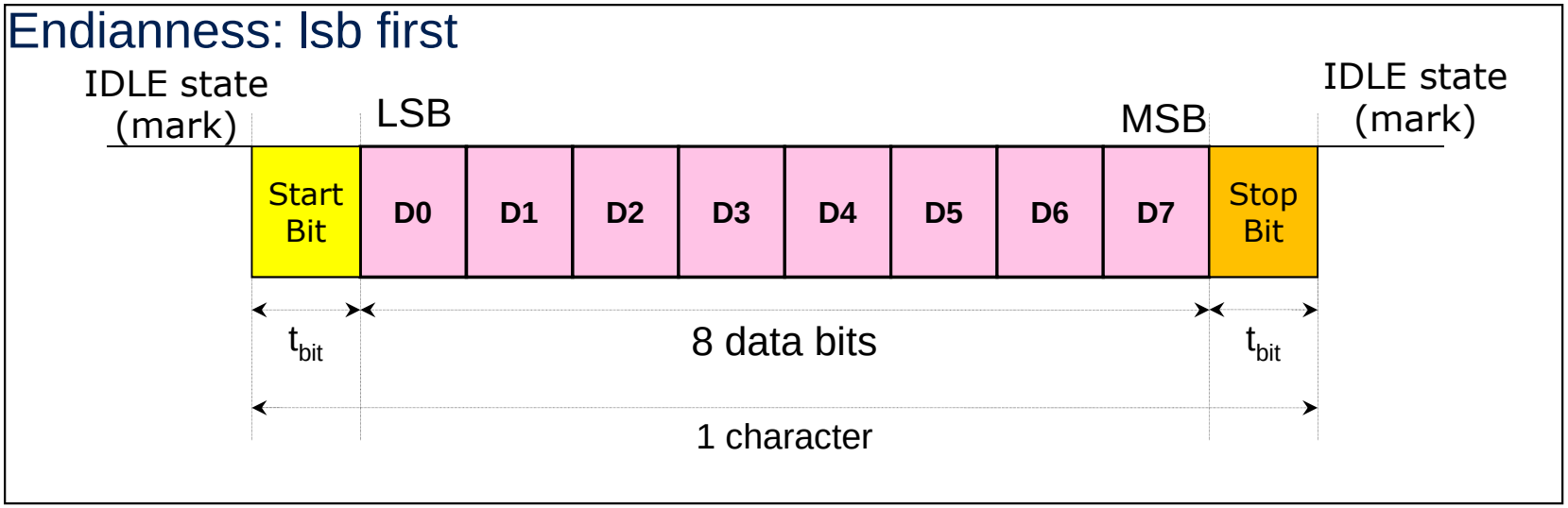
- Communication handled through 5 digital pins:
  - **TXD**: Transmitting Output Data
  - **RXD**: Receiving Input Data
  - **T_REQ**: Arbitration Signal
  - **BR0/TXP/TXD**:
  - **BR1/RXP/RXD**:

Baudrate settings

BR1	BR0	Baudrate (bps)
0	0	**9600**
0	1	**19200**
1	0	**38400**
1	1	**57600**

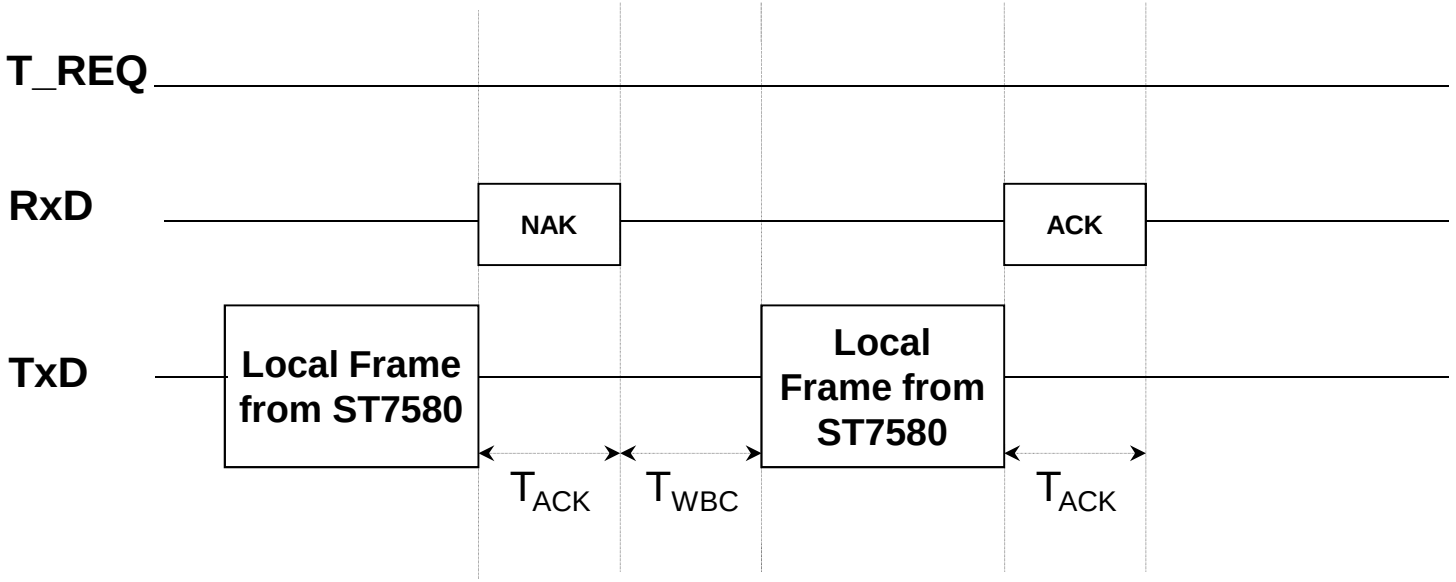
Physical Data Transfer

- UART Serial Interface
- Half Duplex mode
- Physical frame: start bit, 8 data bits, stop bit
- NRZ Coding
- Endianness: lsb first



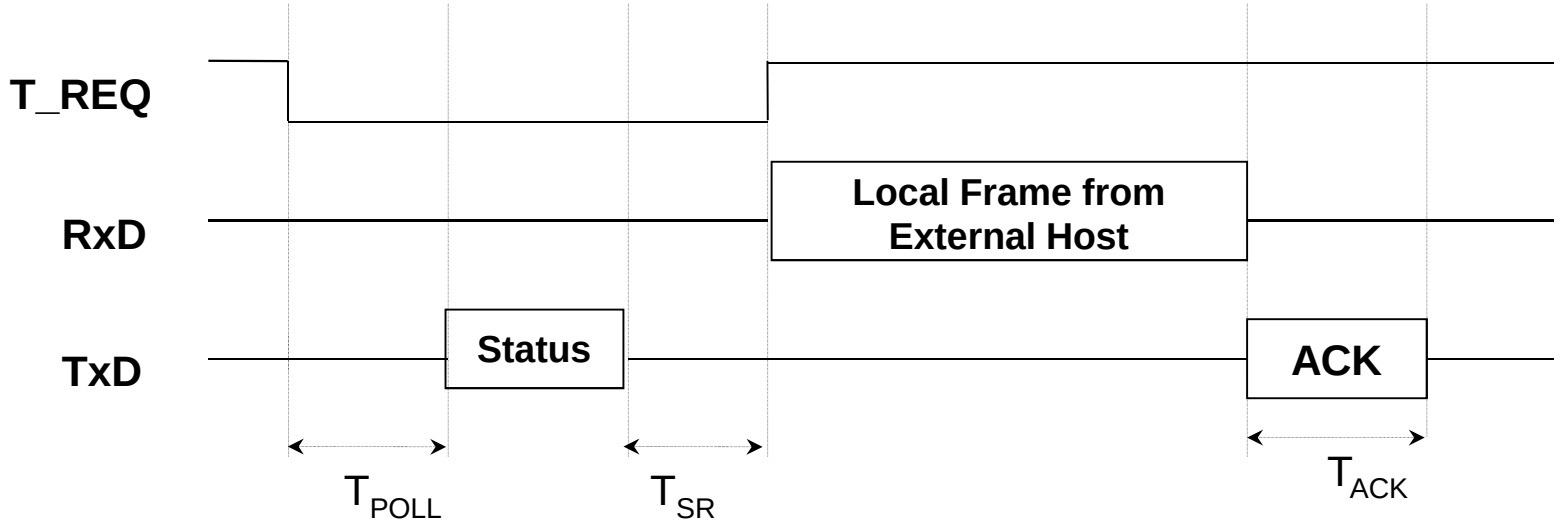
UART Uplink (ST7580 to external Host)

- ST7580 is the communication master and can transmit at any time
- ACK/NACK awaited within T_{ACK}
- New/Repeated Transmission after T_{WBC}



UART Downlink (External Host to ST7580)

- The External Host is the communication slave. It must ask for permission by setting T_REQ low
- Frame transmission by host within T_{SR} (after T_REQ high)
- ACK/NACK returned by ST7580 after reception



Host Interface Messages

- ACK and NACK
  - Sent by both ST7580 and host
  - 1 Byte long
  - Codes: **06h** (ACK) **15h** (NACK)
- Status Message
  - Sent by ST7580 after a transmission request by host
  - 2 Bytes long
  - Codes:
    - **3Fh** for byte 0
    - Depending on ST7580 settings for byte 1

Local Frame

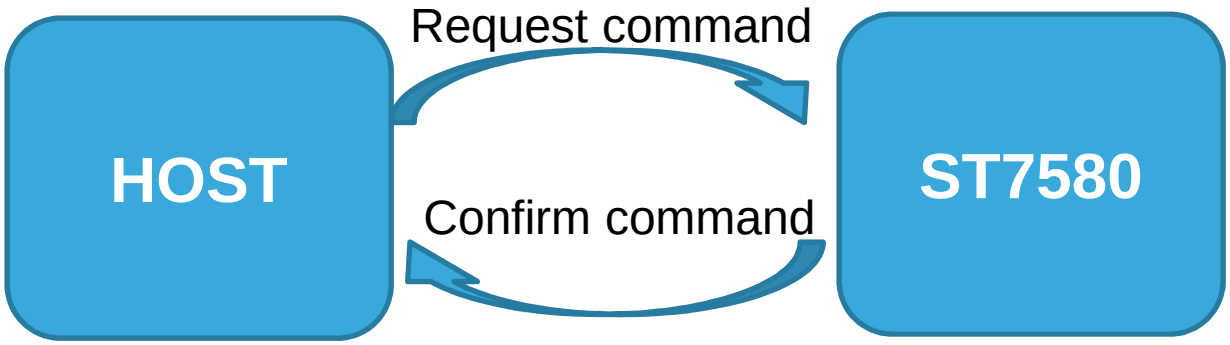
- Sent by both ST7580 and host

	STX	Length	Command Code	DATA	Checksum
Byte Length	1 Byte	1 Byte	1 Byte	0 .. 255 Bytes	2 Bytes
Value	**02h**	**0 .. 255**	**00h .. FFh**		

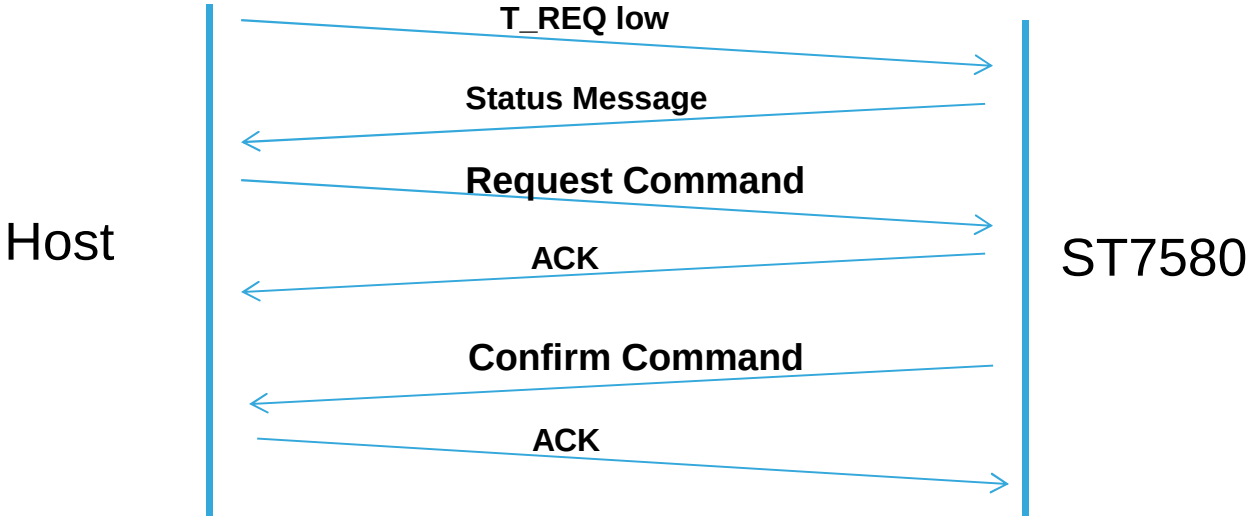
- **STX**: Start of text delimiter
- **Length**: byte length of data field
- **Command Code:** Command Type
- **Data:** Data to be sent
- **Checksum**: calculated on length, code, data

UART Data Flow: uplink messages

- Solicited messages from Host to ST7580:

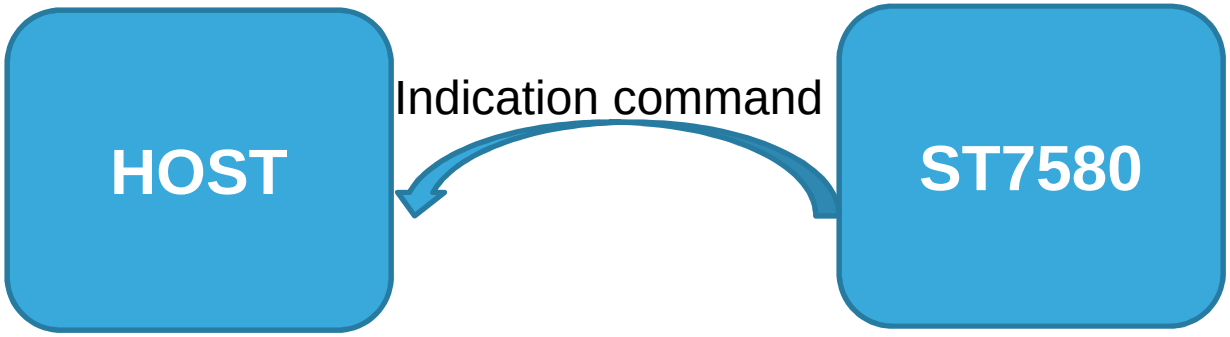


- Total data flow:

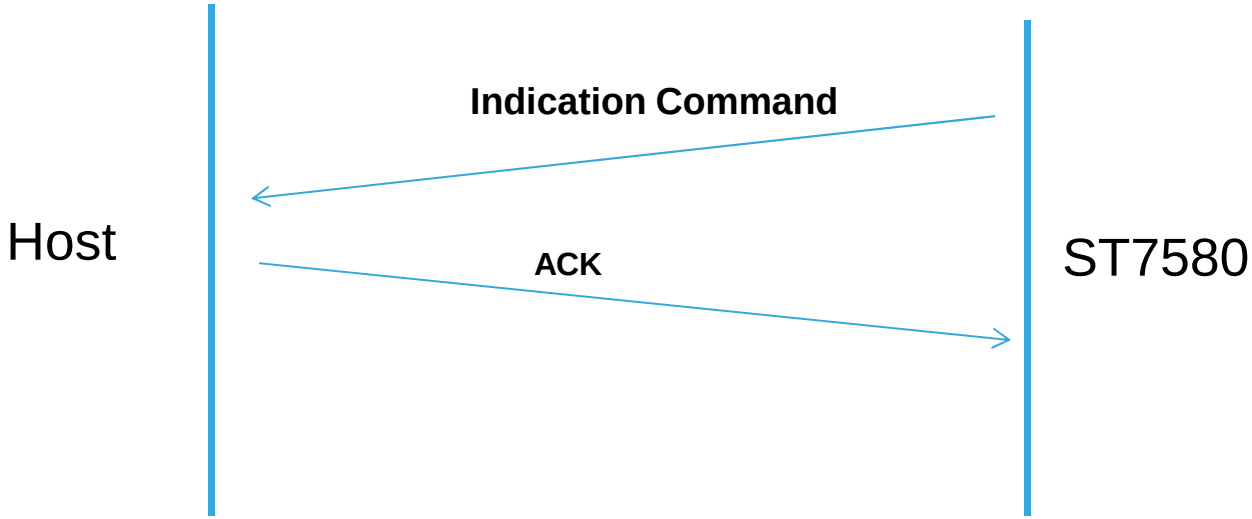


UART Data Flow: downlink messages

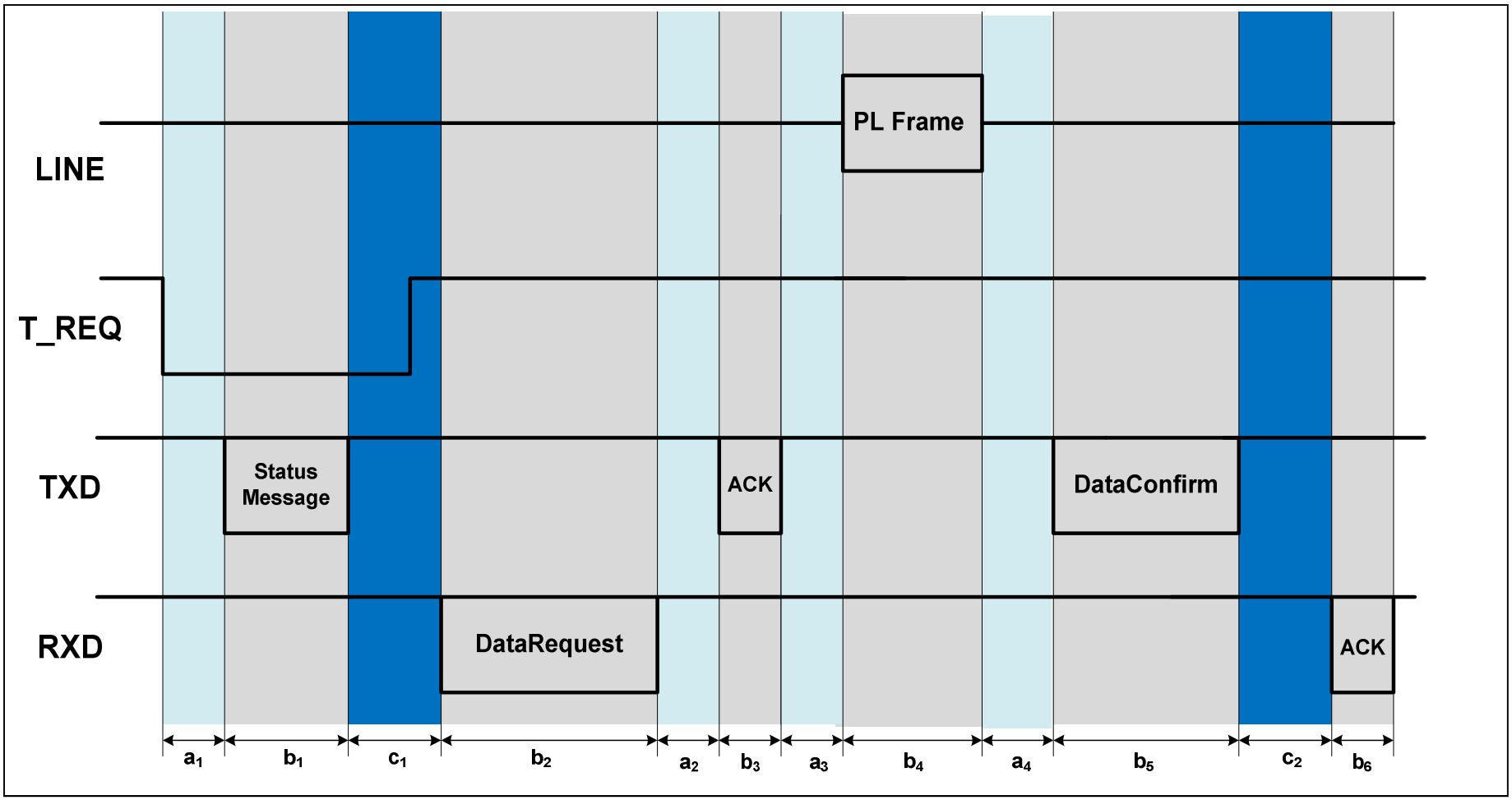
- Unsolicited messages from Host to ST7580:



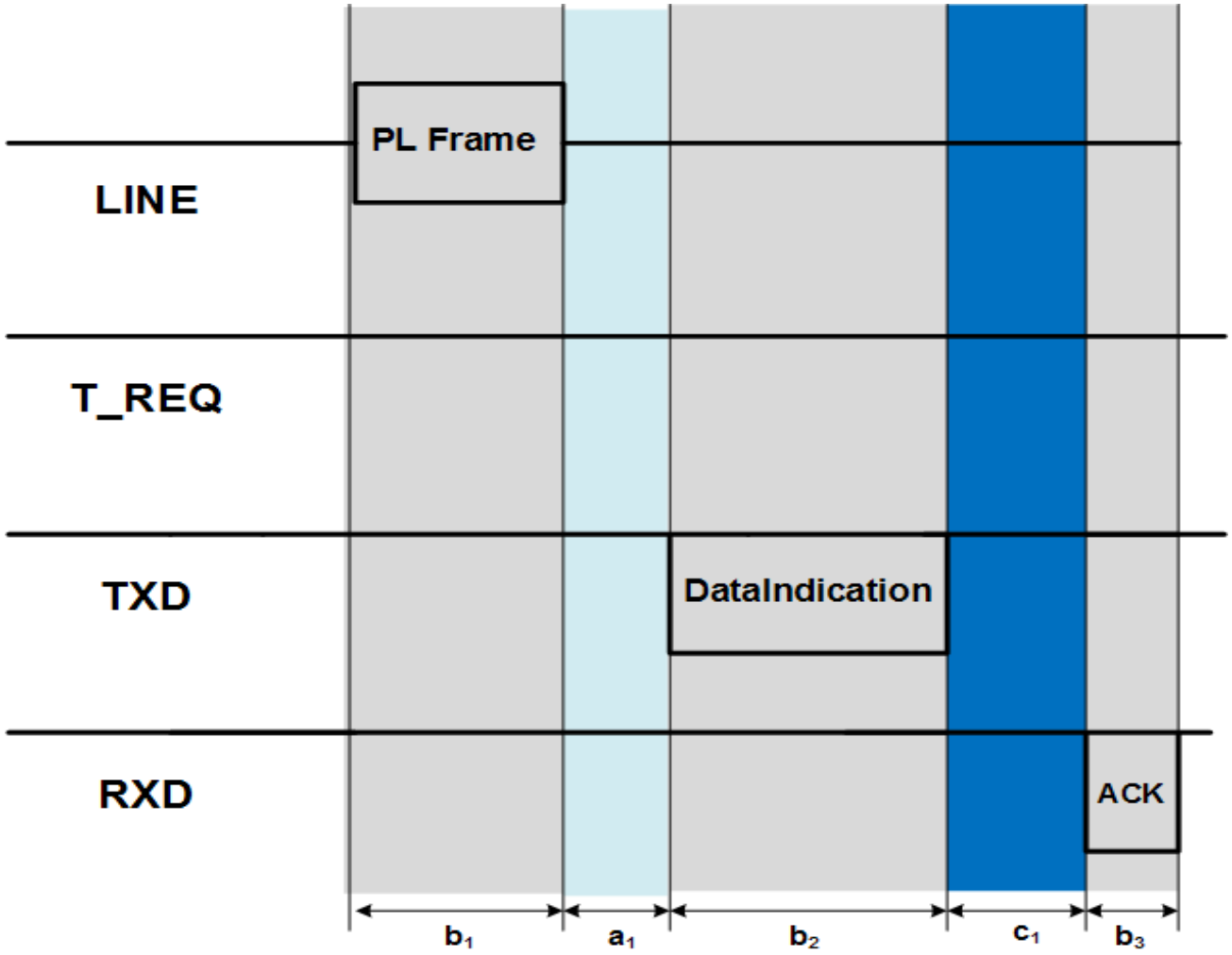
- Total data flow:



Example: Data transmission



Example: data reception

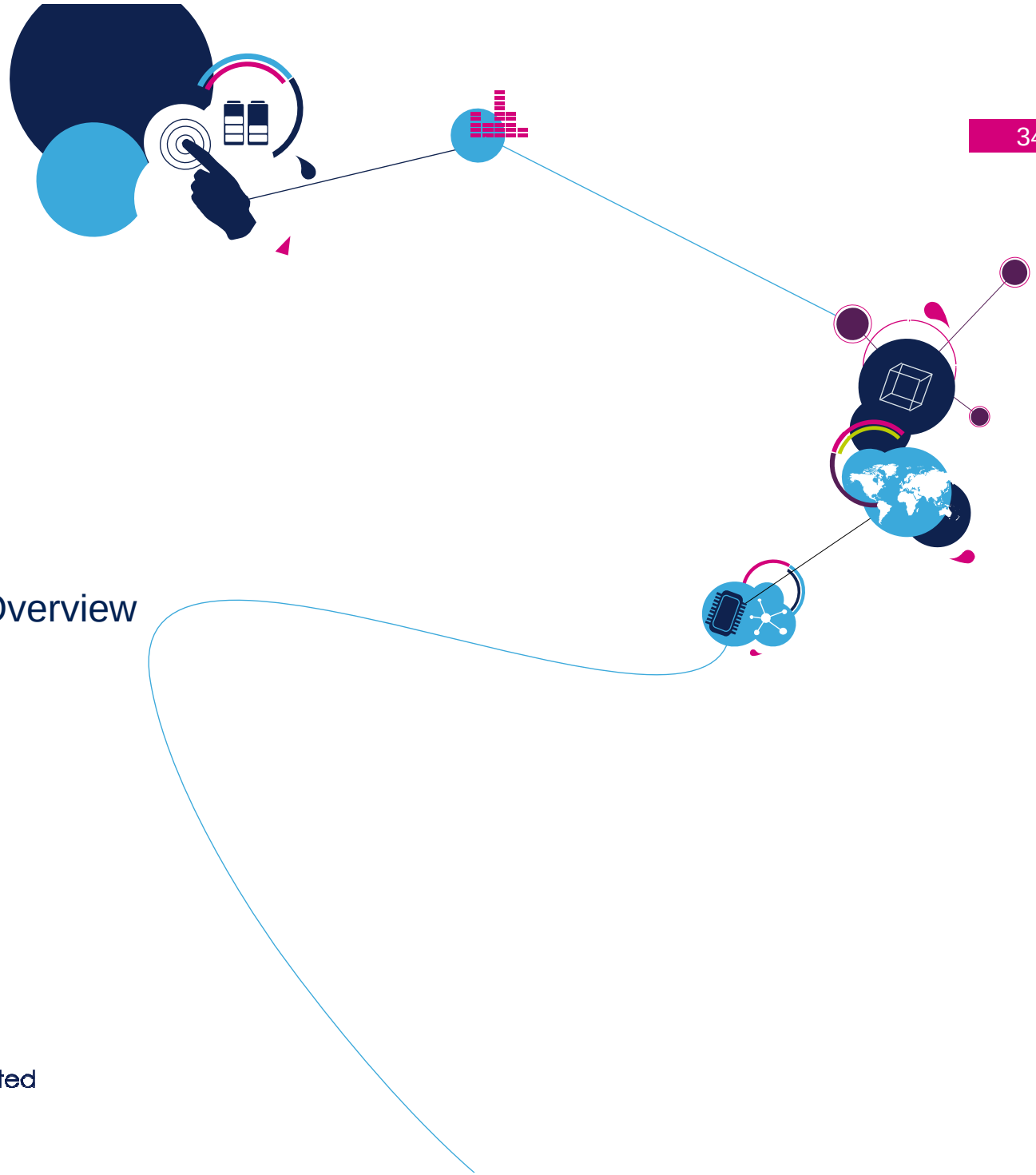


Available Commands on Host Interface

Group	Command	Code
Reset	BIO_ResetRequest	**3Ch**
	BIO_ResetConfirm	**3Dh**
MIB	MIB_WriteRequest	**08h**
	MIB_ReadRequest	**0Ch**
	MIB_EraseRequest	**10h**
	MIB_WriteConfirm	**09h**
	MIB_ReadConfirm	**0Dh**
	MIB_EraseConfirm	**11h**
Data	PHY_DataRequest	**24h**
	DL_DataRequest	**50h**
	SS_DataRequest	**54h**
	PHY_DataConfirm	**25h**
	DL_DataConfirm	**51h**
	SS_DataConfirm	**55h**
	PHY_DataIndication	**26h**
	DL_DataIndication	**53h**
	SS_DataIndication	**57h**

MIB Table

Index	Name	Description	Length [byte]	R/W/E
00h	Modem Configuration	Reception Mode, CRC	1	R/W
01h	PHY Configuration	Operating Frequencies, Reception channels, Modulation settings	14	R/W
02h	SS Key	Key to encrypt/decrypt SS frames	16	R/W
03h	Reserved	Reserved	1	R
04h	Last Data Indication	Information about last received data	4	R
05h	Last TX Confirm	Information about last transmitted data	5	R
06h	PHY_Data	Counters of PHY mode	10	R/E
07h	DL_Data	Counters of DL mode	12	R/E
08h	SS_Data	Counters of SS mode	10	R/E
09h	Host Interface Timeout	Max value for Host Interface Timeouts	3	R/W
0Ah	Firmware Version	Firmware version	4	R



ST7580

Reference Design Overview

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Reference Design – Main sections

- Supply voltages
- Interfaces to STM32
- Power Line Interface
  - Transmission filter
  - Reception filter
  - Line coupling
  - Zero Crossing coupling
- Layout guidelines

Supply voltages

- The **ST7580** device operate from two external supply voltages:
  - **VCC** (8 to 18 V) as the main power supply;
  - **VDDIO** (3.3 or 5 V) for the I/O and digital sections.

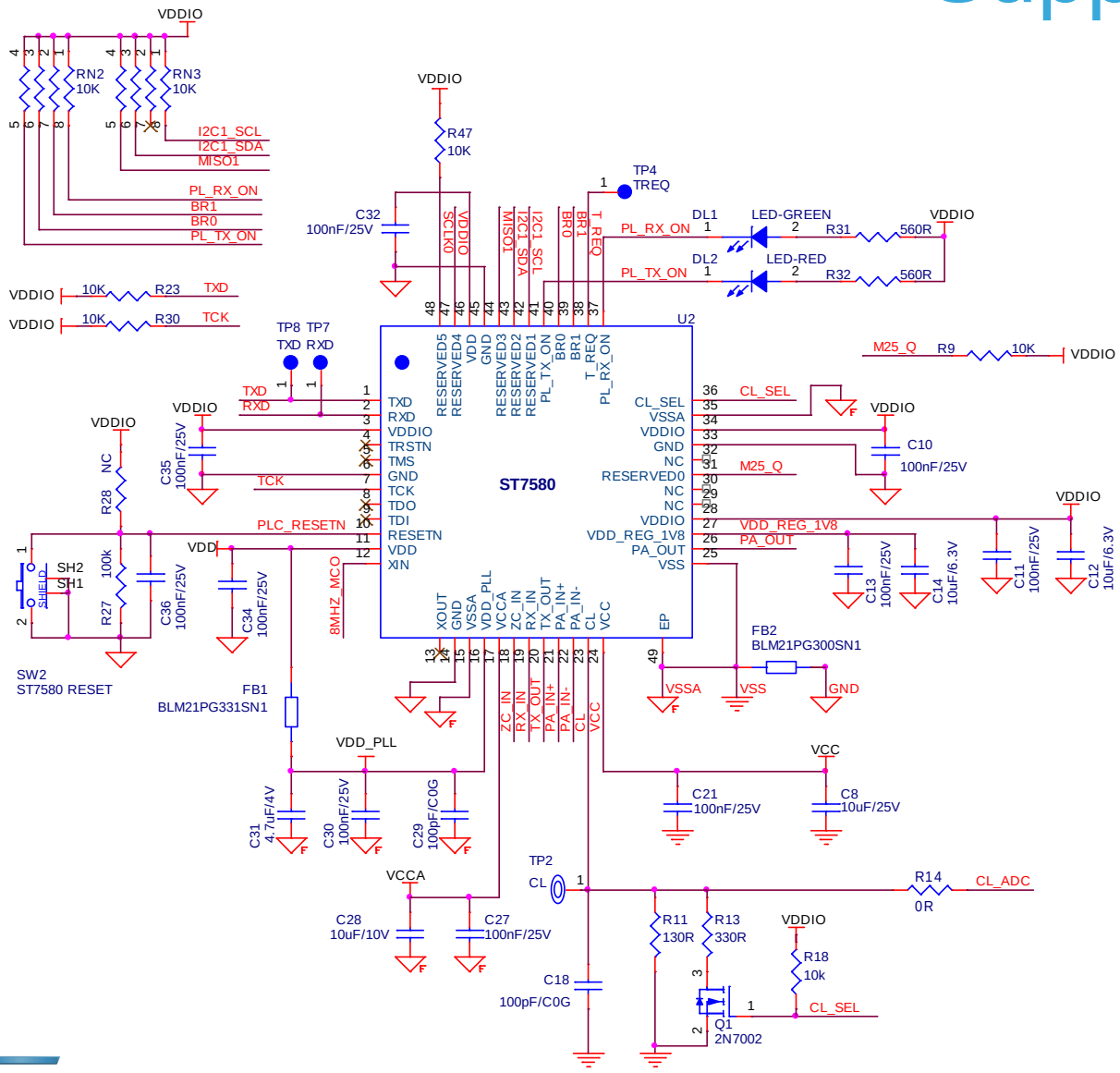
- Two internal linear regulators:
  - 5 V (used by the AFE), generated from VCC and connected to **VCCA** pin;
  - 1.8 V (DSP and microcontroller cores, digital blocks, PLL and oscillator), generated from VDDIO and connected to **VDD_REG_1V8** and **VDD** pin.

- VDD_PLL externally connected to VDD

- Internal regulators connected to VDD_REG_1V8 and VDDIO are externally accessible for filtering purpose only

➔ no loads allowed in the application circuit !

Supply scheme



- One 100nF capacitor close to <u>each</u> supply pin
- One 10uF capacitor per each supply voltage
- IMPORTANT:

  Pay attention to the correct supply-ground association!
- Ferrites used to block high-frequency disturbances

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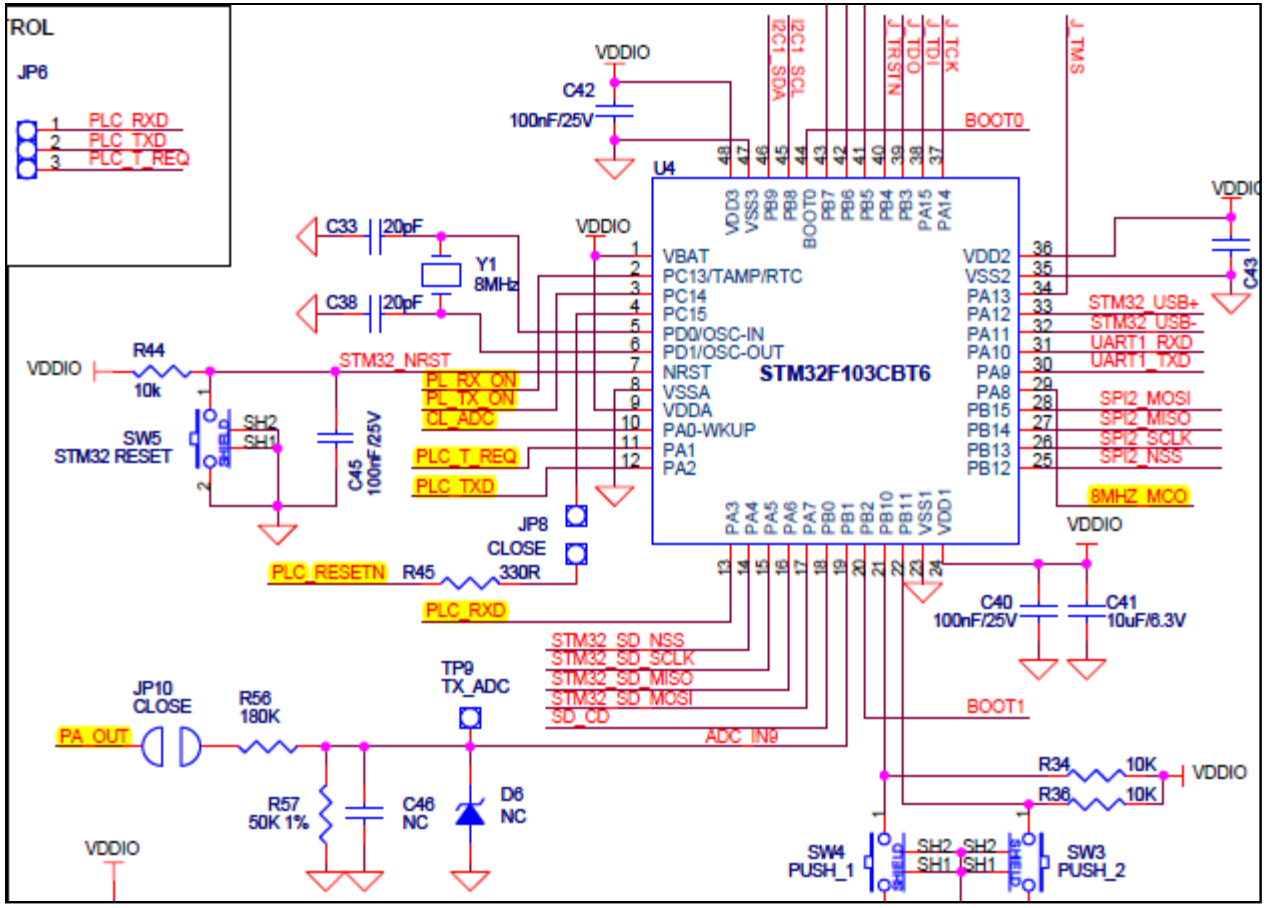
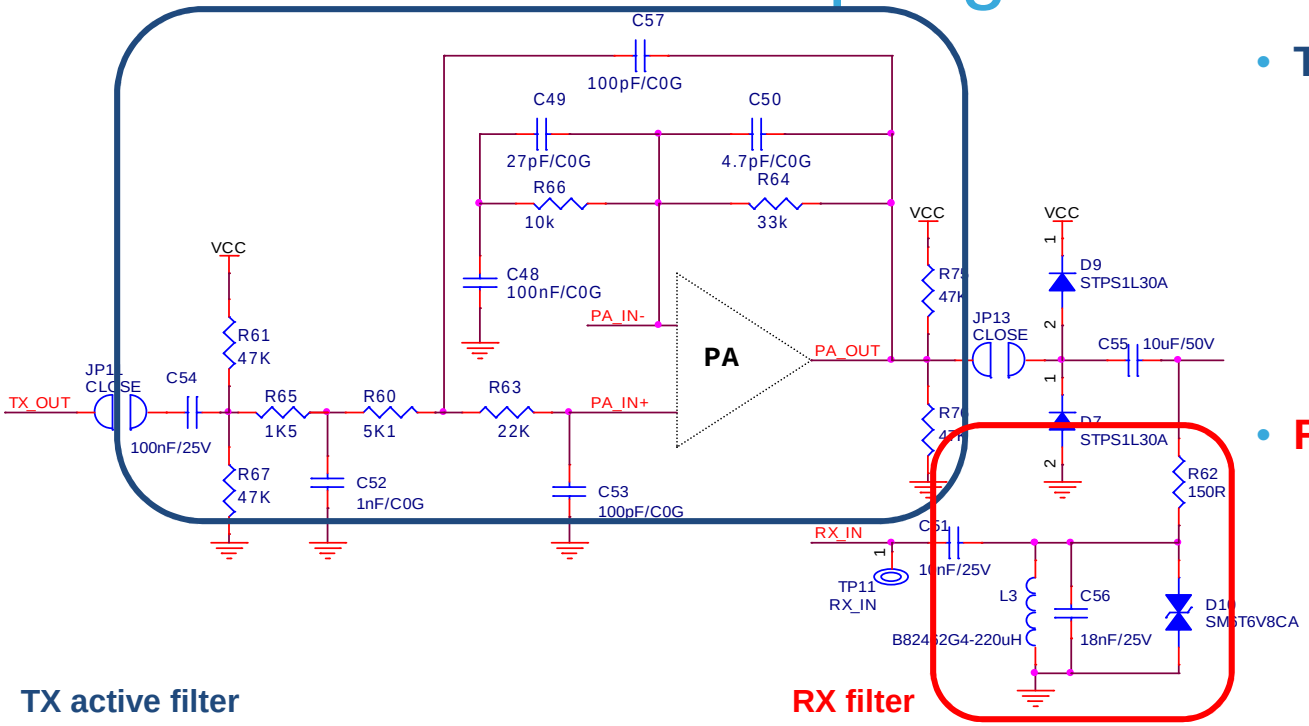
Interfaces to STM32



- UART
  - TXD
  - RXD
  - T_REQ
- RESETN
- PL_TX_ON and PL_RX_ON indications
- 8 MHz oscillator output
  - ➢ Sparing one 8 MHz quartz crystal
- PA_OUT and CL monitoring

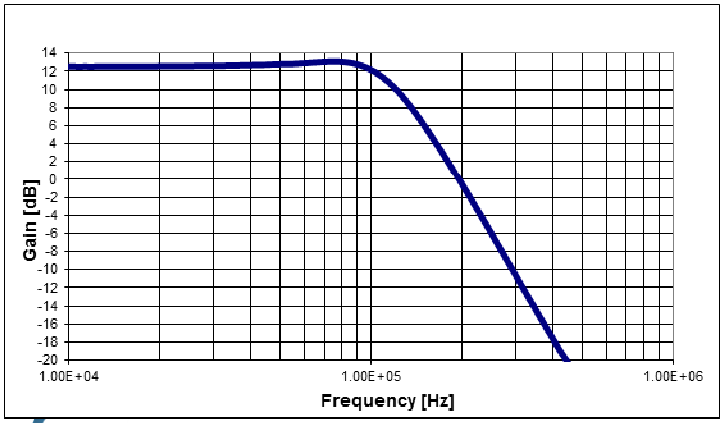
ST Confidential

Power Line coupling – TX and RX filters

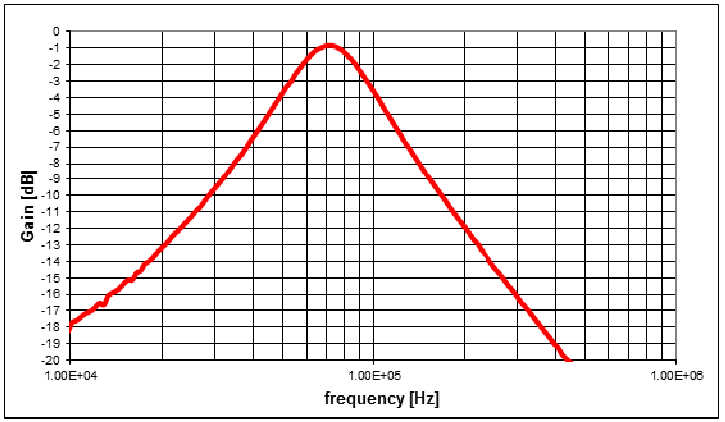


- **Transmission active filter**
  - 3° order low-pass filter to reduce conducted disturbances
  - Designed to transfer the whole signal BW with < 1 dB in-band ripple
- **Reception passive filter**
  - Simple RLC band-pass filter
  - Designed with Q and BW in accordance with the signal BW

TX active filter



RX filter



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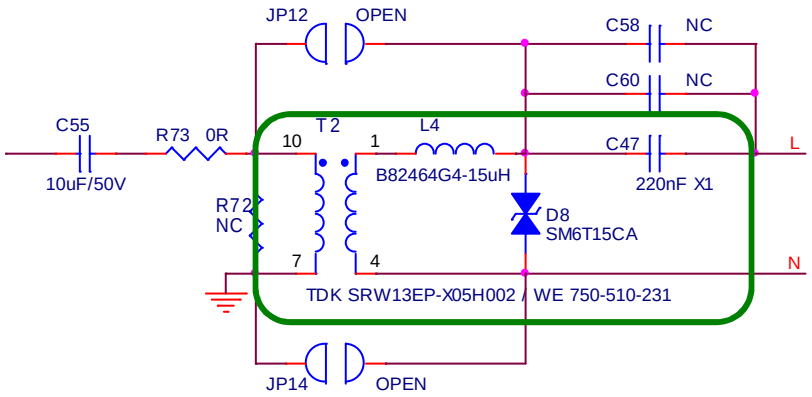
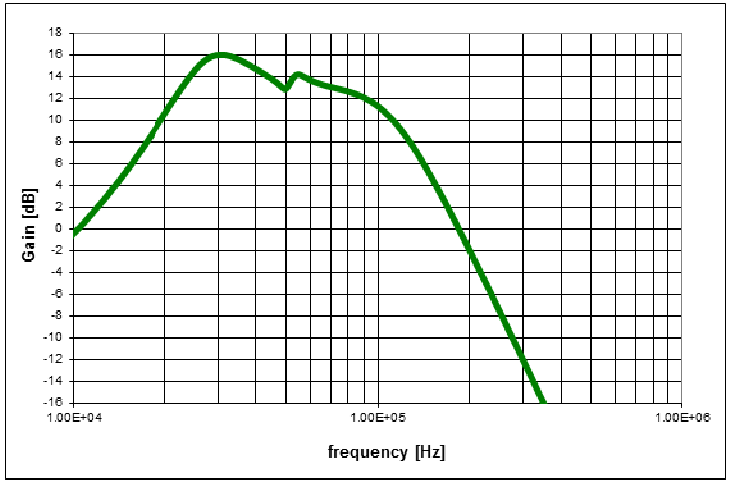
Power Line coupling: AC line coupling

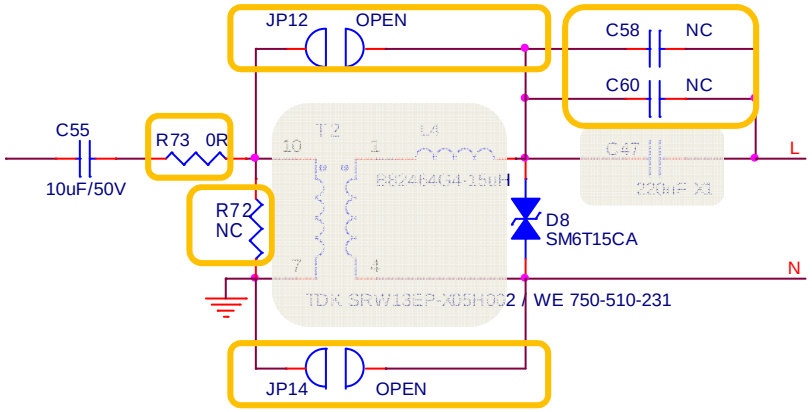


- **AC Line Coupling circuit**
  - Protection from AC voltage and high-energy disturbances from the line
  - Band-pass behavior for impedance adapting

TX active filter + AC Line coupling
Z_load = EN50065-1 LISN



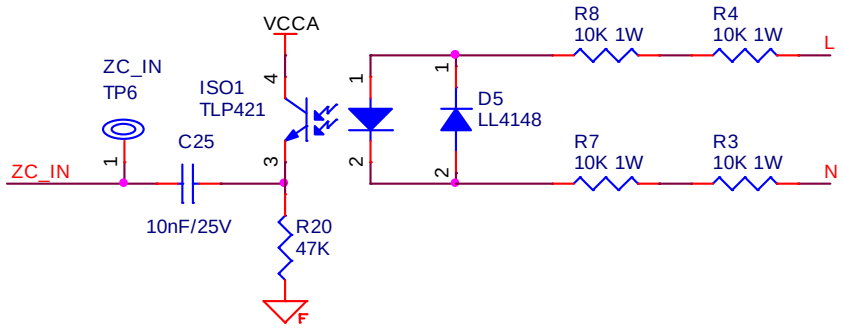
Power Line coupling – DC line coupling



- **Configurable coupling circuit for DC applications:**
  - PV in DC series configuration
  - PV in HV-DC parallel configuration
  - 12, 24 or 48 V DC bus
  - …

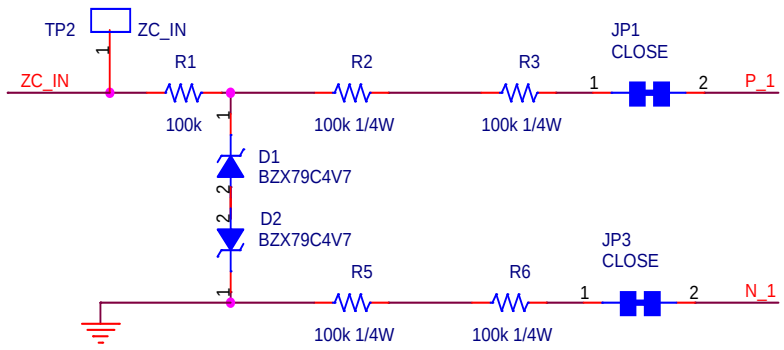
Power Line coupling - ZC coupling

- **Isolated Zero Crossing circuit**
  - Required for some solutions
  - Higher safety but higher consumption
  - Higher and more variable delay
  - Critical for application lifetime



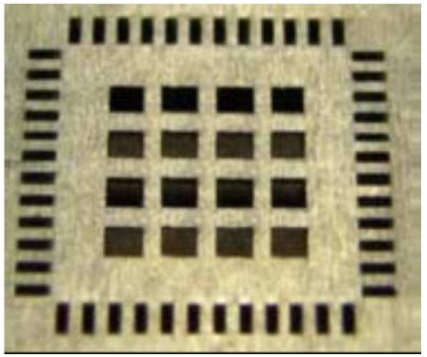
- **Alternative: Non-isolated Zero Crossing circuit**
  - Very simple and effective solution
  - Gives a stable delay between the mains zero crossing and the ZC_IN

    as low as 20 µs
  - Suitable for non-isolated design, such as metering applications



Layout guidelines - 1

- The Exposed pad has the purpose to guarantee very good thermal dissipation
  - VSSA plane below used as dissipating copper area
  - A number of open vias is required for cooling through air convection
- To avoid soldering issues about the Exposed pad, the solder paste quantity on the PCB top layer pad should be controlled
- A good solder paste distribution can be achieved with several small stencil openings:

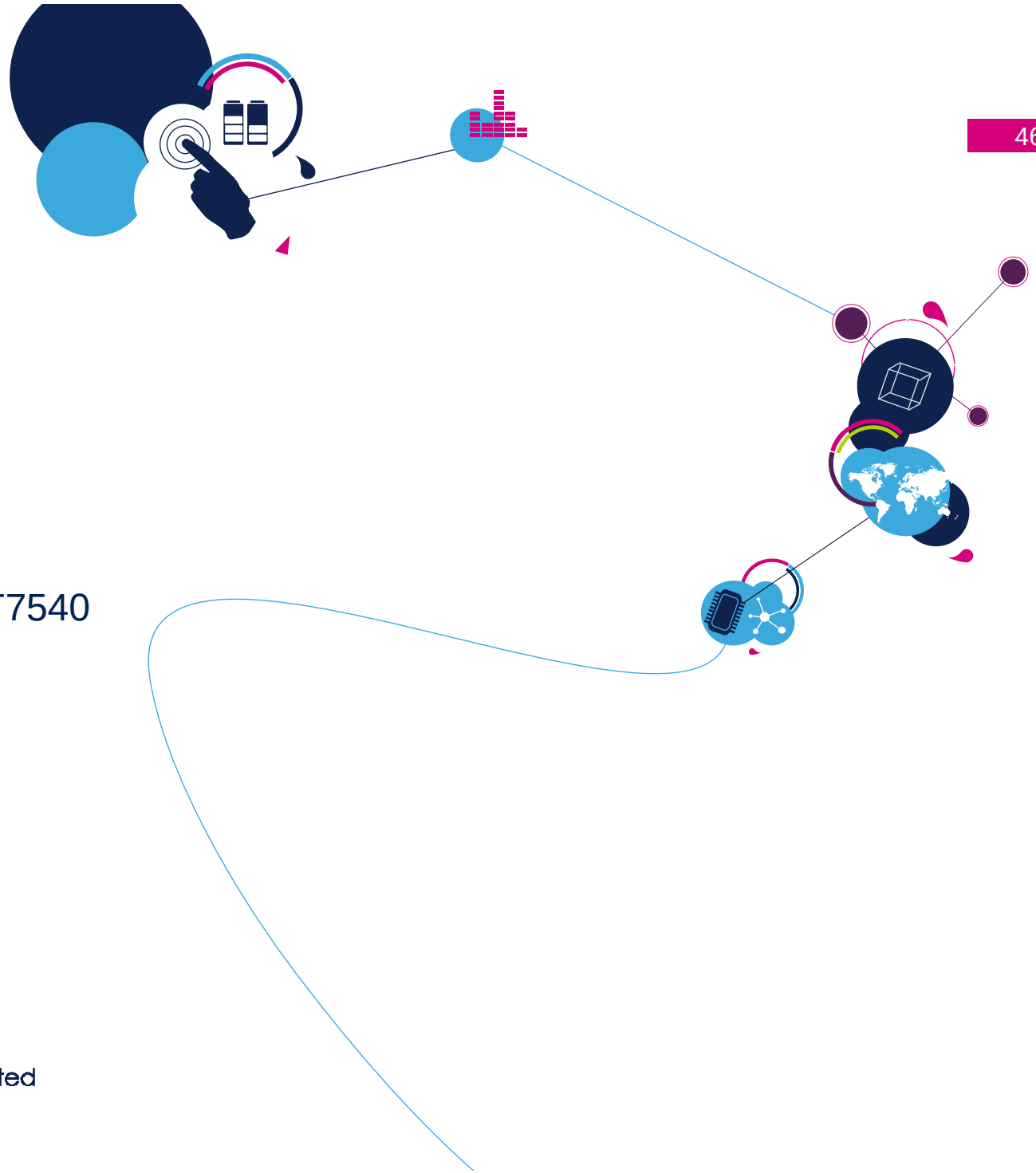


Layout guidelines - 2

- Extend the GND ground plane under the crystal
- Use large routes (≥ 12 mils) for VCC and PA_OUT (high-current lines)
- Keep the bypass capacitors close to each relative supply pin
- Keep supply and ground loops as short as possible to improve radiated disturbance immunity
- Keep good connection between top and bottom layers using several vias all around the PCB

ST7580 Status

- Product Webpage: here
  - Full documentation (DS, UM, AN) available
- Evaluation board available
  - Webpage: here
  - Documentation and SW available
- Mass production, ST7580 Lead Time : 18 wks



ST7580

Comparison with ST7540

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ST7540 vs. ST7580 (1)

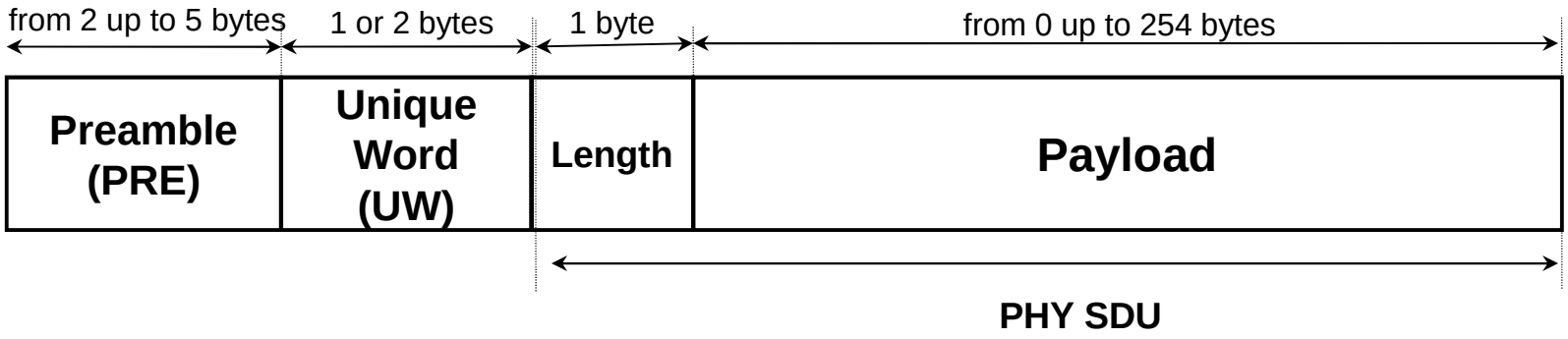
	ST7540	ST7580
Carrier frequency value	To be selected among 8 values	Any value (1 Hz resolution) between 9 kHz and 250 kHz
Channel reception	Single	Dual (2400 bps max)
PSK max. bitrate	Not supported	28800 bps
FSK max. bitrate	4800 bps	9600 bps
Powerline frame format	Selectable composition	Fixed composition
Powerline frame length	Selectable (*bits*)	Selectable (*bytes*)
Host interface	SPI	UART
Host interface dataflow	Bitstream	Frame syntax
Host interface max. bitrate	4800 bps	57600 bps
Host interface delays	Fixed	Depending on processing

ST7538 vs. ST7580 (2)

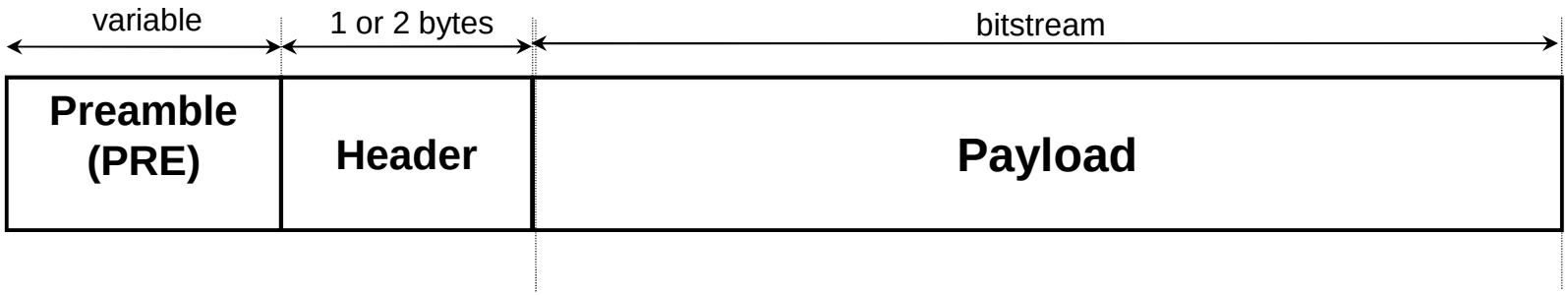
	ST7540	ST7580
Zero-Crossing synch	Optional	Optional
Embedded Power Amplifier	Up to 500 mArms – 8 Vpp single ended output	Up to 1Arms-14 Vpp single ended output with advanced thermal protection
Receiver sensitivity	54 dBµV	35 dBµV
Power supply	Single: • from 7.5 V to 12.5 V	Dual: • Analog part: from 8 V to 18 V • Digital part: 3.3 V (or 5 V)
Idle mode consumption	5 mA	• Analog part: 6 mA • Digital part: 40 mA
External clock frequency	16 MHz	8 MHz
Collision detection	BU (Band-in-Use) pin signaling communication frequency occupancy	Digital output pins (TX_ON, RX_ON) signaling effective powerline communication

Powerline frame format

- ST7580 frame (PHY layer):

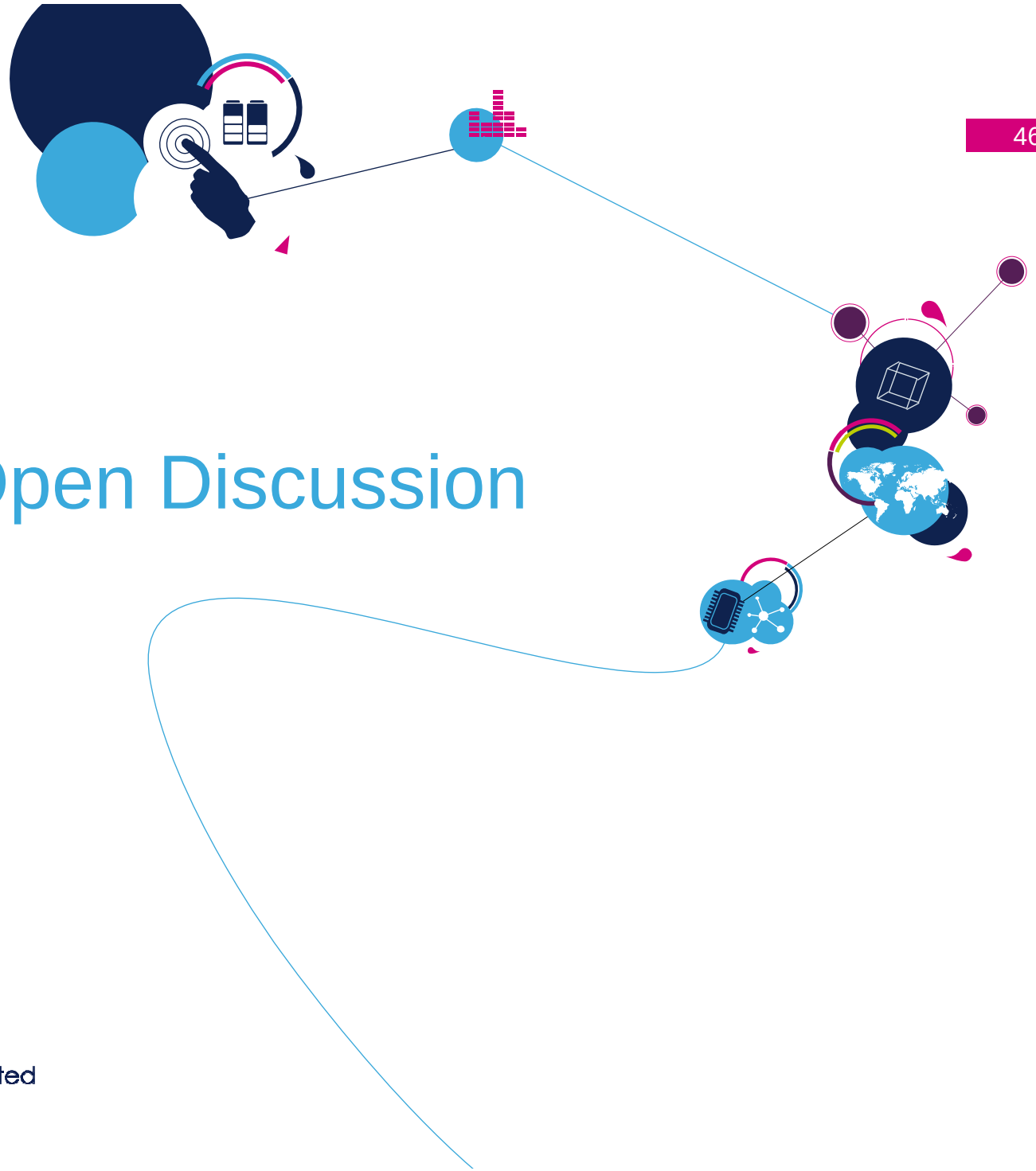


- ST7540 frame (Header recognition):



Powerline frame

	Direction	ST7540	ST7580
Preamble	TX	To be added from Host	Automatically built
	RX	Automatically handled	Automatically handled
Header/UW	TX	To be added from Host	Automatically built
	RX	Automatically handled	Automatically handled
Length	TX	To be added from Host	Automatically built
	RX	To be handled from Host	Automatically handled
Payload	TX/RX	Bit stream	Byte sort (254 max)
CRC	TX/RX	To be handled from Host	Eventually add DL layer
Bit order	TX/RX	Bit-to-bit (msb first)	Byte-to-byte (lsb first)
UW order	TX/RX	Msb	16-bit word, lsb first



ST7580 Open Discussion

Questions and answers

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