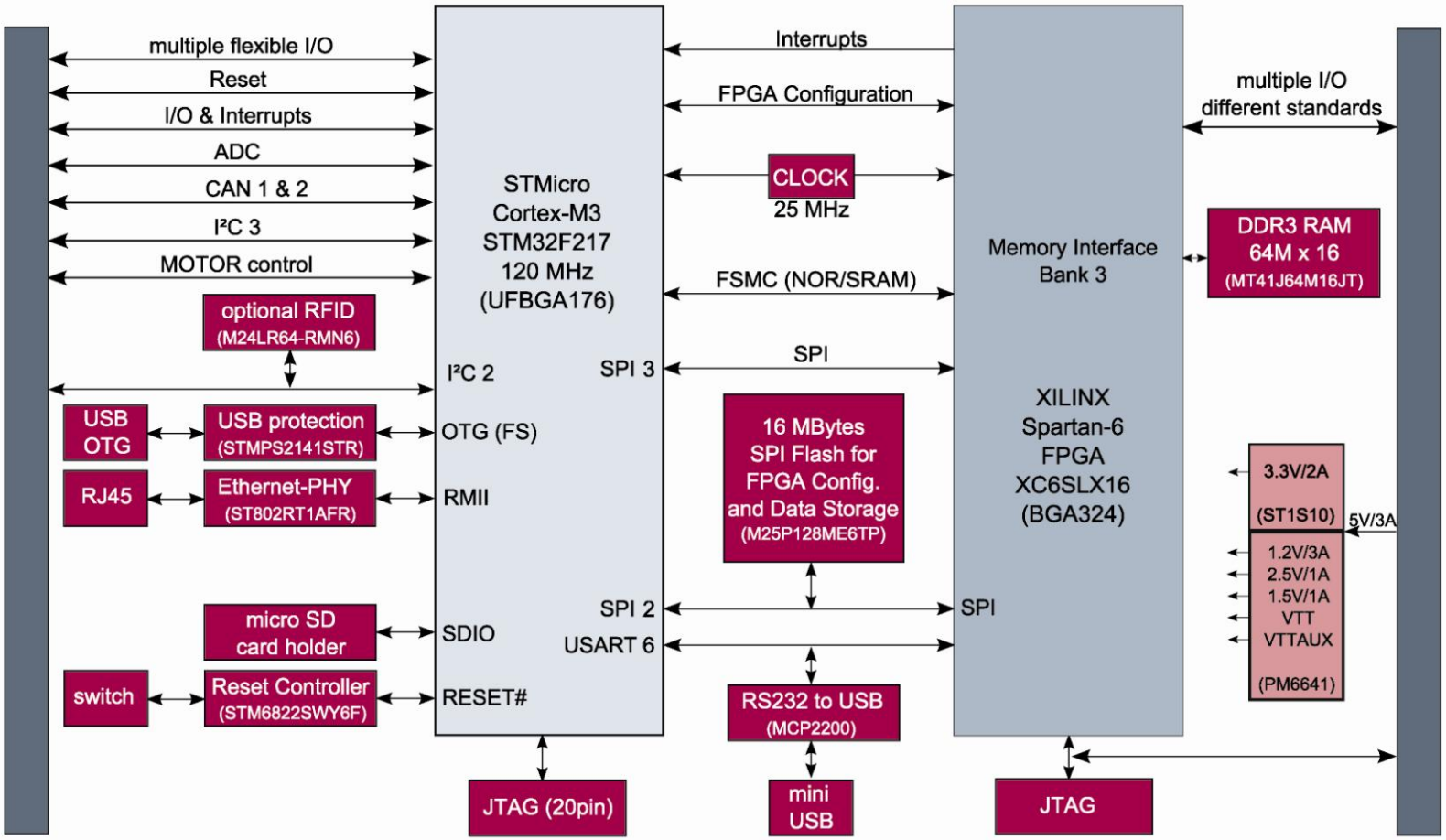
Xynergy – It really makes the difference!

STM32F217 meets XILINX **Spartan-6**

Why Xynergy?

- Very easy: There is a clear **S**ynergy achieved by combining the last generation of the most popular ARM Cortex-M3 implementation (STM32) and state-of-the art low cost FPGA technology (Spartan-6) coming from XILINX
- **S**ynergy ist too „general“ for a name … so just take the „**X**“ from XILINX and substitute it for the „**S**“ and you are done!
- Xynergy is the only board available on the market combining an ARM Cortex-M MCU together with a low cost FPGA

Xynergy Block Diagram



STM32F217
Outstanding Performance and Power

- **Cortex-M3 core's maximum processing performance with 0-wait state execution from Flash up to 120MHz**
- **150 DMips at 120MHz**
- **Adaptive Real Time (ART memory acceleratorTM)**
  - **128-bits wide Flash with Prefetch**
  - **Intelligent Branch management**
- **32-bit 7 layers AHB bus matrix interconnects**

- **188µA/MHz, 22.5mA at 120MHz**
  - **ST's 90nm process, 1.2V core**
  - **ST ART Accelerator™ reducing accesses to Flash**
- **Advanced low-power modes and features**
  - **Backup SRAM and RTC**
  - **<1µA with RTC on**
  - **<1uA with 4-Kbyte backed up SRAM**
  - **<2uA with both on**
- **VDD min down to 1.65V**

STM32F217
Peripherals and integration

- High Speed USB OTG
- Audio PLL, I²S and USB synchronization
- Camera interface, 8- to 14-bit parallel, up to 48Mbyte/s at 48MHz
- Flexible static memory interface up to 60 MHz
- Crypto / Hash processor: 3DES, AES256/SHA-1, MD5, HMAC
- 3 SPIs running at up to 30Mbit/s,
- 6 USARTs running at up to 7.5Mbit/s
- 3x 12-bit ADC, 2 MSPS, up to 6MSPS in interleaved mode
- True random-number generator
- Fast GPIO (60 MHz toggling)

- 1-MByte Flash
- 128-Kbyte SRAM
- 4-Kbytes back up SRAM: used as EEPROM to save application state, calibration data,
- 528 bytes of OTP memory to store critical user data such as Ethernet MAC addresses or cryptographic keys.

Features Spartan-6 XC6SLX16

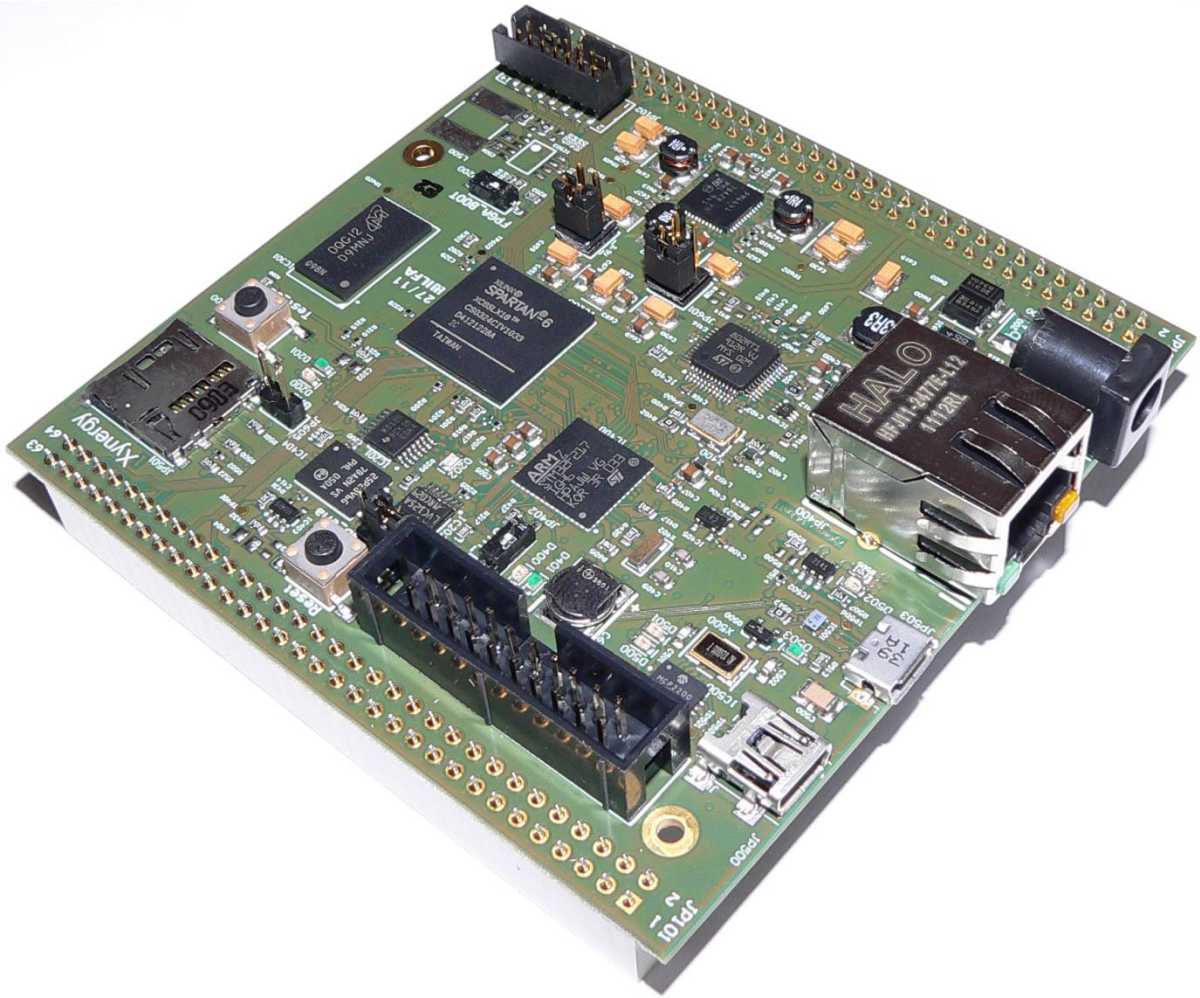
- **14.579 Logic Cells (6 Bit LUT, 2 Flip-Flops)**
- **576Kb Block RAM organized in 32 18Kb Blocks**
- **2** Clock Management Tiles (CMTs), each containing 2 DCMs and 1 PLL
- **Maximum 232 Single-Ended or 116 Differential User I/Os**
- **32 DSP48A1 Slices: Multiply Accumulate (MAC) and many more arithmetic functions**
- **2** DDR2 / DDR3 SDRAM **Memory Controller Blocks**

Target Applications

- Evaluation of mixed Microcontroller / FPGA designs
- General purpose industrial applications using Ethernet / USB / CAN / SPI / I^2C
- General purpose pre-, post- and co-processing with FPGA, i.e. digital filtering , advanced crypto, video etc.
- Implementation of industrial Ethernet IP in FPGA
- Motorcontrol with FPGA acceleration of closed loop algorithms
- Access to DDR3-Memory for the Microcontroller
- Custom interfaces

Packing List

The Board…



Packing List cont.

… 5V / 3A wall power supply with all potentially needed adapters for all relevant countries …

Packing List cont.

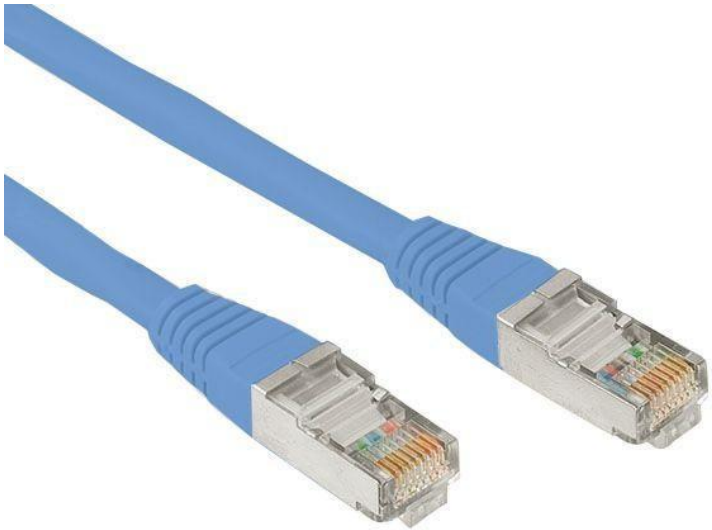
… ST-Link/V2 low cost in-curcuit debugger for STM32 …

Packing List cont.

… USB A / mini B cable for Virtual COM Port Connection …

Packing List cont.

… CAT-5(e) cable for Ethernet connection …



Packing List cont.

… 2-page Flyer with a very short introduction, then referencing the Xynergy Homepage for Download of all further documentation, software etc. : http://www.silica.com/xynergy

SILICA
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SILICA | The Engineers of Distribution.

Silica Xynergy Board

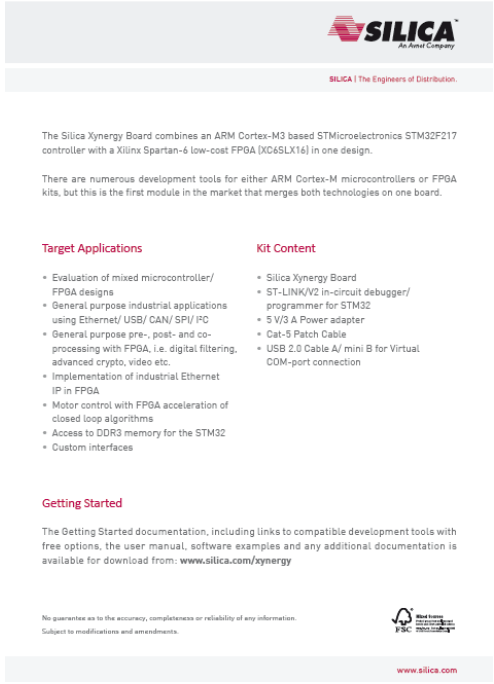
STM32 Meets Spartan-6

XILINX.

Ordering Information:
XYZBAYXYNERGY € 199.-

For further details, please visit: www.silica.com/xynergy

www.silica.com



SILICA
An Avnet Company

SILICA | The Engineers of Distribution.

The Silica Xynergy Board combines an ARM Cortex-M3 based STMicroelectronics STM32F217 controller with a Xilinx Spartan-6 low-cost FPGA (XC6SLX16) in one design.

There are numerous development tools for either ARM Cortex-M microcontrollers or FPGA kits, but this is the first module in the market that merges both technologies on one board.

Target Applications

- Evaluation of mixed microcontroller/ FPGA designs
- General purpose industrial applications using Ethernet/ USB/ CAN/ SPI/ I²C
- General purpose pre-, post- and co-processing with FPGA, i.e. digital filtering, advanced crypto, video etc.
- Implementation of industrial Ethernet IP in FPGA
- Motor control with FPGA acceleration of closed loop algorithms
- Access to DDR3 memory for the STM32
- Custom interfaces

Kit Content

- Silica Xynergy Board
- ST-LINK/V2 in-circuit debugger/ programmer for STM32
- 5 V/3 A Power adapter
- Cat-5 Patch Cable
- USB 2.0 Cable A/ mini B for Virtual COM-port connection

Getting Started

The Getting Started documentation, including links to compatible development tools with free options, the user manual, software examples and any additional documentation is available for download from: **www.silica.com/xynergy**

No guarantee as to the accuracy, completeness or reliability of any information.
Subject to modifications and amendments.

www.silica.com

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Silica.com » Xynergy Software Download

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Silica Xynergy Board Documentation

Find below the necessary material to get started with your Silica Xynergy Board:

- Xynergy User Guide (pdf, 1.6 MB)
- Schematic & Silkscreen (zip, 1.8 MB)

Software Examples

- Getting_Started (pdf, 0.3 MB)
- Preloaded_Software_on_Xynergy (pdf, 0.6 MB)
- Microchip MCP2200 Virtual COM-Port Driver and Utilities

STM32:

- Xynergy-Networking (WEB-Server) (zip, 16.4 MB)
- Xynergy-Resource-Examples (zip, 49.1 MB)

Xilinx:

- FSMC-Interface for Spartan-6 (zip, 2.4 MB)
- DDR3-Memorytest with MicroBlaze (zip, 20.3 MB)

Xynergy Testing:

- Xynergy_Board_Test (pdf, 0.7 MB)
- Xynergy_Testing (zip, 0.6 MB)

Gerber Data

To receive the Gerber Data, please, send an email to knut.sennewald@silica.com with a brief description of your application.

SW: What is done so far

- Header / Configuration files for Xynergy for use with ST Standard Libraries which contain test routines for peripherals
- Test SW for Ethernet (Webserver with SILICA branding)
- DDR3 Test SW on FPGA based on MicroBlaze with UART output (Terminal)
- SD-Card test SW
- UART output for test of RS232 to USB bridge
- Test Design on FPGA for FSMC connection with STM32
- Demo with ST MEMS-Device (Acceleration) / Servo

Keil and IAR -> Integration!

- **Keil** has already included **Xynergy** in their Development Suites for ARM!
- **IAR** is in preperation to support **Xynergy** very soon

KEIL™ Tools by ARM

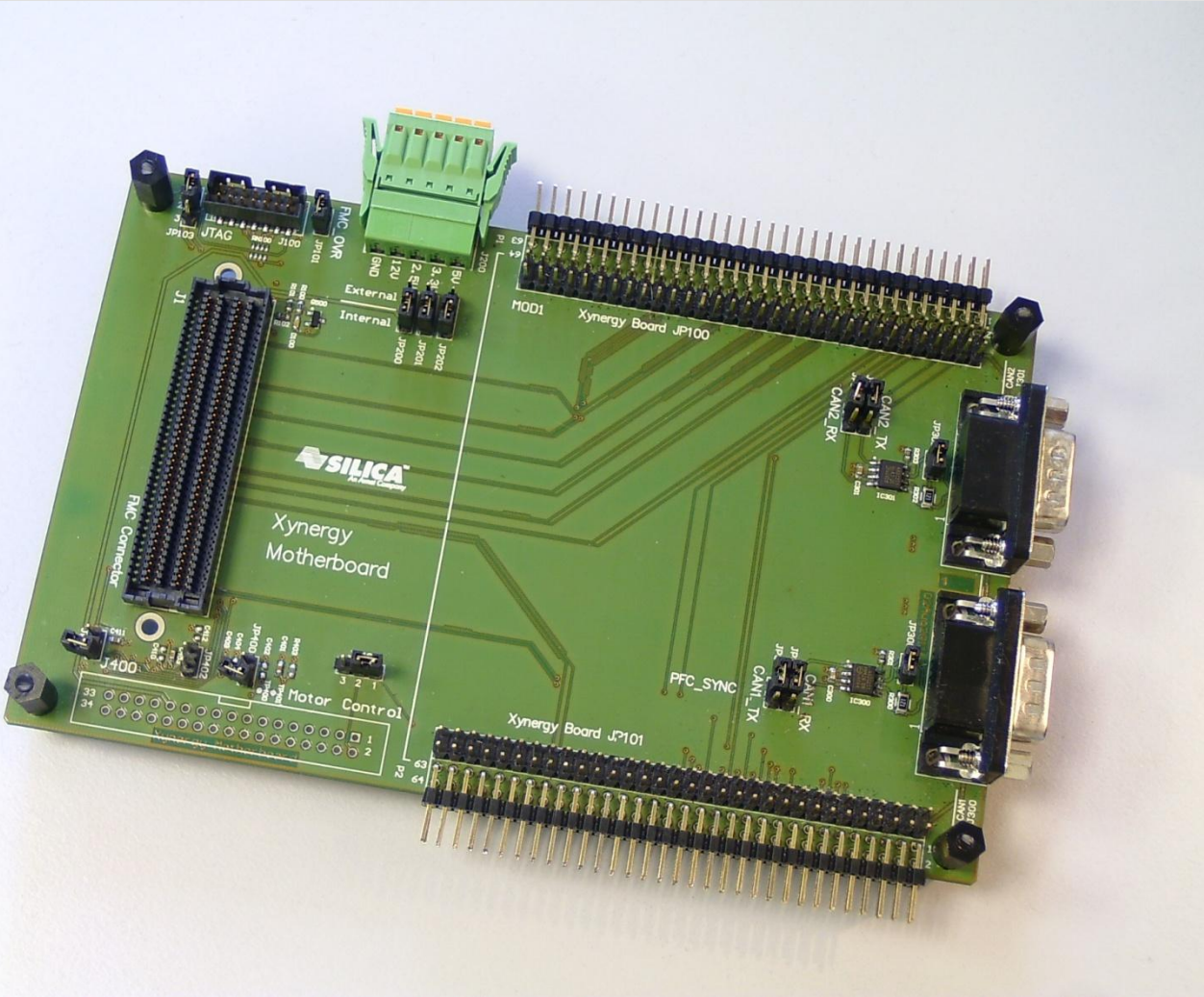
IAR Embedded Workbench™ IAR SYSTEMS

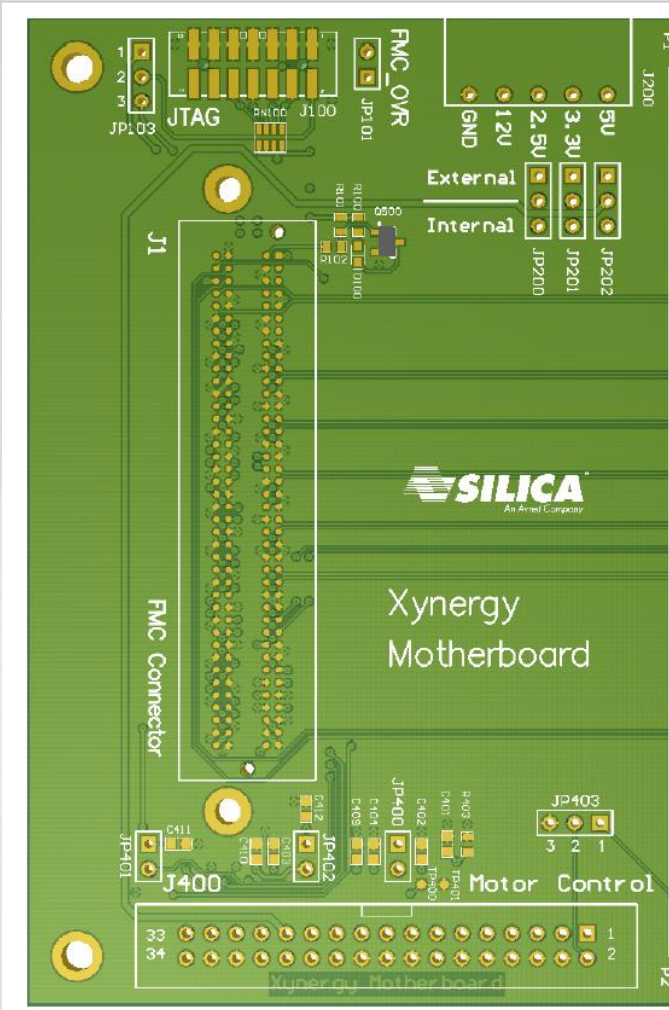
Next steps -> Motherboard!

Motherboard with:

- FMC connector (FPGA Mezzanine Connector)
- 2 CAN Tranceivers with two D-Sub 9
- Connector to STM Motorcontrolboards
- Connector block for additional FMC power supply (12V) if needed
- Replication of expansion connectors to standard 2,54mm pin headers

Next steps cont. / Motherboard





FMC Modules

Find a long list of available FMC modules on:

http://www.xilinx.com/products/boards_kits/fmc.htm

- **AD/DA Conversion**
- **Serial Connectivity**
- **Image Processing**
- **Interface Peripherals/Debug**

Example: AVNET IndustrialNetworking FMC Module

Cortex-M4 Edition (planned)

- „**Cortex-M4 Edition**“ with **pin compatible** STM32**F417**IGH6

  That is extensive re-use of the design for STM32F4x with Cortex-M4

→ **Excellent option for designers who need additional performance in terms of f_{max} (168 MHz vs 120 MHz), FPU and DSP instruction set!**

How to order, Price, Availability

- **Part number is *XYZBAYXYNERGY***
- **Price: *€199,-***
- **Available from SILICA *stock***

Demo

- **Live Demonstration of Webserver Design and DDR3-Memory Test including test output via Virtual COM-Port (USB)**
- **Xynergy is delivered pre-loaded with this design !**