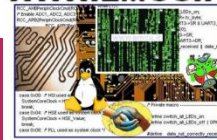


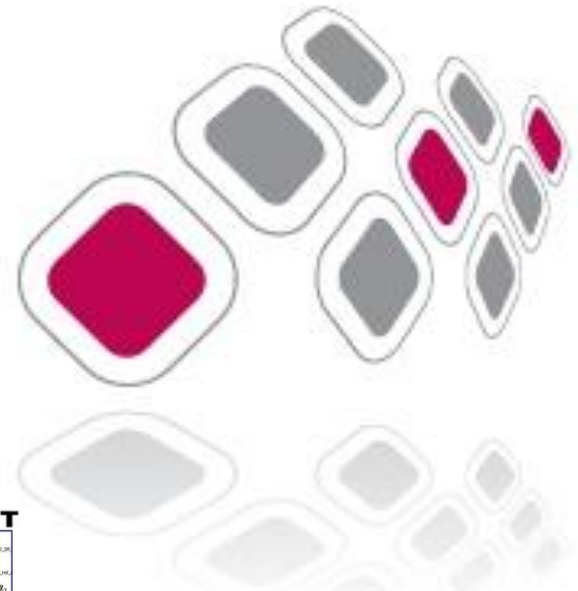


ST Microelectronics

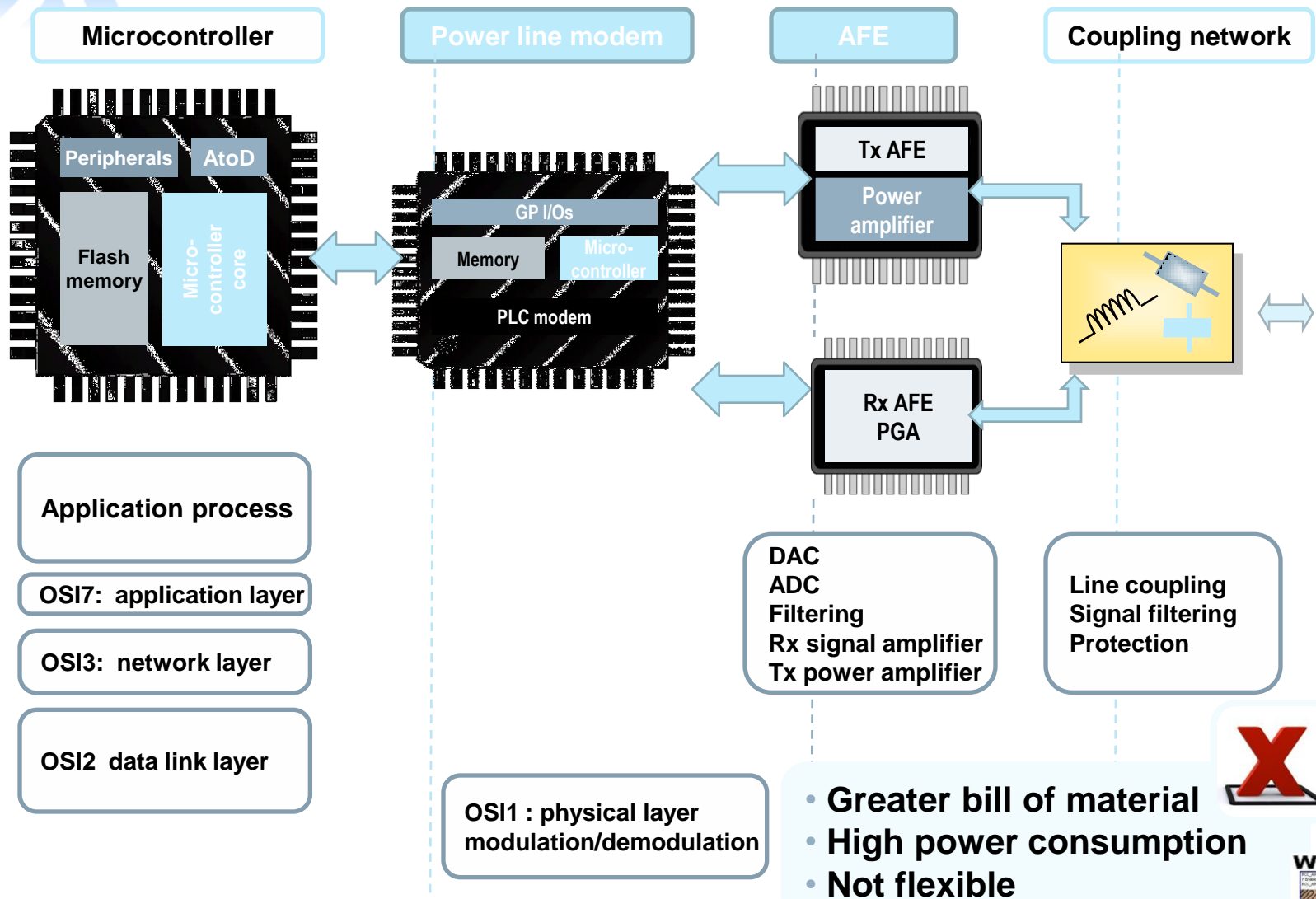




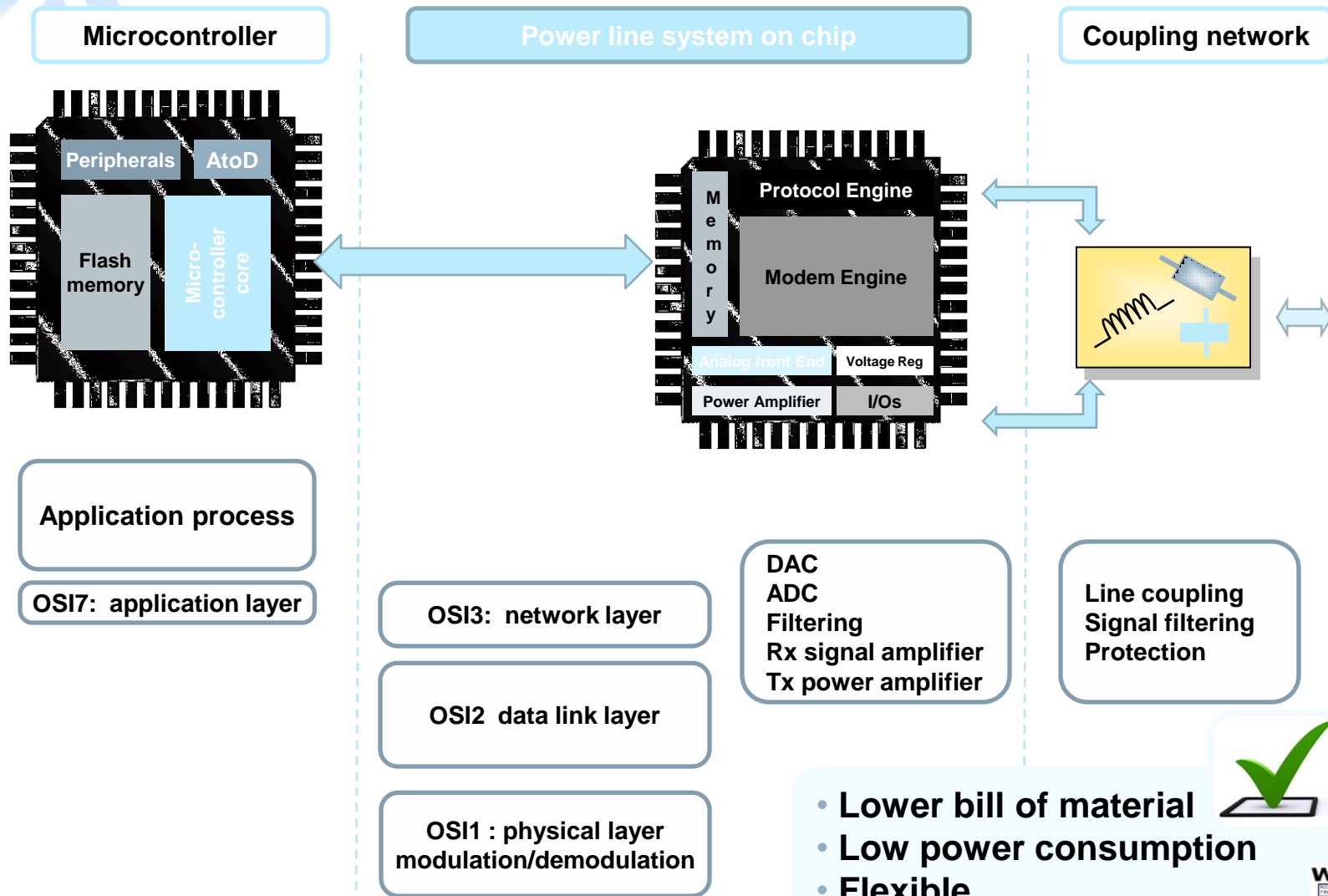
ST's Smart Grid Solutions: Power Line Communication and Metering



PLC node partitioning: from typical approach ...



PLC node partitioning: ...to STarGRID SoC approach

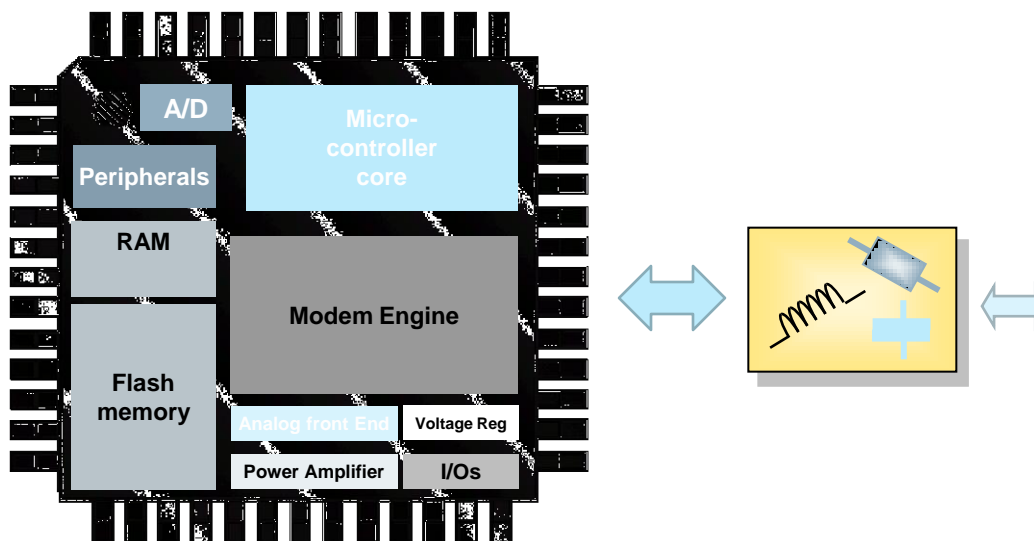




Towards full SoC Evolution

Full application system on chip

Coupling network

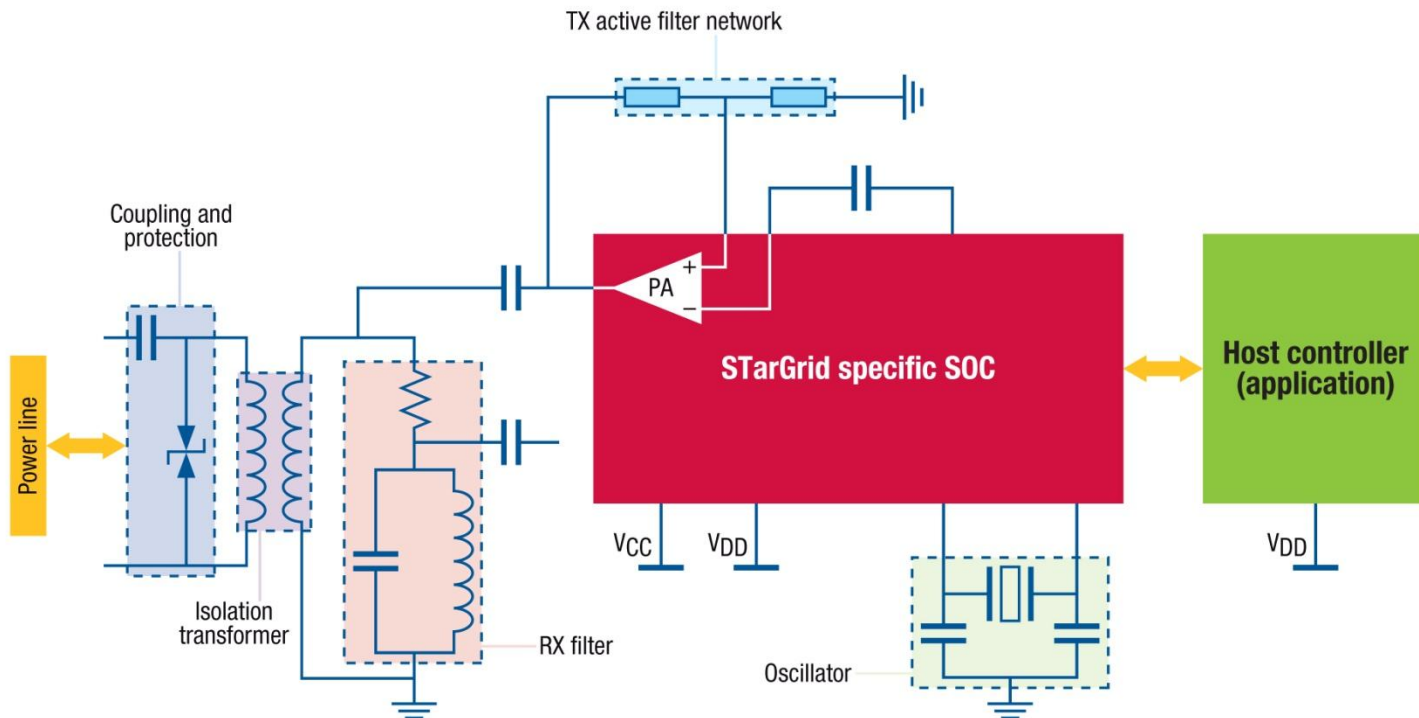


....towards full system integration



STarGRID

based PLC application diagram



**Most compact, lowest BOM
PLC node on the market**



Suggested ST PLM versus CENELEC PLC Frequency Bands & Use

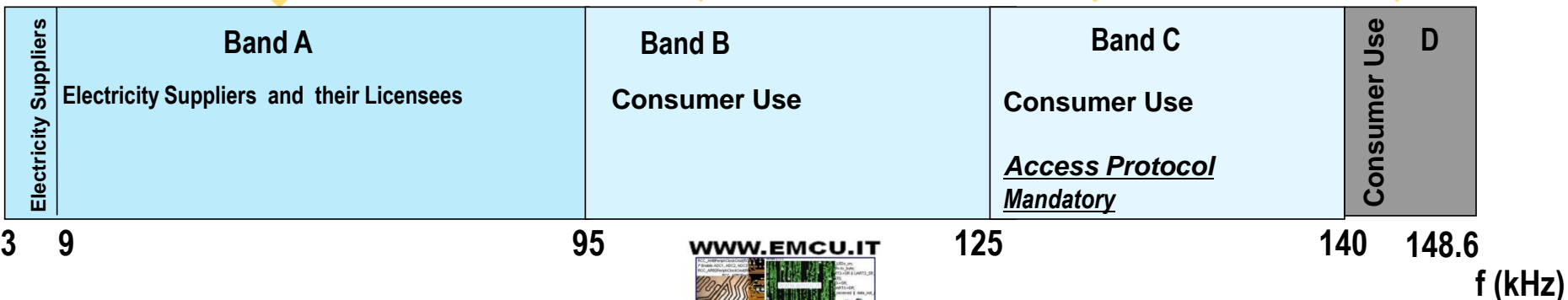
ST7580 (meters&more), ST7590
(PRIME)
ST7570 (IEC 61334-5-1)



ST7580



ST7540

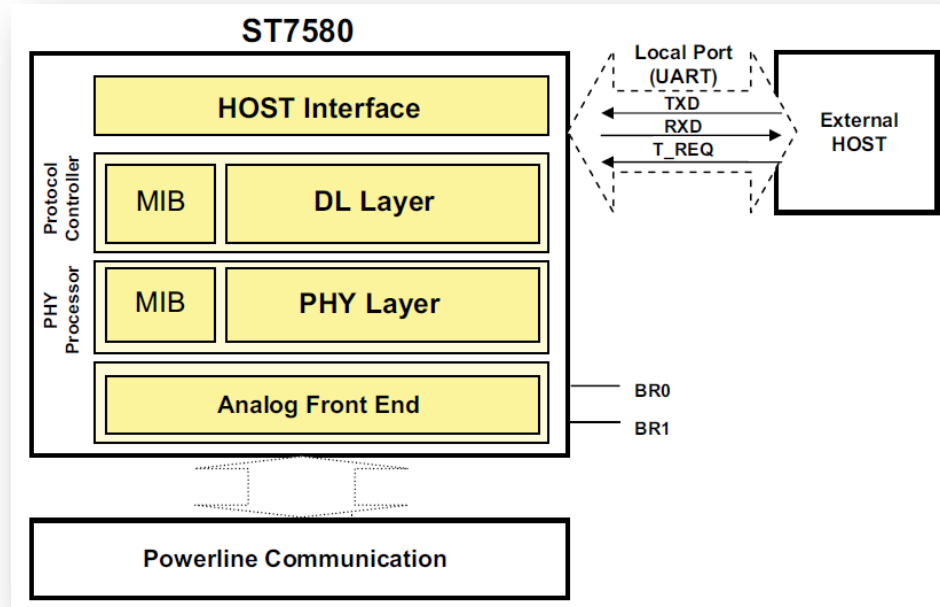


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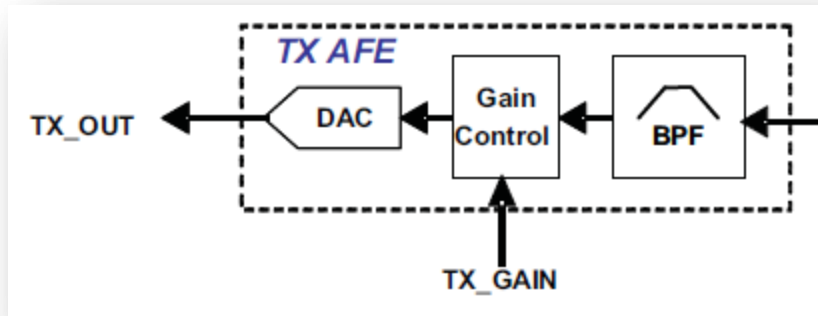
ST7580: Functional Overview



- Complete physical layer (PHY): a BFSK and a multi-mode PSK modulation with channel quality estimation and dual channel receiving mode
- Basic Data link layer (DL) services
- AES-128 based authentication
- A UART host interface is available for communication with an external host

The diagram illustrates the RX AFE (Receiver Front-End) block. It is enclosed in a dashed box and contains three main processing blocks: PGA (Programmable Gain Amplifier), ADC (Analog-to-Digital Converter), and BPF (Band-Pass Filter). The signal flow starts with an input signal labeled **RX_IN** entering the PGA block. The output of the PGA is fed into the ADC block. The output of the ADC is then fed into the BPF block. The final output of the BPF is shown as a signal exiting the dashed box. A feedback loop is also indicated, connecting the output of the BPF back to the input of the PGA.

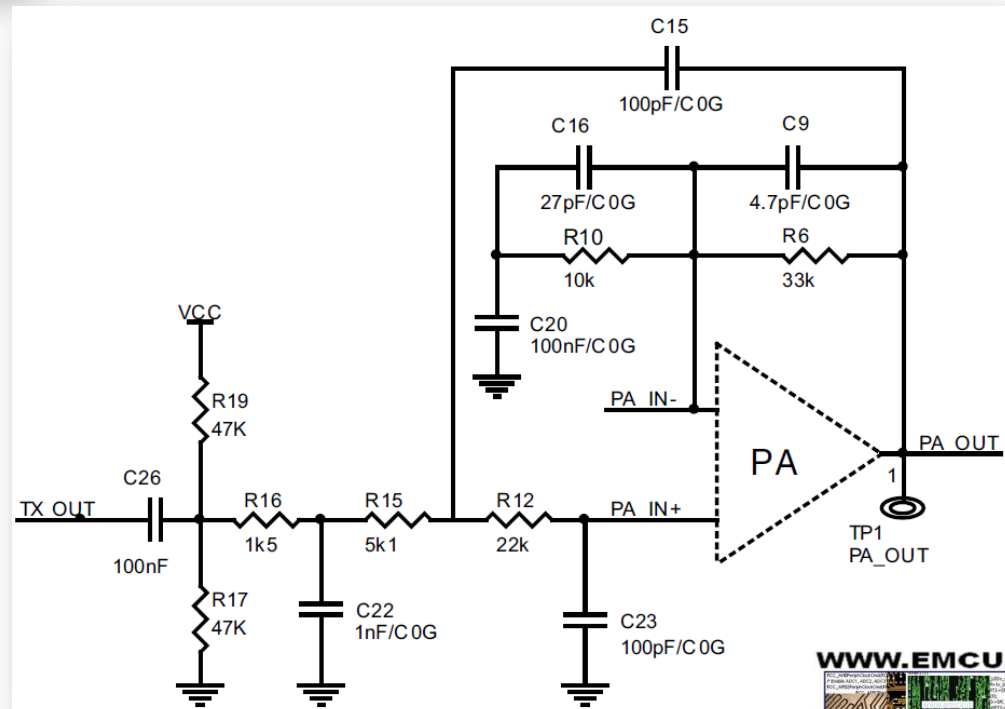
PGA code	PGA gain (typ.) [dB]	RX_IN max. range [V p-p]
0	-18	V(RX_IN) MAX
1	-12	8
2	-6	4
3	0	2
4	6	1
5	12	0.500
6	18	0.250
7	24	0.125
8	30	0.0625



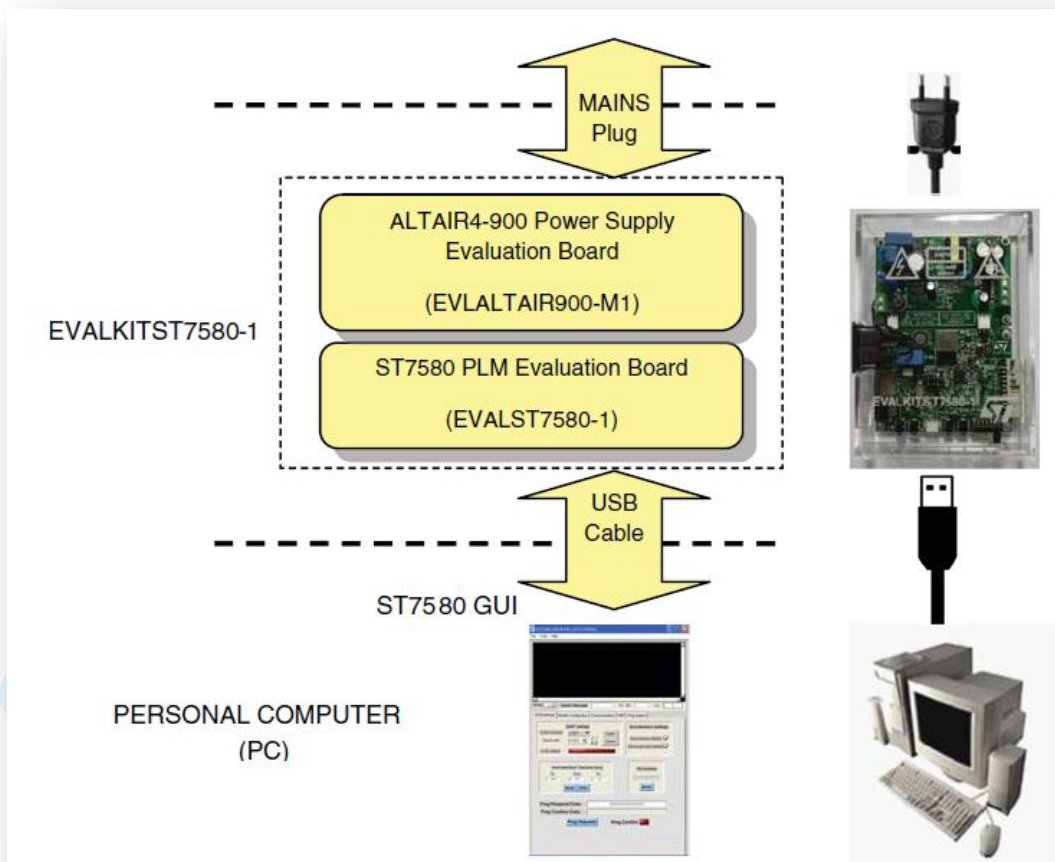
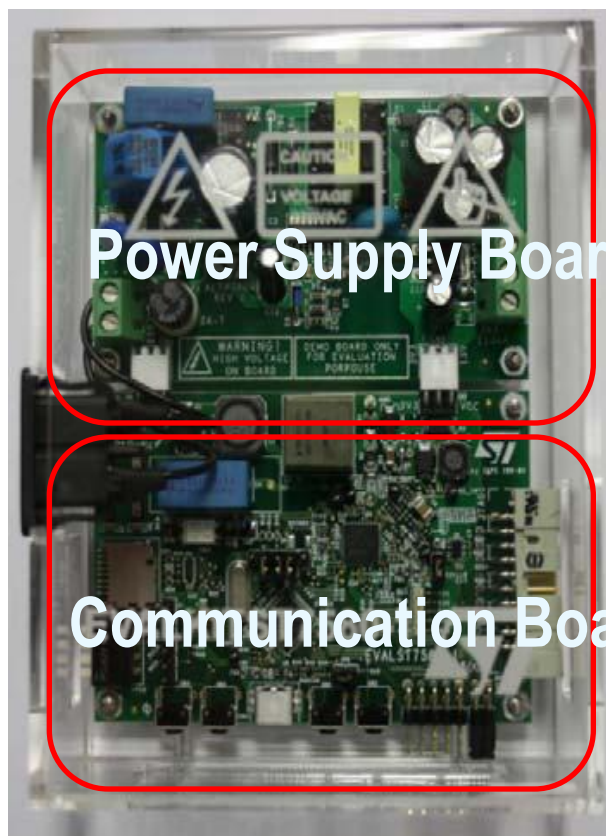
A gain control block before the DAC gives the possibility to scale down the output signal to match the desired transmission level.

Current capability power amplifier allows to drive even very low impedance points of the network

All pins of the power amplifier are accessible, making it possible to build an active filter network to increase the linearity of the output signal.

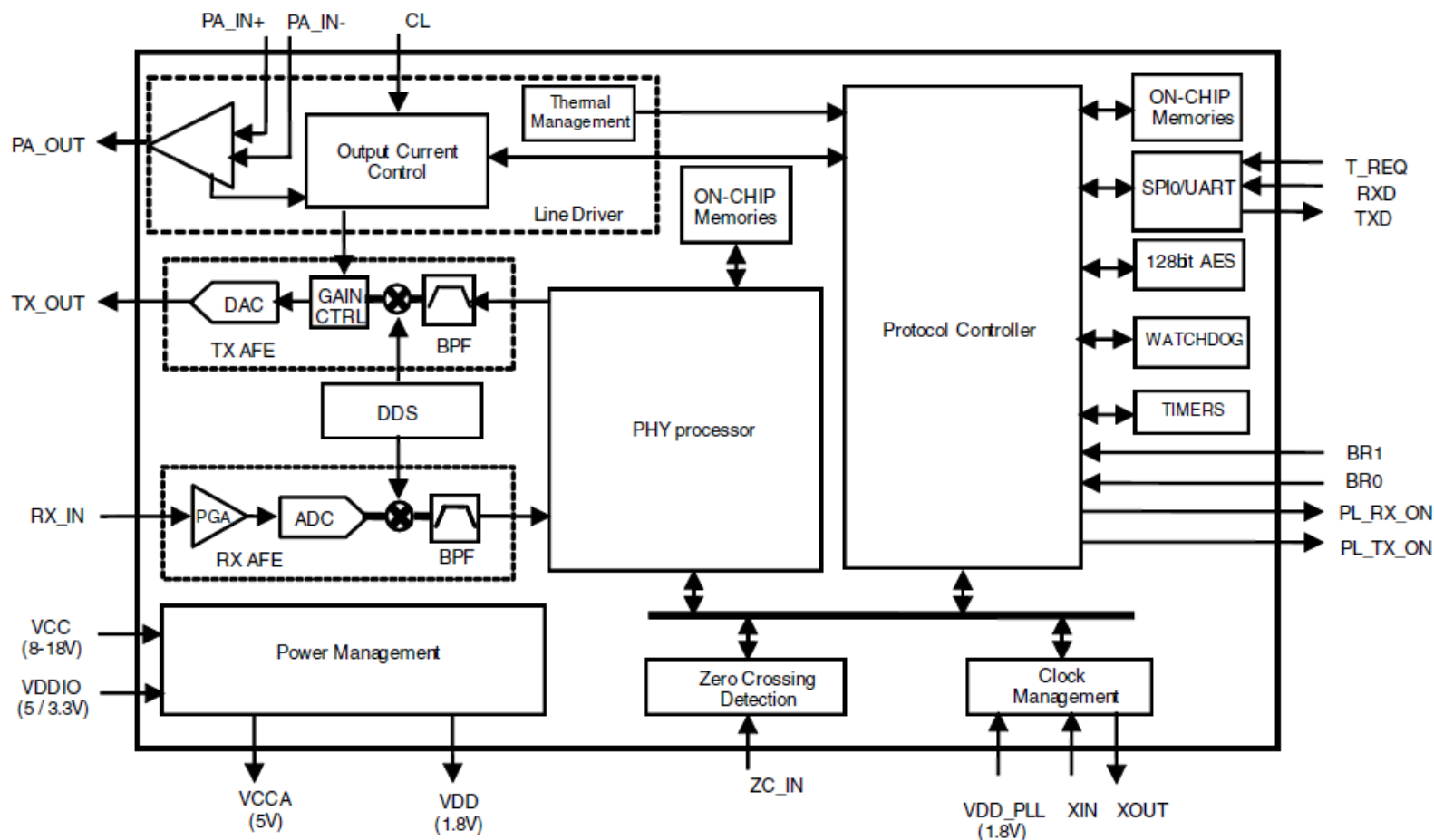


- ▶ Turn key evaluation boards available for ST7540 (EVALST7540-2) and STarGRID SoC ICs (EVALST7570KIT-1, EVALKITST7580-1, EVALST7590-1)
- ▶ Example for ST7580: PLC Evaluation Node with Power Supply Board and embedded STM32 MCU for application prototyping



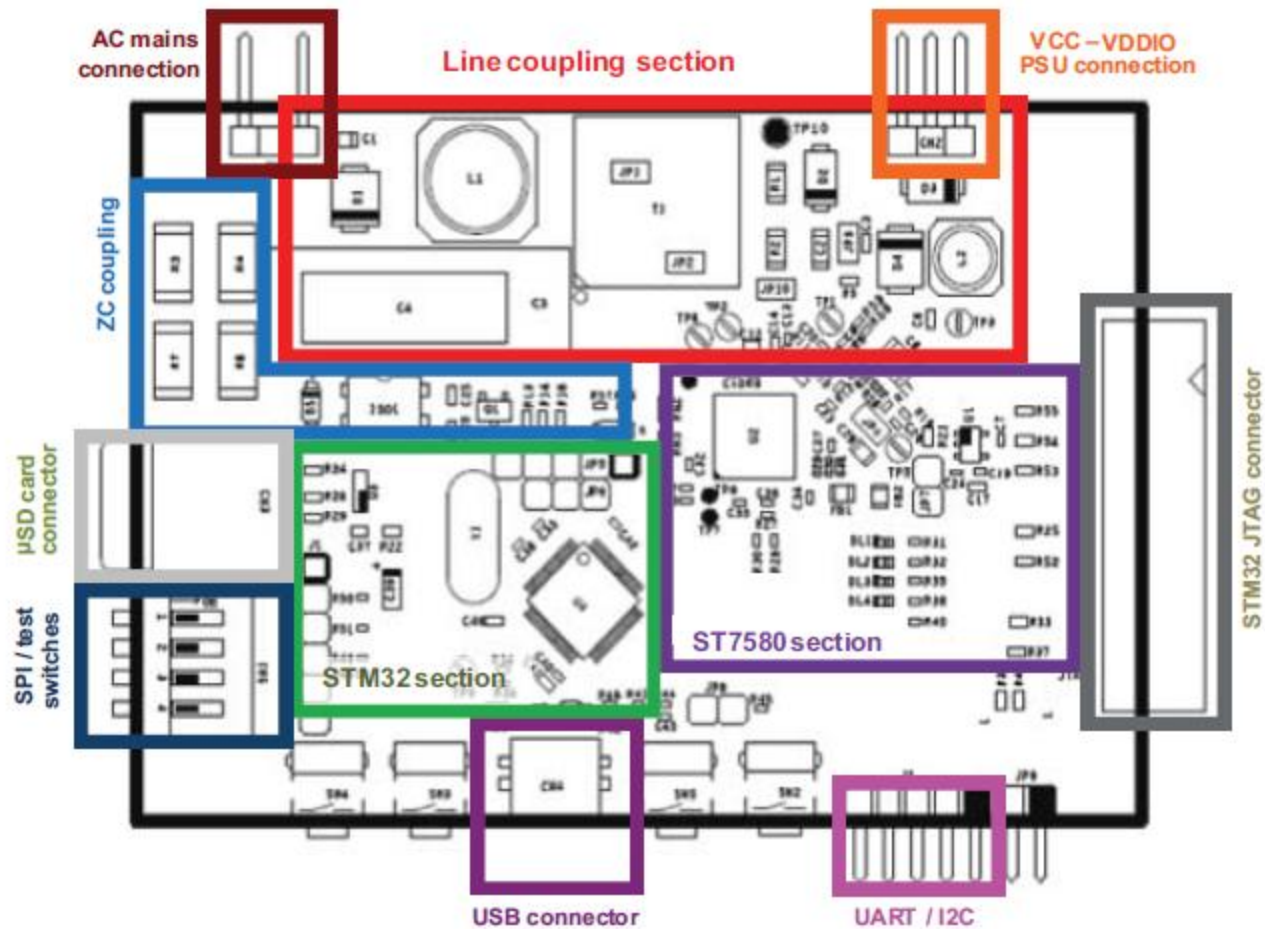


ST7580: Evalboard (schematic)





ST7580: Evalboard (functional blocks)





MODEM CONFIGURATION

COM settings | **Modem configuration** | Communication | MIB | Ping Session

RX layer
DL layer ▼

Sniffer
On
Off

CRC Length
CRC-32 LE ▼

Fields involved in CRC
Payload ▼

Modem Configuration Write **Modem Configuration Read**

PHY CONFIGURATION

Frequencies **RX settings** **TX settings**

High Freq [Hz]
86000

Low Freq [Hz]
72000

RX channel
Single (High) Channel ▼

RX High ch. mode
PSK ▼

RX Low ch. mode
PSK ▼

Current Ctrl **TX Gain**
On
Off

ZC Delay Code
0

FSK settings **PSK settings**

Baudrate
2400 bps ▼

Preamble length
32 bits ▼

Deviation
1 ▼

UW Length
16 bits ▼

UW MSB/LSB
9B x 58

Preamble Length
32 bits ▼

PHY Configuration Write **PHY Configuration Read**



ST7580 GUI: Communication

TRANSMISSION BOX

COM settings | Modem configuration | **Communication** | MIB | Ping Session

TRANSMISSION

TX layer DL_DATA	Frame Modulation BPSK	TX Freq [Hz] 86000	TX Gain Custom PHY Cfg SS Header len 0
TX Freq Custom PHY Cfg	TX Freq Set (PHY Cfg) High Low	TX Freq Overwrite Yes No	ZC Delay PHY Cfg Random

Data Request

Payload 0123456789ABCDEF **Length** 8

RECEPTION BOX

RECEPTION

Received Frame PHY_DATA	RX Freq (PHY Cfg) High Low	PGA Code 0	SNR [dB] 0
Frame Modulation BPSK	ZC Delay Code 0	Payload length 0	

Payload



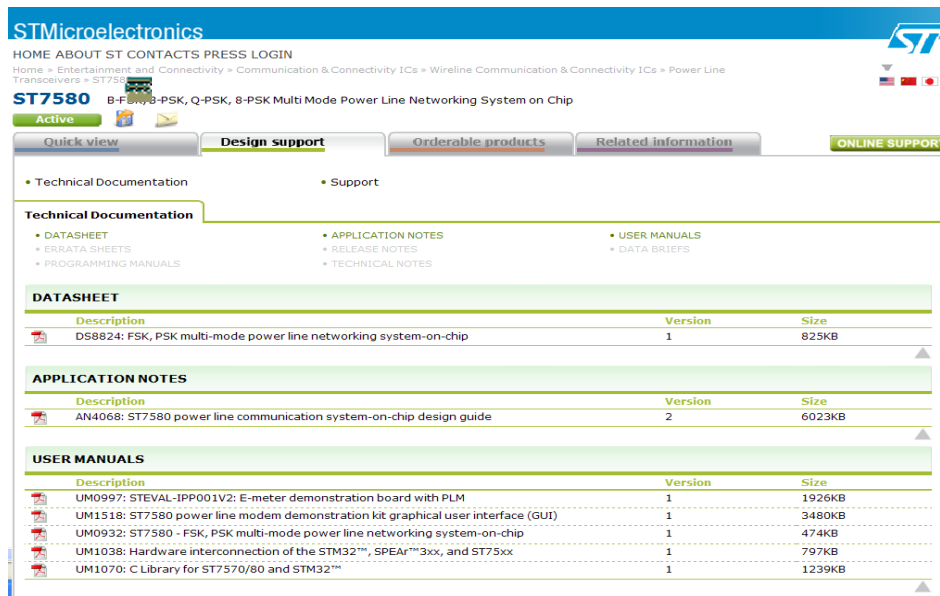
► Click here  for ST PLC Information, Documentation, Support

- Data Sheet
- Application Note
- User Manuals

www.st.com/powerline

► Click here  for EVALKITS support

- Data Brief
- User Manual
- Evaluation boards Bill of Material
- PCB Layout
- Schematics
- SW GUI



Description	Version	Size
DS8824: FSK, PSK multi-mode power line networking system-on-chip	1	825KB

Description	Version	Size
AN4068: ST7580 power line communication system-on-chip design guide	2	6023KB

Description	Version	Size
UM0997: STEVAL-IPP001V2: E-meter demonstration board with PLM	1	1926KB
UM1518: ST7580 power line modem demonstration kit graphical user interface (GUI)	1	3480KB
UM0932: ST7580 - FSK, PSK multi-mode power line networking system-on-chip	1	474KB
UM1038: Hardware interconnection of the STM32™, SPEAr™ 3xx, and ST75xx	1	797KB
UM1070: C Library for ST7570/80 and STM32™	1	1239KB



Thanks for your attention

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