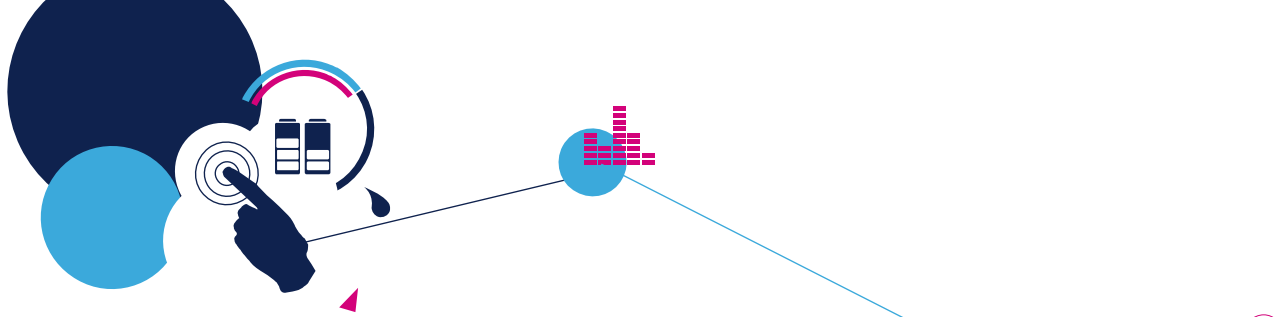
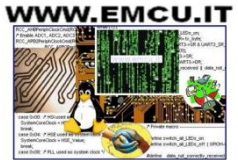
STM32L4 – Architecture



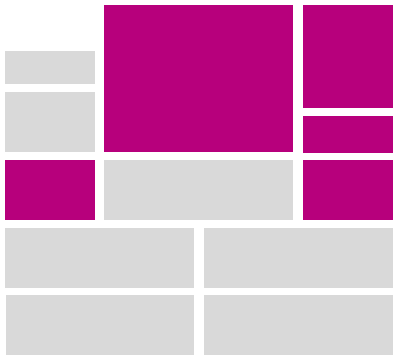
life.augmented



AVNET Memec

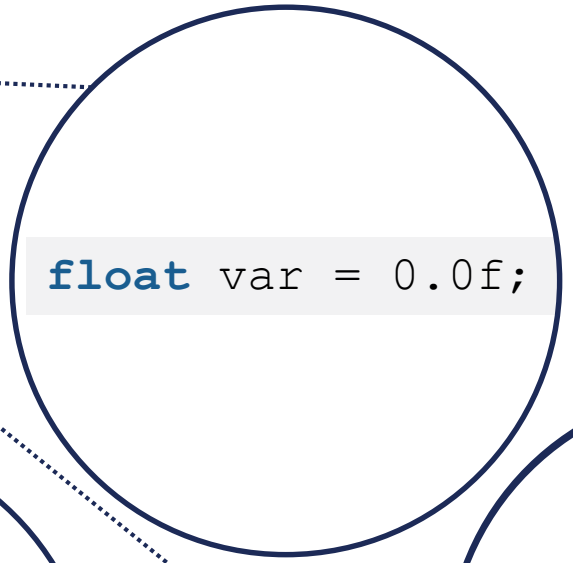
SILICA An Avnet Company

1 High-performance



STM32 L4

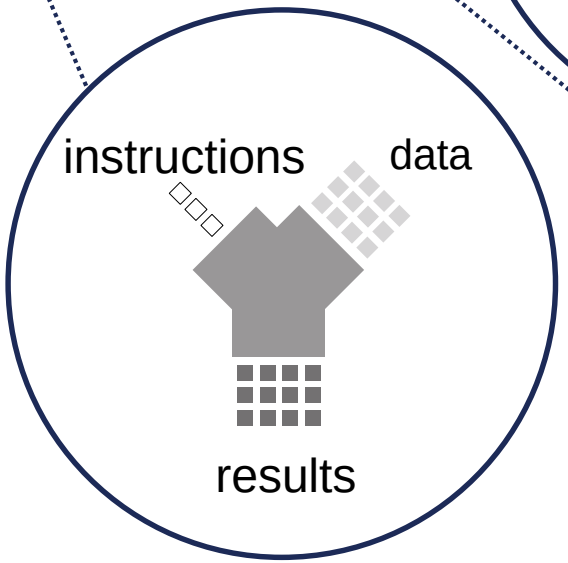
FPU coprocessor



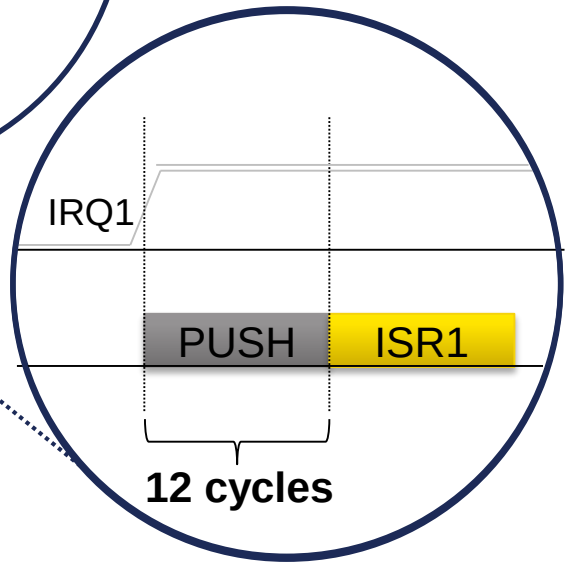
ARM® Cortex®-M4F

I-bus D-bus S-bus

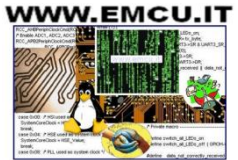
BUS MATRIX



SIMD instructions



Known IRQ latency



life.augmented

AVNET Memec SILICA An Avnet Company

Memory

STM32 L4

ARM® Cortex®-M4F

I-bus D-bus S-bus

BUS MATRIX

~0WS whatever CPU frequency is

Dual-Bank (RWW)

1kB OTP memory

ART

FLASH (1MB)

OTP

System Memory

64+8bit (ECC)

Bootloaders

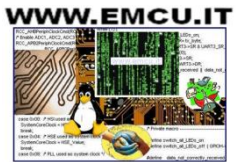
SRAM1 (96kB)

SRAM2 (32kB)

- 32+4bit(parity)
- Readout protection
- Write protection

FMC QUADSPI

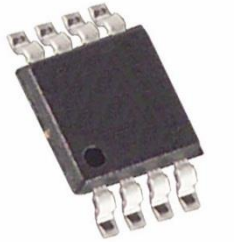
NOR FLASH
NAND FLASH
PSRAM
SRAM

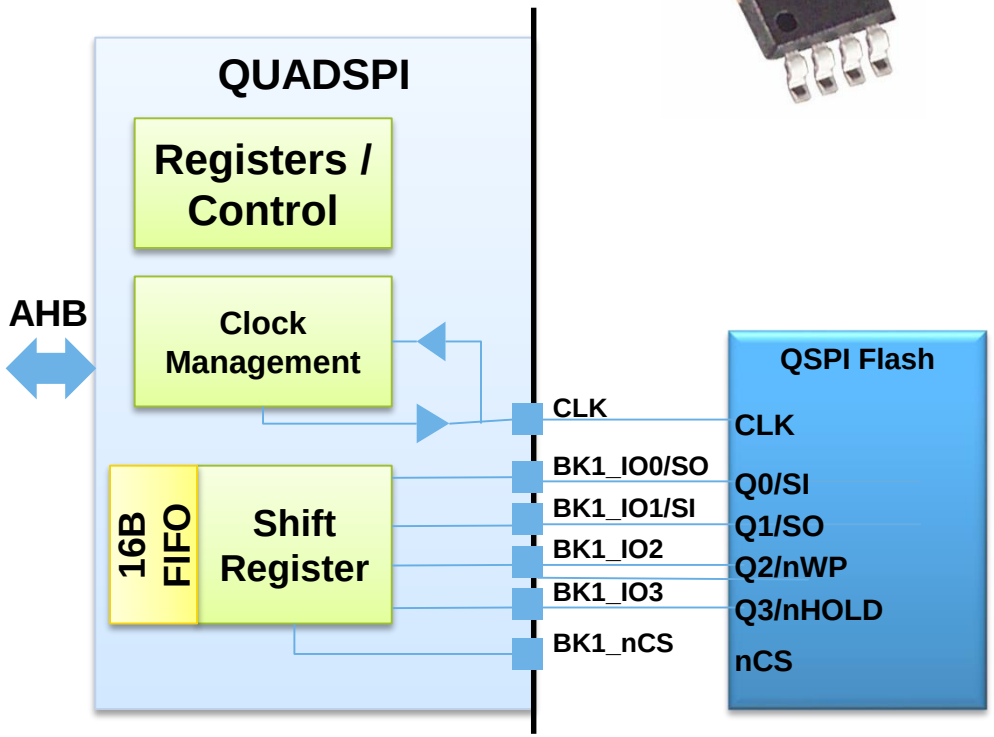


life.augmented

AVNET Memec SILICA An Avnet Company

Quad SPI Interface





- The Quad-SPI memory interface provides a communication interface with **external serial Flash** memories
  - Fully configurable
  - Supports Execute in Place (XiP)
  - Memory mapped

Application benefits

- Supports all SPI Flash memories
- Only a few (4+2) pins needed
- Easy memory expansion in existing project

Performance & power consumption

- Data fetch performance comparison
  - Time to read a 10kB table from external Quad-SPI Flash / internal Flash / internal SRAM
  - Code execution from internal Flash memory

Conditions	External QSPI	Internal Flash	Internal SRAM
CPU @ 80 MHz – QSPI SDR 4 lanes @ 40 MHz	257 µs	152 µs	88 µs
CPU @ 48 MHz - QSPI DDR 4 lanes @ 48 MHz	**214 µs**	227 µs	147 µs

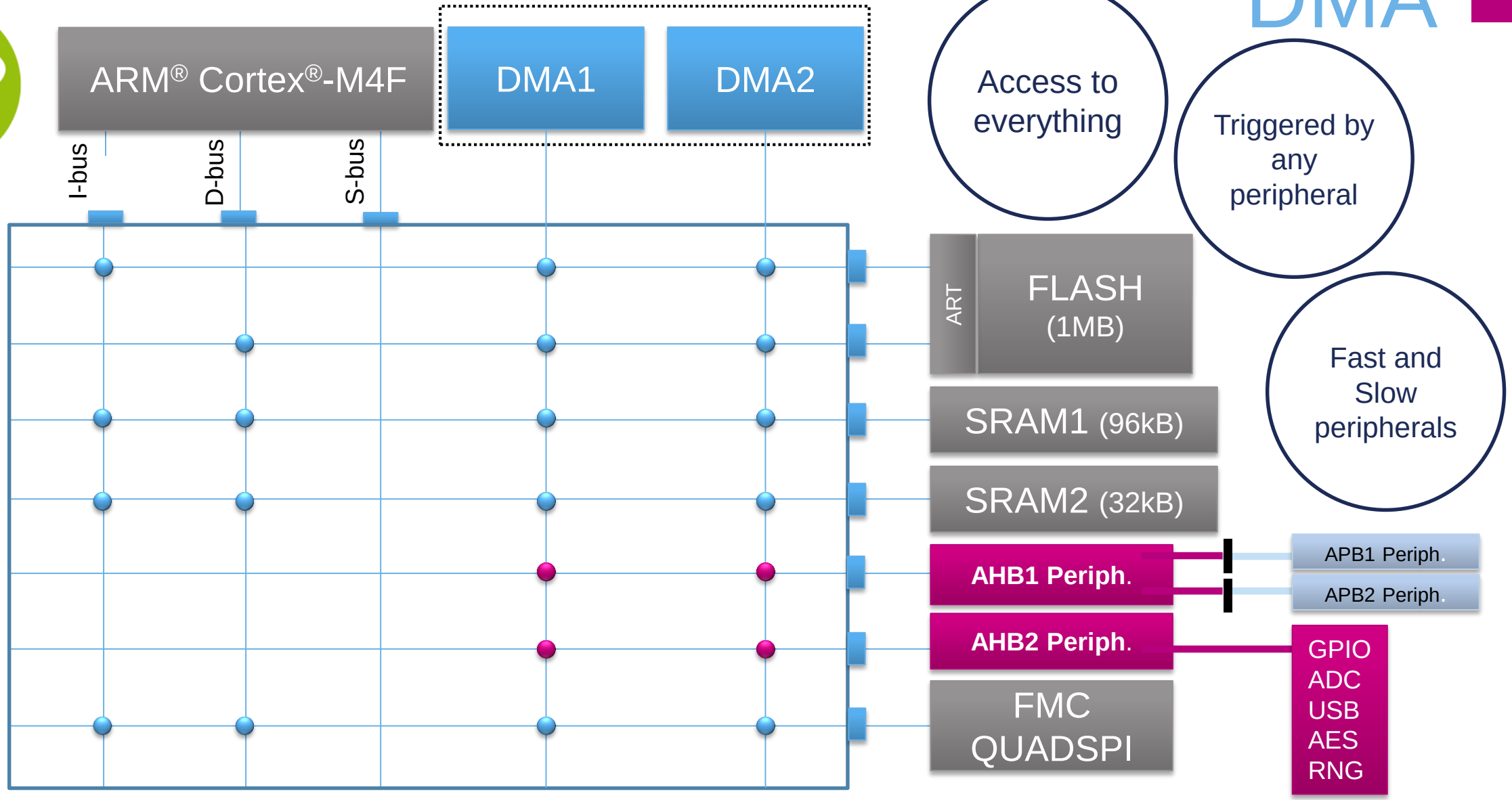
External Quad-SPI: Micron N25Q256A13EF840E / XiP Mode - Internal Flash: ART enable - Compiler: IAR v7.30.1.7746

- Power consumption of the STM32L4 during this benchmark (External Flash memory excluded)

Conditions	External QSPI	Internal Flash	Internal SRAM
CPU @ 80 MHz – QSPI SDR 4 lanes @ 40 MHz	21 mA	12.74 mA	14.11 mA
CPU @ 48 MHz - QSPI DDR 4 lanes @ 48 MHz	14.6 mA	8.79 mA	8.64 mA

External Quad-SPI: Micron N25Q256A13EF840E / XiP Mode - Internal Flash: ART enable - Compiler: IAR v7.30.1.7746
The external Flash consumption depends on the Quad-SPI Flash device.
We measured ~4.7 mA @ 80 MHz/SDR and ~6.1 mA @48 MHz/DDR on data read benchmark for the selected part.

DMA



Access to everything

Triggered by any peripheral

Fast and Slow peripherals

Clock Sources Parameters

STM32 L4

80MHz max

RESET

CLK Source	Frequency	Conso	Precision (0-85°C)	Settling time
MSI (default)	100kHz~48MHz (4MHz default)	**0.6~155µA**	-3.5%~+3%	**10~2.5µs**
MSI (in PLL mode)	100kHz~48MHz		60ps (cycle to cycle jitter)	**252.5µs** (10% of final freq)
HSI	16MHz	155µA	**±1%**	3.8 µs
HSE external crystal	4~48MHz	**~440µA** (8MHz, 10pF)	-	**2ms**
PLL	2~80MHz	~520µA (@344MHz VCO)	N/A	15µs (2MHz input)
LSI	32kHz	0.11µA	**~10%**	125µs
LSE external crystal	32.768kHz (typ.)	**~0.25µA**	-	**~2s**

Including stabilization time

+ Clock Source Wake-Up time

LSE usually woken-up only once after power-on

life.augmented

AVNET Memec

SILICA An Avnet Company

Debug support

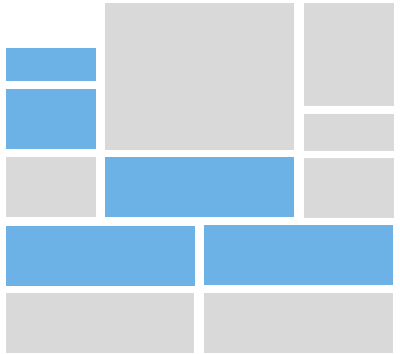
- STM32L4 provides on-chip debug support
  - MCU programming
  - Application debugging
  - Code analysis

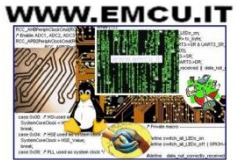
Application benefits

- Basic debugging features
- Advanced features (Embedded Trace Macrocell) to quickly identify malfunctioning code
- Coverage and profiling features

STM32L4 series

1. **High-performance**
2. **Multiple Peripherals**





Connectivity

STM32 L4

6 UART

- up to 10Mbit/s
- 7, 8, 9 data bits
- Even/odd or no-parity
- Synchronous mode (Master)
- Swappable Tx/Rx pins
- Auto-baudrate detection

IrDA SIR, Smartcard, Modbus, LIN, RS-232/485 flow control

SMBus 2.0
PMBus 1.1

3 I2C

- up to 1Mbit/s (Fast Mode+)
- Master or Slave (Multi)
- 7b and 10b addressing mode
- Multiple 7b addressing mode
- Clock stretching support
- Fully programmable timing

3 SPI

- up to 40MHz ($f_{PCLK/2}$)
- Master or Slave (Multi)
- Full/Half-duplex or Simplex
- Two-wire interface as min.
- Motorola and TI standards
- Tx & Rx FIFOs, CRC

1 USB

- USB2.0 Full Speed (12Mbps)
- OTG2.0 spec support
- Link Power Management
- Battery Charger Detection
- HSE crystal not needed (thanks to MSI in PLL mode)

!

1 CAN

- up to 1Mbit/s
- CAN protocol v2.0A and B
- 2x receive FIFO (3 stages)
- 14 scalable filter banks
- HSE crystal not needed (thanks to 1% HSI)

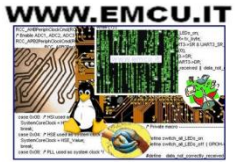
1 SDMMC

- default speed (<25MHz)
- high-speed support (50MHz)
- 1b, 4b and 8b data mode
- Secure Digital (SD) 2.0
- MultiMediaCard (MMC) 4.2
- SD I/O devices (SDIO) 2.0

Wi-Fi, Bluetooth, Camera, Memory modules

DMA support by all these peripherals

life.augmented



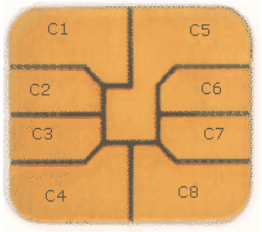
AVNET Memec

SILICA An Avnet Company

Connectivity addon

1 SWPMI

- 100Kbit/s to 2Mbit/s
- single-wire protocol
- ETSI TS 102 613 standard (Master mode)
- Full duplex
- Smartcard interface

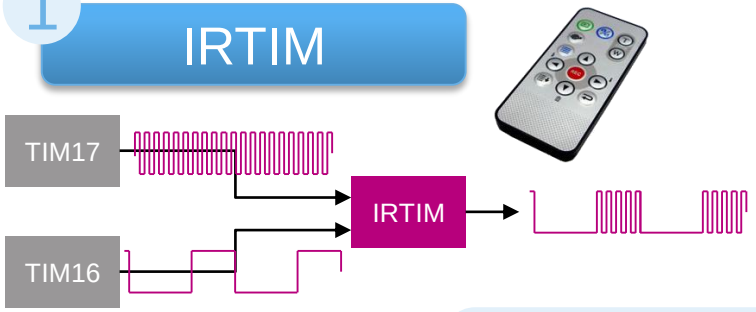


2 SAI

- 2 x Serial Audio Interface blocks
- up to 32-bit/192kHz
- various protocols support (including I2S SPDIF and AC'97)

To external device (DAC…) by I2C

1 IRTIM



Supports RC5, RC6, RCA, SIRC,…

Up to 20mA direct IR LED driving

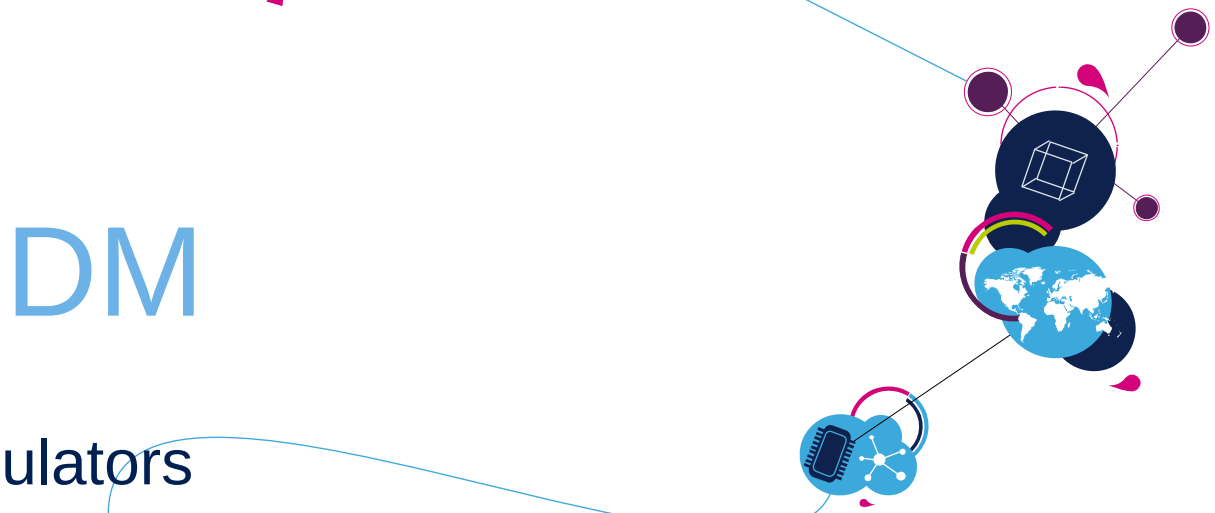
IR_OUT pin

1 DFSDM

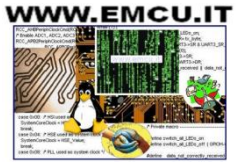
Digital Filter for Sigma Delta Modulators Interface

STM32L4 - DFSDM

Digital filter for Sigma-Delta modulators interface



life.augmented

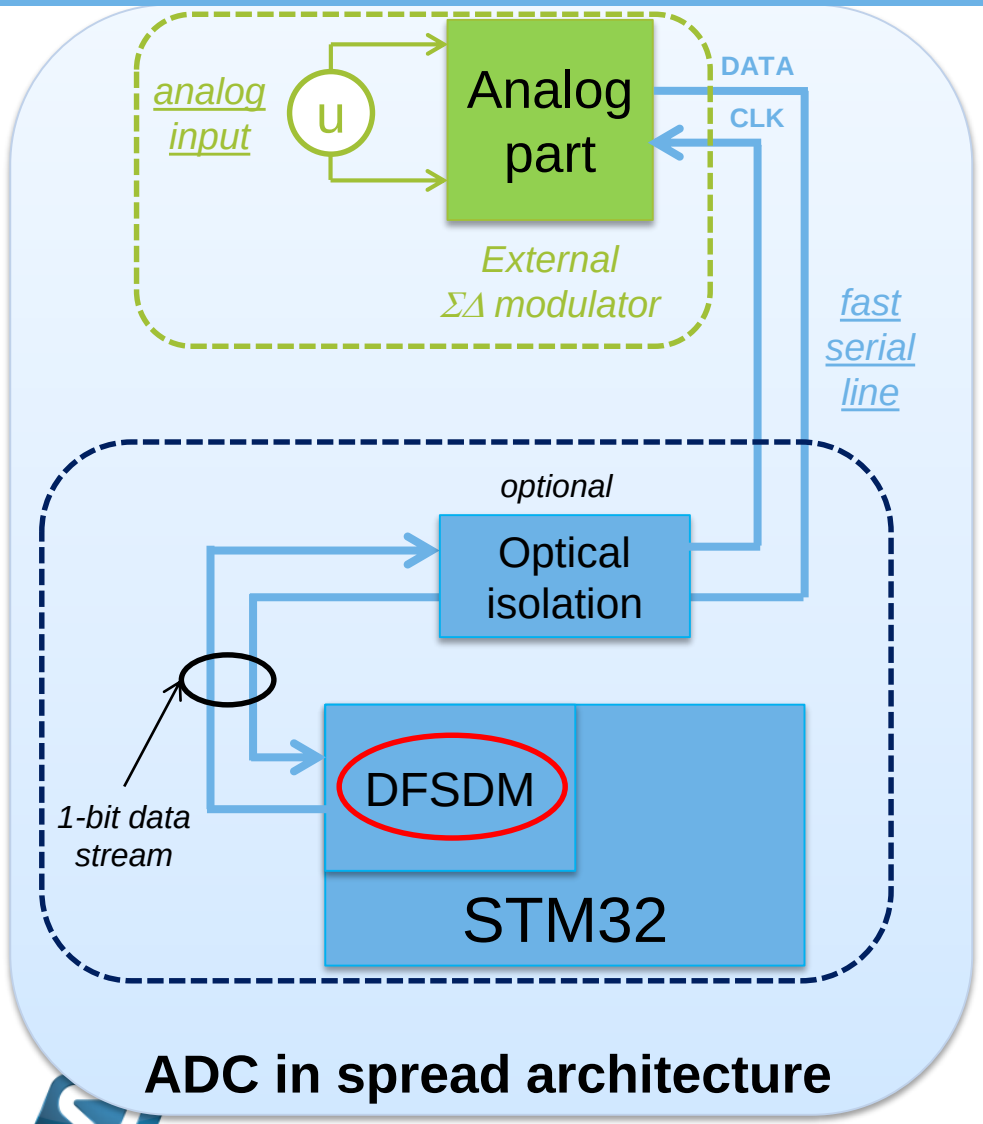


AVNET Memec

SILICA An Avnet Company

DFSDM: introduction and typical usage

Behavior like ADC with scalable speed/resolution and external analog front end

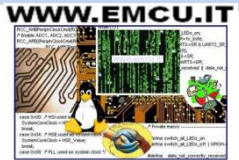


ADC in spread architecture

- Split of analog and digital part:
  - Benefit from external analog selection
  - Benefit from internal digital features (DFSDM)

Application benefits

- External analog part: selection according needs: precision, less noise, extra fast, galvanic isolation, linearity, cheap, high voltage-side operation
- Digital part: serial line interface (1 or 2 wires), scalable speed vs. resolution (up to 24 bits), full features like ADC
- Examples: electricity meter, motor control, medical applications, MEMS microphone audio,



life.augmented

AVNET Memec SILICA An Avnet Company

Key features

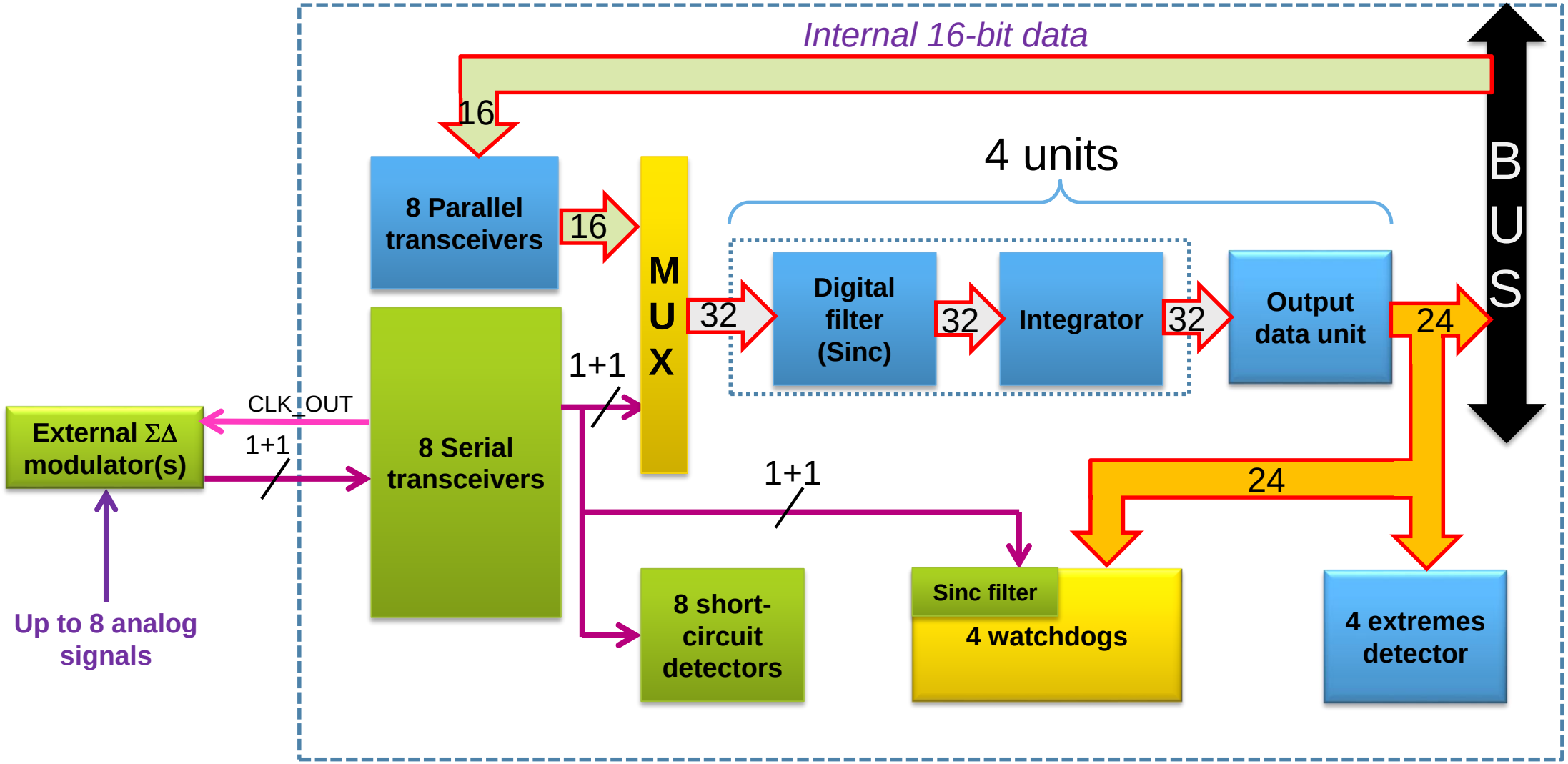
Decreased CPU burden and low-latency HW safety features

- Transceivers
  - Fast serial input (20 MHz):
    - SPI or Manchester-coded mode (with clock absence detection)
    - Clock generation
  - Internal parallel data input
    - 16-bit register data input (write by CPU/DMA)
- Filters
  - Sinc1, Sinc2, Sinc3, Sinc4, Sinc5 and FastSinc filters with oversampling ratio up to 1024
  - Integrator with oversampling ratio up to 1024

Application Benefits

- Support for various ΣΔ modulators suppliers (ST, TI, Analog Devices,…)
- Speed vs. resolution selection by filter configuration
- Internal data post-processing (SAR ADC results, ...)
- Additional functions: watchdog, short-circuit detector, extremes detector, offset correction

Block diagram



„Analog chain“

- low consumption (down to 400nA)
- progr. hysteresis (0, 8, 15 or 27mV)
- low propag. delay (down to 0.1µs)

COMP1

COMP2

- up to 4mA output (35µA I_{VDDA})
- low error with load -3/+1(2.048V), ±2 (2.5V)

VREFINT

1.2V

VREFBUF

V_{REF+} (no 64pin)

ADC/DAC

2.048V / 2.5V

V_{BAT}

$V_{BAT}/3$

DAC1

DAC2

- 2 channels DAC
- 8b or 12b resolution
- Buffered output
- S&H for low-power app
- Noise & Triangular wave generator

OPAMP1

OPAMP2

PGA

- Rail-to-Rail In/Out
- Normal mode (120µA, 1.6MHz GBW)
- LP mode (45µA, 0.42MHz GBW)

Timers / IRQ

Tsensor

V_{TS}

- 4.7µA, 70µs (ON)
- 5µs sampling
- 2.5mV/°C slope
- factory calibration (30°C, 110°C)

ADC1

ADC2

ADC3

- up to 5.33 Msamples/s (12-bit SAR)
- 16-bit with oversampling
- Sequencer, Differential inputs
- Low consumption (210µA @1MSps)
- 3x analog watchdog per ADC

GPIO

life.augmented

Control logic

TIM

- 11x 16-bit timers
- 2x 32-bit timers
- 1x 24-bit SysTick (Core)
- 2x Low-Power timer
- 17x CAPCOM in total
- 6x CAPCOM with compl. out

Suitable for motor control

RTC

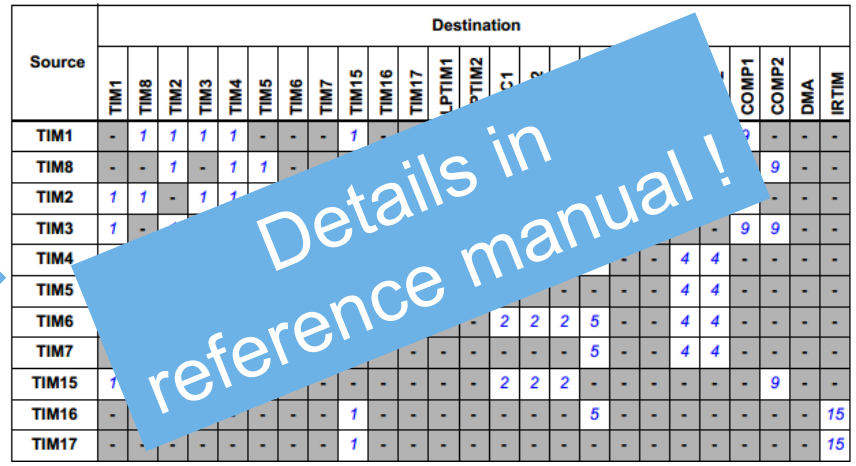
300nA @1.8V

- full calendar support (BCD)
- 2x Alarm (sub-second res.)
- Periodic Wake-Up Timer
- 3x Tamper pins (opt. filtering)
- Smooth digital calibration
- Inside V_{BAT} domain

GLASS LCD

- up to 176 (44x4) or 320 (40x8) segments
- 1/2, 1/3, 1/4, 1/8 or static duty
- 1/2, 1/3, 1/4 or static bias
- Dual-buffer LCD_RAM
- Internal STEP-UP

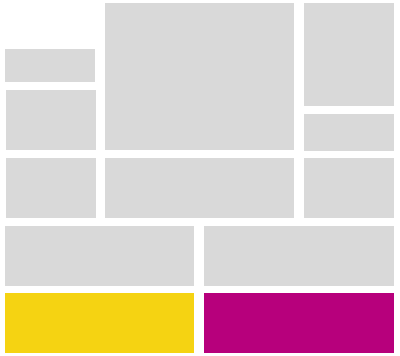
1.5µA @3.0V
1/8 duty, 1/4 bias
64div ratio



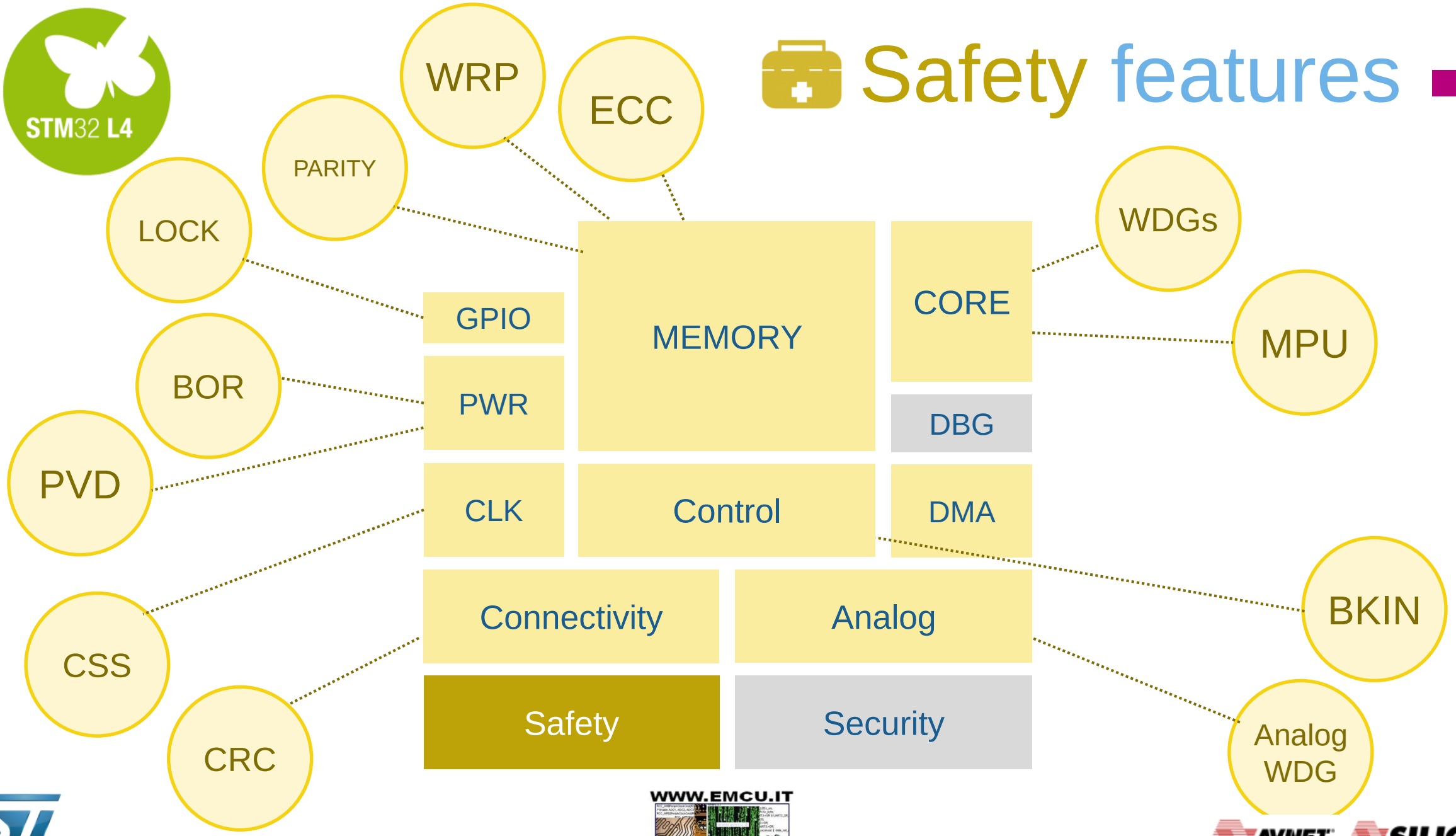
interconnection matrix

STM32L4 series

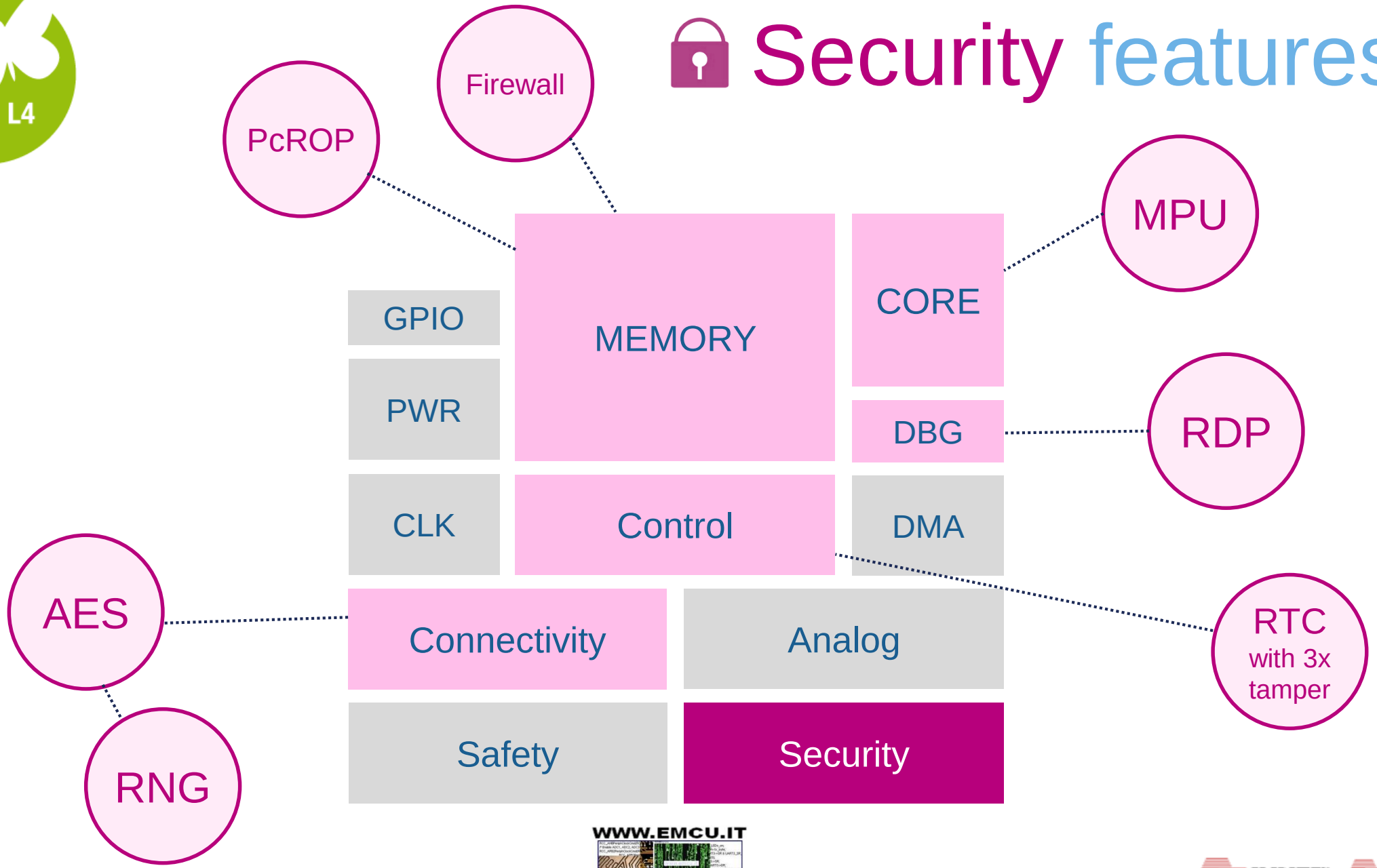
1. **High-performance**
2. **Multiple Peripherals**
3. **Safety and Security featured**



Safety features

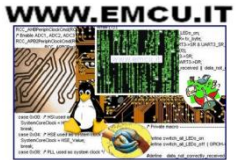


Security features



STM32L4 series

1. High-performance
2. Multiple Peripherals
3. Safety and Security featured
4. Ultra-Low-Power consuming



ULP

STM32 L4

Wake Up

LOW LEAKAGE

Wake Up

ON OFF

LP Entry

ON OFF

Voltage Scaling

Low-Power Modes

GPIO

MEMORY

CORE

PWR

DBG

LP Debug

MSI

CLK

Control

DMA

BAM

Wake Up

LSE

Wake Up

Connectivity

Analog

Low Conso

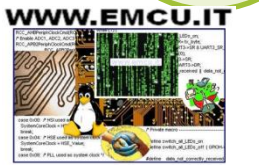
Safety

Security

CSS (LSE)

AES

Painted Green

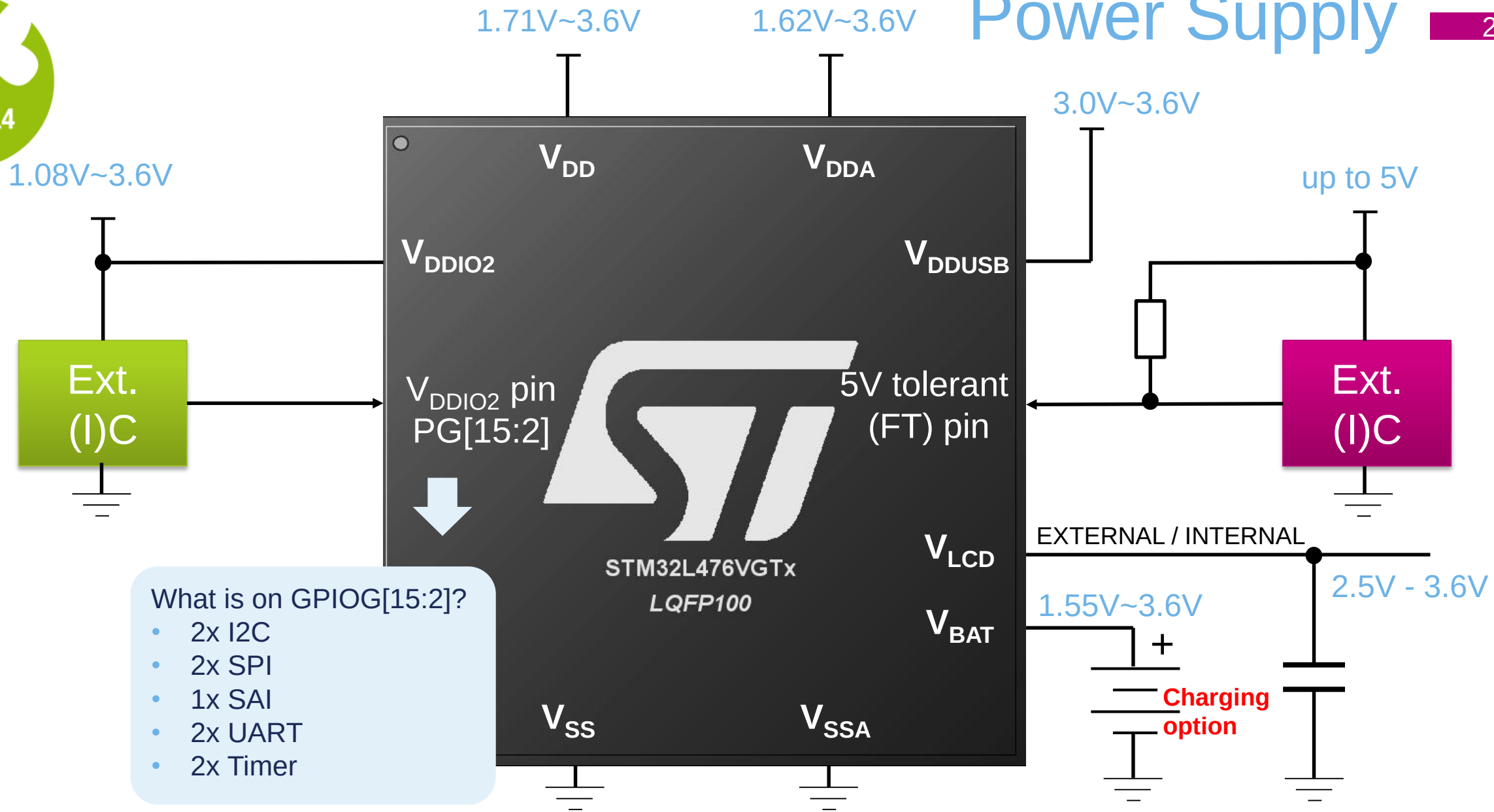


life.augmented

AVNET Memec

SILICA An Avnet Company

Power Supply

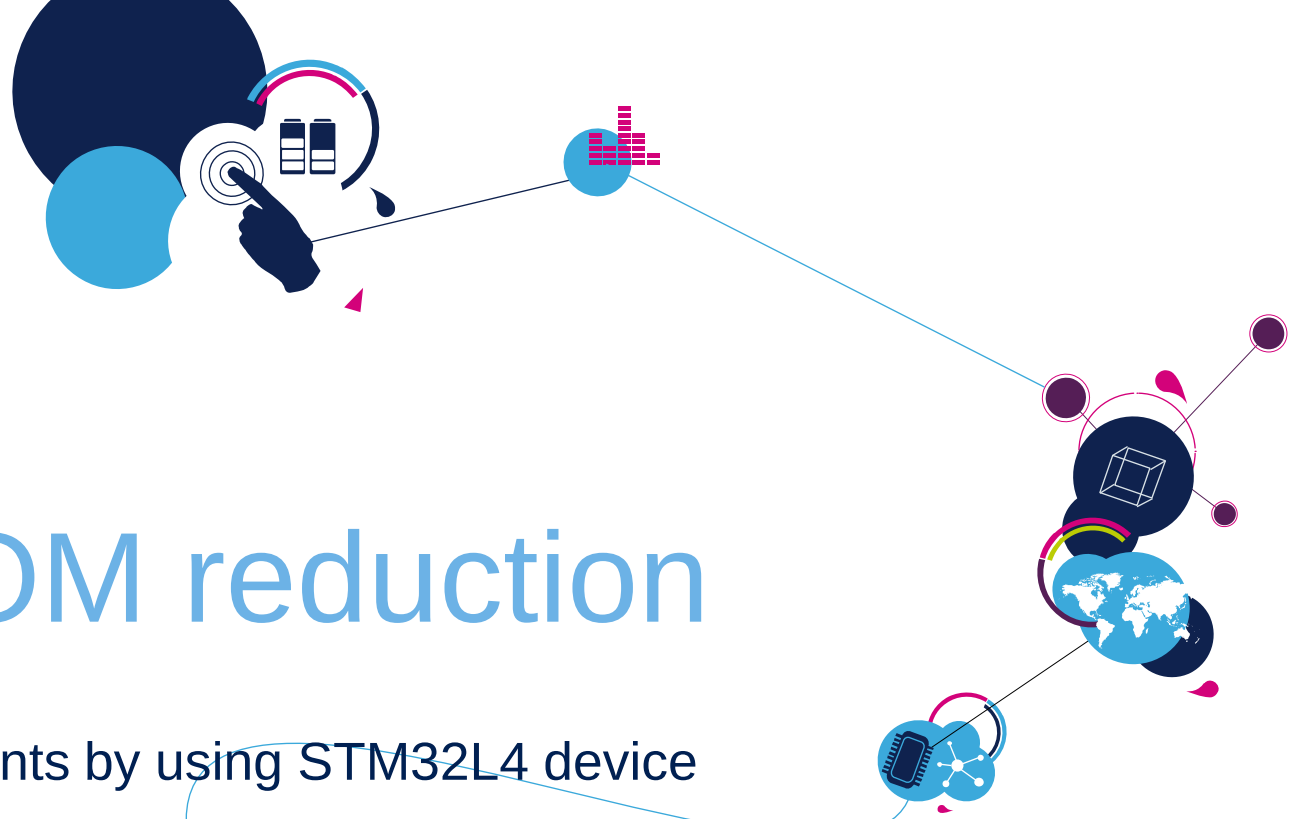


What is on GPIOG[15:2]?

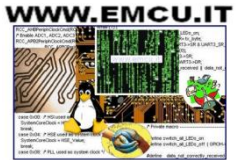
- 2x I2C
- 2x SPI
- 1x SAI
- 2x UART
- 2x Timer

STM32L4 – BOM reduction

How we can reduce list of components by using STM32L4 device



life.augmented

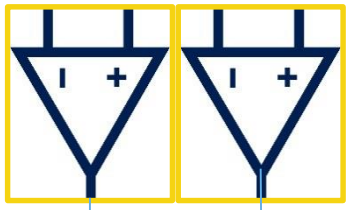


AVNET Memec

SILICA An Avnet Company

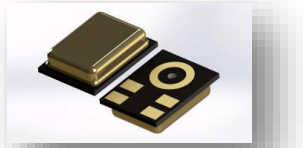
Nice to have, but…

Low cost, low power 2-channel ADC (Single Integration):
2 external comparators
2 external capacitors

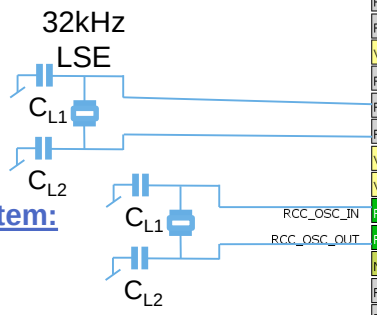


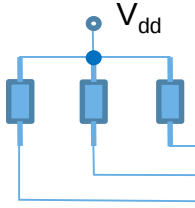
External ADC converter data processing:
High CPU load on data processing

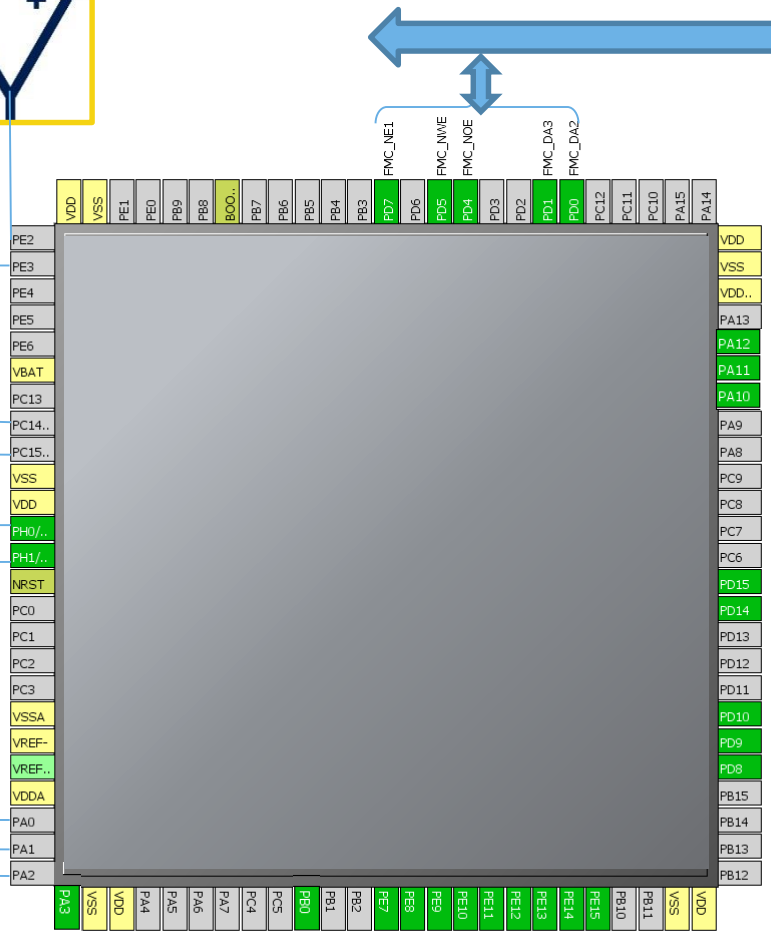
Data collection from stereo MEMS microphone:
High CPU load on PDM decoding



Precise clock for USB and system:
2 lines for the crystal
3 external components



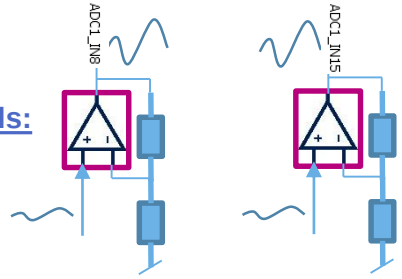




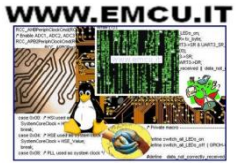
USB connector to the host:
Power supply >3.3V
External resistor
Additional hardware for USB reconnection

Configured state on N I/O lines in STANDBY mode:
N external pull-up/pull-down resistors

Measurement of low amplitude analog signals:
External OpAmps
2 external resistors per OpAmp



External Flash memory to store more data
NOR Flash over FSMC:
19 lines (16 data, 3 control)



life.augmented

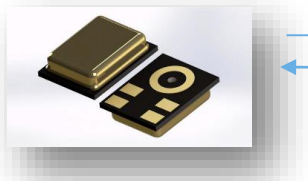
AVNET Memec SILICA An Avnet Company

STM32L4 offer

Low cost, low power 2-channel ADC (Single Integration):
Built-in comparators

External ΣΔ ADC converter data processing:
Built-in Digital Filter for Sigma Delta Modulators

Data collection from stereo MEMS microphone:
Built-in Digital Filter for Sigma Delta Modulators
(HW processing of PDM signal)

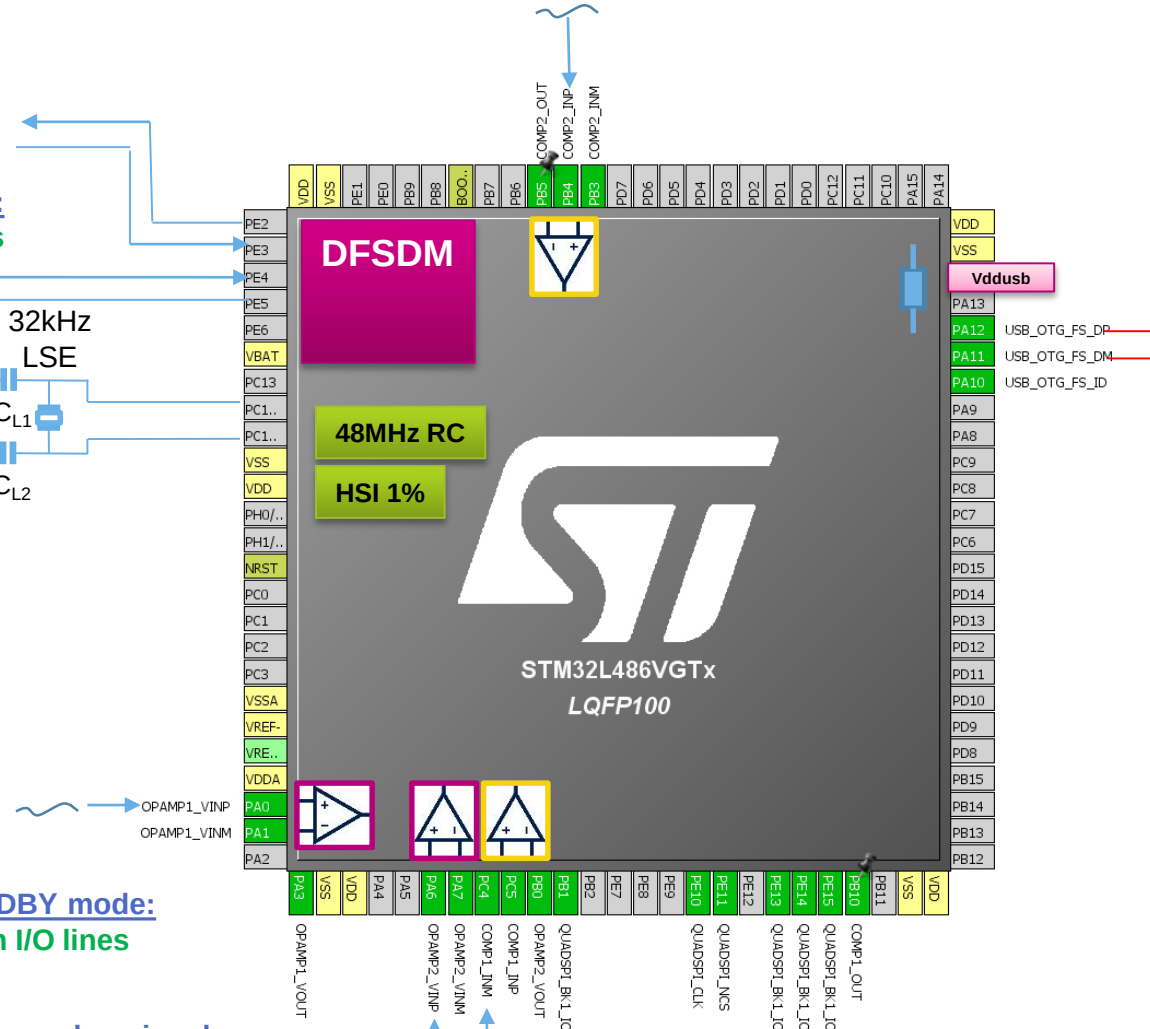


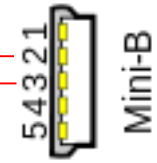
32kHz
LSE

C_{L1}

C_{L2}

Precise clock for USB and system:
Built-in precise RC oscillators:
MSI 48MHz – self-trimmable to LSE



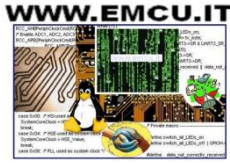


USB connector to the host:
Separate USB power supply
Built-in pull-up resistor on DP line
Software reconnection

Configured state on N I/O lines in STANDBY mode:
Programmable pull-ups/pull-downs on I/O lines

Measurement of low amplitude analog signals:
Built-in PGA (programmable gain amplifiers)
Possible to add external components

External Flash memory to store more data
QSPI Flash memory:
6 lines (4 data, 2 control)



life.augmented

AVNET Memec

SILICA An Avnet Company

Enjoy!

www.st.com/stm32l4

life.augmented

WWW.EMCU.IT

AVNET Memec

SILICA An Avnet Company