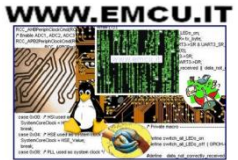
STM32L4 – System operating modes

life.augmented



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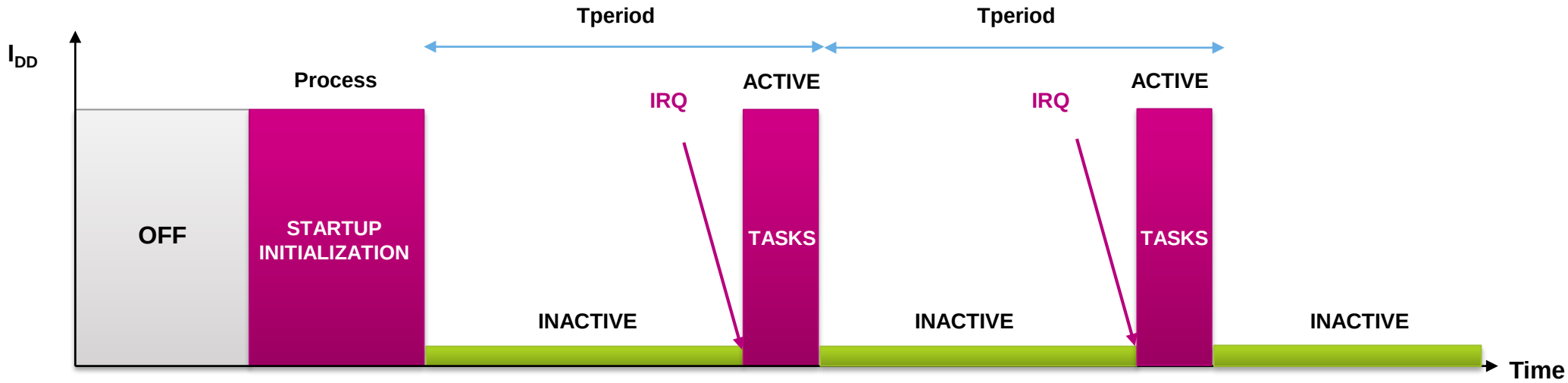
Typical application profile



- Application phases:
  - OFF – power is not applied to MCU
  - STARTUP INITIALIZATION – MCU performs configuration (peripherals, clocks, …)
  - Tperiod
    - INACTIVE – MCU is in low power mode to reduce power consumption
    - ACTIVE – MCU is in normal mode and performs tasks

Overview

Wake-up time		
	RUN (Range1) at 80 MHz	120 µA / MHz**
	RUN (Range2) at 26 MHz	100 µA / MHz**
	LPRUN at 2 MHz	112 µA / MHz**
6 cycles	SLEEP at 26 MHz	35 µA / MHz
6 cycles	LPSLEEP at 2 MHz	48 µA / MHz
4 µs	STOP 1 (full retention)	6.6 µA / 6.9 µA*
5 µs	STOP 2 (full retention)	1.1 µA / 1.4 µA*
14 µs	STANDBY + 32 KB RAM	350 nA / 650 nA*
14 µs	STANDBY	115 nA / 415 nA*
256 µs	SHUTDOWN	30 nA / 330 nA*
	VBAT	4 nA / 300 nA*

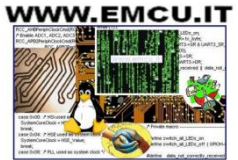
Typ @ VDD =1.8 V @ 25 °C

Application benefits

- High performance
  - ➔ CoreMark score = **273**
- Outstanding power efficiency
  - ➔ ULPBbench score = **187.7**

** : with RTC*
*** : from SRAM1*

life.augmented



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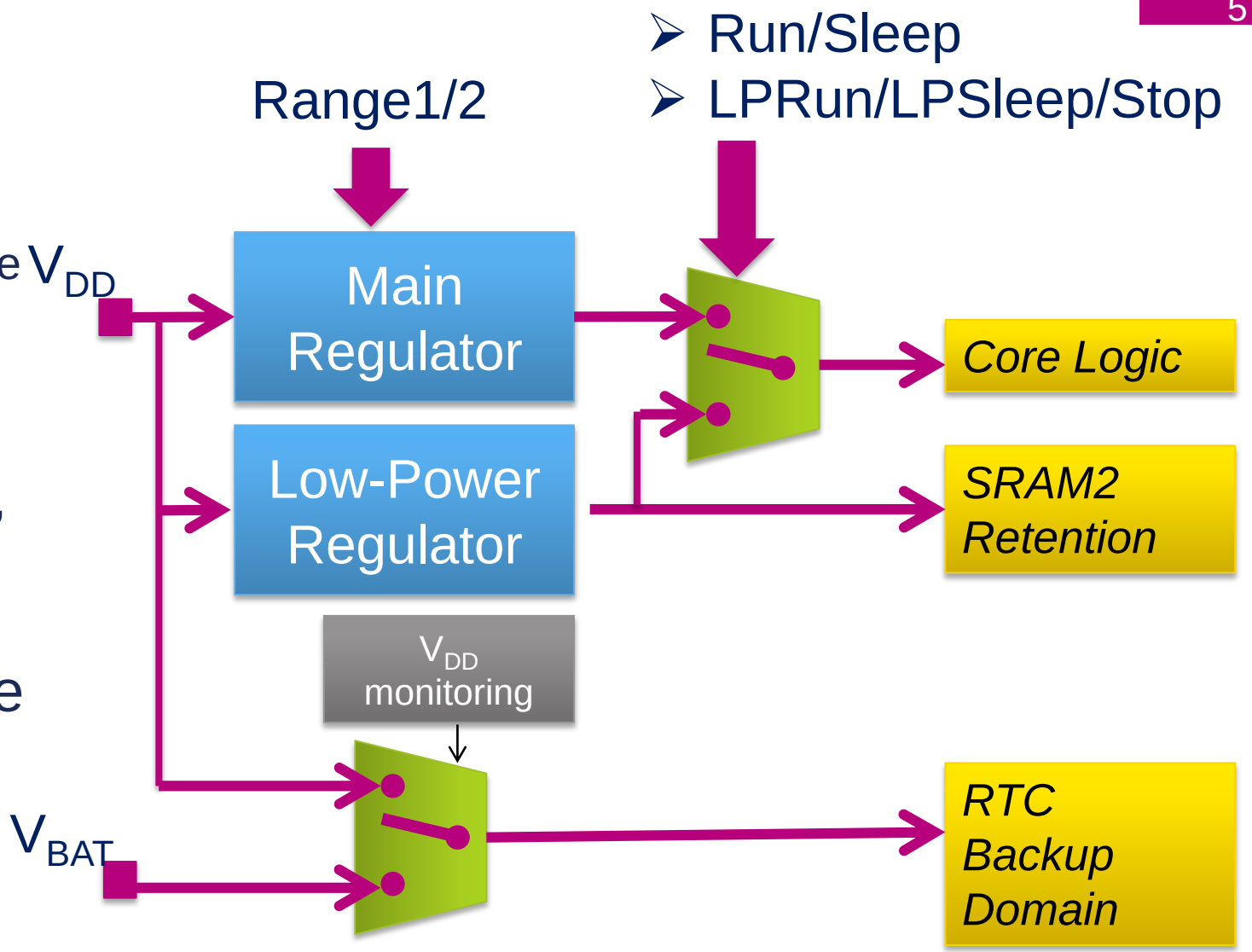
Key features

- Down to **100 µA/MHz** in Run mode with code execution from FLASH (RUN)
- Down to **350 nA** with 32 kB RAM retained (Standby)
- Down to **30 nA** with I/O wake-up (Shutdown)
- Wake-up from high number of peripherals (RTC in each mode)

Voltage regulators

- Two Voltage Regulators
  - The **Main Regulator** with two voltage ranges for Dynamic Voltage Scaling; used in Run and Sleep modes
  - The **Low-power Regulator** for Low-power run, Low-power sleep, Stop 1, and Stop 2 modes
- In Standby and Shutdown mode both regulators are off.



Run mode: Range 1

- All MCU's resources are ON
- System frequency up to the maximum value

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Cortex M4

FLASH memory (1 MB)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low-power Regulator (LPR) up to 2 MHz

Range 1 from FLASH
131 µA/MHz at 80 MHz
(10.5 mA)

Available clocks

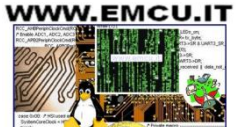
- HSI
- HSE
- LSI
- LSE
- MSI

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock



Run mode: Range 2

- Most of MCU's resources are ON
- System frequency is limited

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
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- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Cortex M4

FLASH memory (1 Mbyte)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low-power Regulator (LPR) up to 2 MHz

Range 2 from SRAM1
100 µA/MHz at 26 MHz
(2,6 mA)

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock

Low-power run mode

- Main regulator is OFF
- System frequency is limited

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
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- Systick Timer
- Touch Sens
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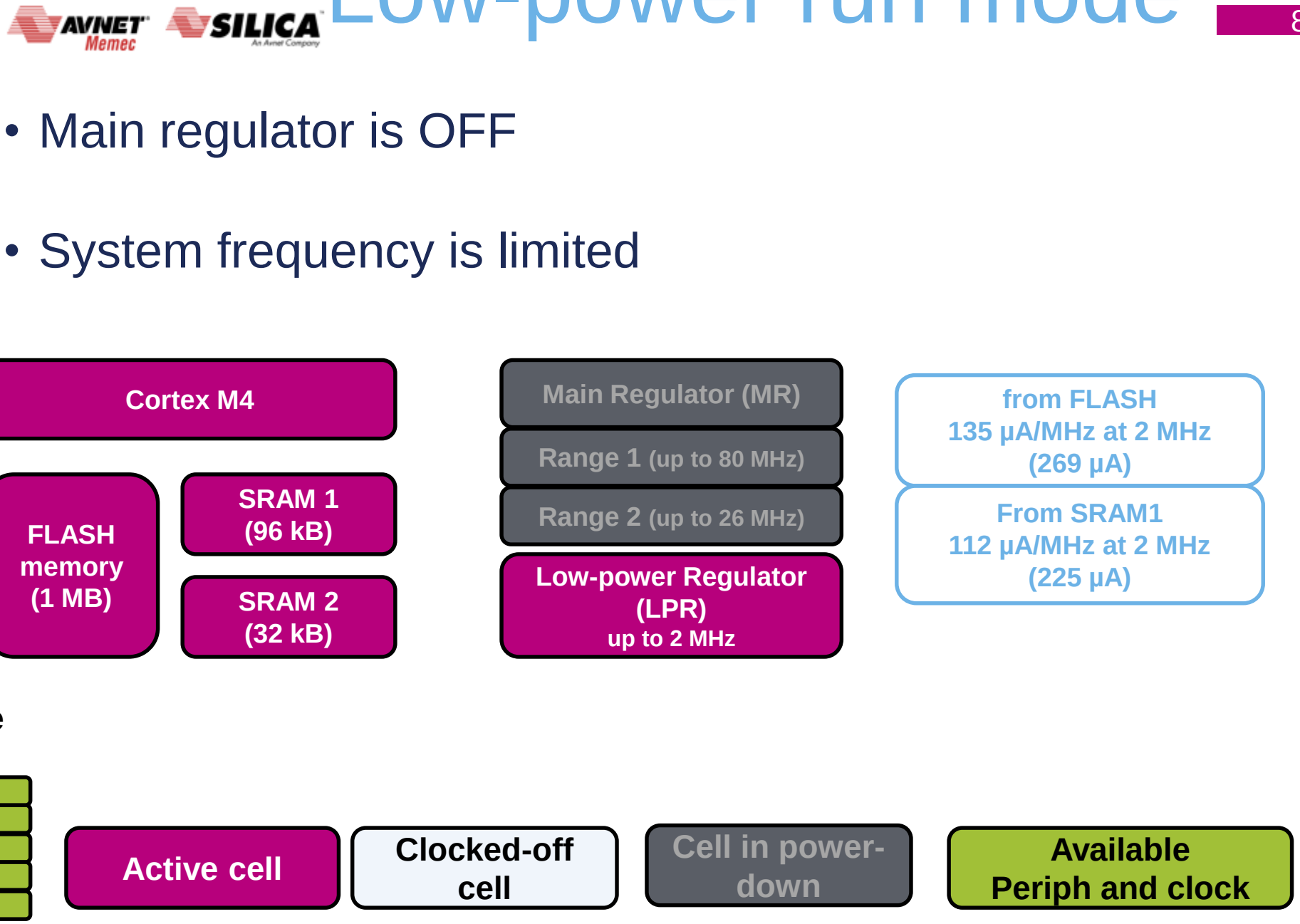
- AES
- CRC

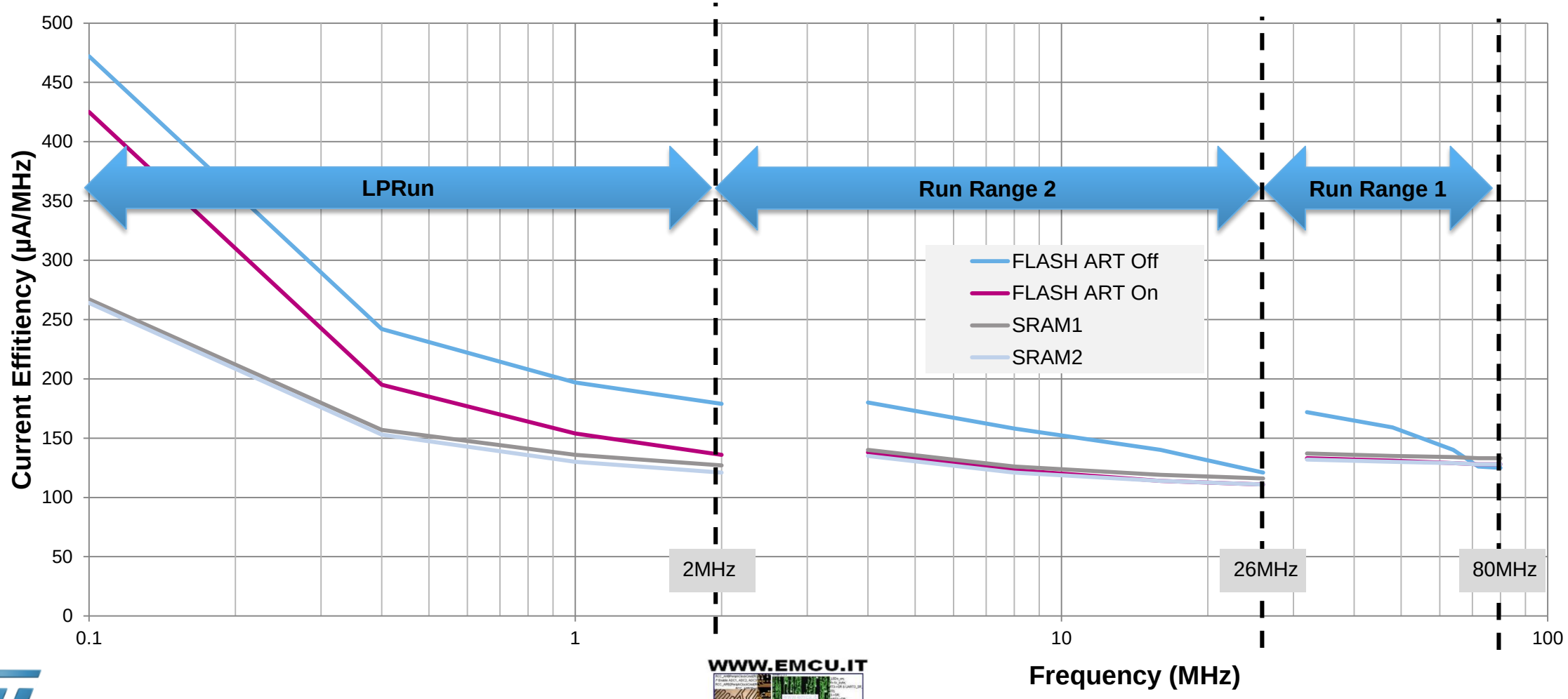
Available clocks

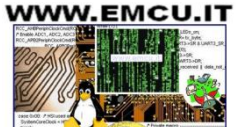
- HSI
- HSE
- LSI
- LSE
- MSI



Power optimization versus frequency

Flexibility between required performance and consumption





Sleep mode

- Core is stopped
- All peripherals and clocks are available
- Fastest wakeup time

Wakeup time: 6 cycles

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
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- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Zzz

Cortex M4

FLASH memory (1 MB)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low Power Regulator (LPR) up to 2 MHz

Range 1
37 µA/MHz at 80 MHz (2.96 mA)

Range 2
35 µA/MHz at 26 MHz (0.92 mA)

Available clocks

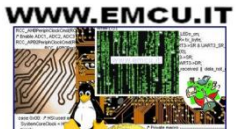
- HSI
- HSE
- LSI
- LSE
- MSI

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock



Low-power sleep mode

- Core is stopped
- Main regulator is OFF
- Fastest wakeup time

Wakeup time: 6 cycles

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
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- RNG
- AES
- CRC

Zzz

Cortex M4

FLASH memory (1 MB)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Range 1 (up to 80 MHZ)

Range 2 (up to 26 MHZ)

Low Power Regulator (LPR) up to 2 MHz

FLASH ON, SRAMs OFF
48 µA/MHz at 2 MHz (96 µA)

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell

Clocked-off cell

Cell in power-down

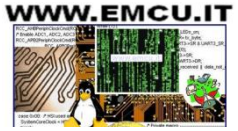
Available Periph and clock

Stop modes

Lowest power modes with full retention

- SRAM1, SRAM2 and all peripheral registers retention
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can stay active to wake device up from Stop mode
- System Clock at wakeup can be HIS or MSI up to 48MHz
- In Stop 2 current consumption is lower; in Stop 1 more active peripherals are supported and wake up time is shorter

Stop 1 mode



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Available peripherals

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

w/o RTC: 6.6 µA @ 3.0 V
w/ RTC: 7.1 µA @ 3.0 V

Wakeup time @ 48 MHz:
In SRAM: 4 µs
In FLASH memory: 6 µs

Zzz

Cortex M4

FLASH memory (1 MB)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Low Power Regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

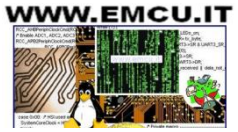
Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Clocked-off cell | Cell in power-down | Available cell



Stop 2 mode

Available peripherals

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

w/o RTC: 1.2 µA @ 3.0 V
w/ RTC: 1.7 µA @ 3.0 V

Wakeup time @ 48 MHz:
In SRAM: 5 µs
In FLASH memory: 8 µs

Zzz

Cortex M4

FLASH memory (1 MB)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Low Power Regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

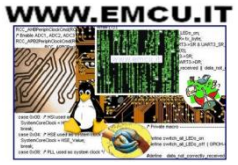
Active cell | Clocked-off cell | Cell in power-down | Available cell

Stop 1 & Stop 2 comparison

Voltage range	Stop 1 mode	Stop 2 mode
Consumption	25 °C, 3 V	25 °C, 3 V
	6.6 µA w/o RTC	1.2 µA w/o RTC
Wakeup time to 48 MHz	6 µs in FLASH memory 4 µs in RAM	8 µs in FLASH memory 5 µs in RAM
Wakeup clock	**MSI** (configurable **up to 48 MHz)** or **HSI (**at **16 MHz)**	
Peripherals	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG	
	USB (suspend, ADP) 2 LP TIMERs 1 LP UART (Start, address match or byte reception) 5 UARTs (Start, address match or byte reception) 3 I2C (address match) SWPMI (resume from suspend)	1 LP TIMER (**LPTIM1**) 1 LP UART (Start, address match or byte reception) 1 I2C (**I2C3**) (address match)

Lowest power mode with SRAM2 retention

- Ultra low power consumption, down to 115 nA without SRAM retention
- Possibility to **retain 32 kB of SRAM2**
- **5 wakeup pins**: the polarity of each of the **5** wakeup pins is configurable
- Wakeup clock is **MSI configurable from 1 to 8 MHz**



Standby mode with or without SRAM2

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

w/ SRAM

w/o RTC: 390 nA @ 3.0 V
w/ RTC: 890 nA @ 3.0 V

w/o SRAM

w/o RTC: 150 nA @ 3.0 V
w/ RTC: 650 nA @ 3.0 V

Wakeup time @ 8 MHz:
In FLASH memory: 14 µs

Cortex M4

Main Regulator (MR)

FLASH memory (1 MB)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Low Power Regulator (LPR)

Wake-up event

- NRST
- BOR
- RTC + Tamper
- IWDG
- 5 WKUP pins

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Backup domain

Backup Register (32x32-bits)

RTC

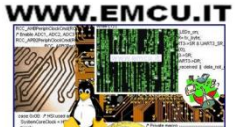
Active cell | **Clocked-off cell** | **Cell in power-down** | **Available cell**

Shutdown mode

Lowest power mode

- Similar to Standby but
  - **NO power monitoring:** no BOR, no switch to VBAT
  - **NO LSI**, no IWDG
- 128-byte **backup registers**
- Wakeup sources: **5 wakeup pins**, **RTC**
- Wakeup clock is **MSI 4 MHz**

Shutdown mode



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Available peripherals

- GPIO
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- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
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- LPTIM 1
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- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

w/o RTC: 60 nA @ 3.0 V
w/ RTC: 550 nA @ 3.0 V

Wakeup time @ 4 MHz:
In FLASH memory: 250 µs

Cortex M4

FLASH memory (1 Mbyte)

SRAM 1 (96 kB)

SRAM 2 (32 kB)

Main Regulator (MR)

Low Power Regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Wake-up event

- NRST
- RTC + Tamper
- 5 WKUP pins

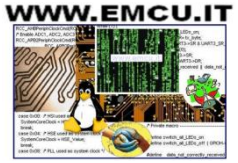
Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Clocked-off cell | Cell in power-down | Available cell

How to associate LP modes

- **RUN:** do you need high computation power, but would like to be green?
- **LOW POWER RUN:** do you have weak power source, but supercapacitors are too costly?
- **SLEEP/LPSLEEP:** do you need peripherals running all the time, but power budget is limited?
- **STOP:** do you need balance between wake up time and low power consumption?
- **STANDBY:** do you need to consume very little power, but still SRAM needs to be retained?
- **SHUTDOWN:** is a low power consumption a top priority in your design?



The End

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