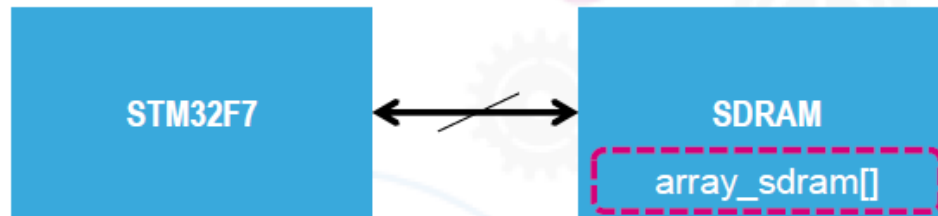


# Hands-On n.1 - Data cache



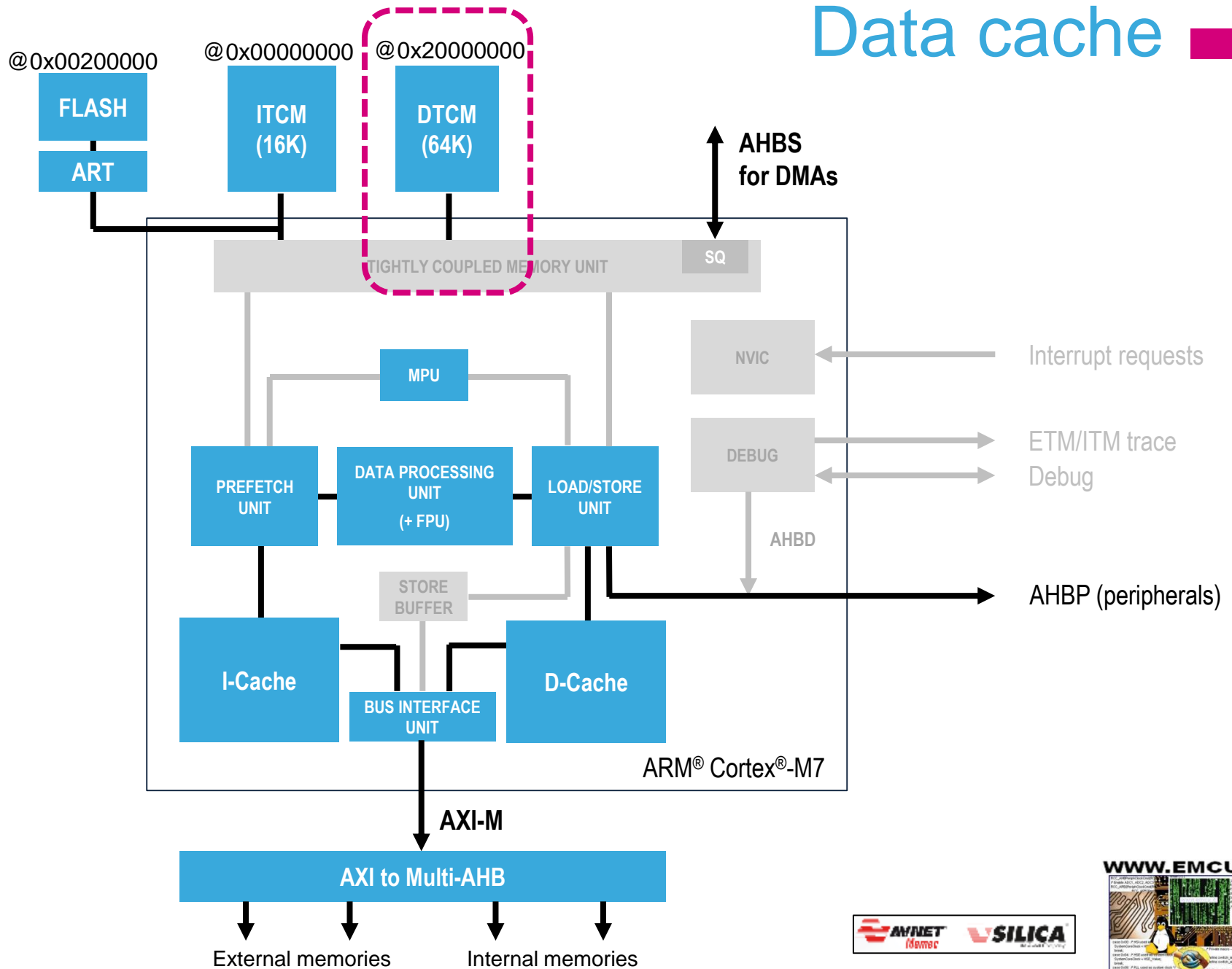
**The purpose of this example is show the difference using an array in SDRAM (with and without cache) and in DTCM**

```
#define NUM_SAMPLES 500
```

```
uint32_t array_sdram[NUM_SAMPLES] __attribute__((at(0xC0000000))); // in SDRAM
uint32_t array_dtcn[NUM_SAMPLES]; // in DTCM SRAM
```

```
// initialize the array with some values
```

```
for (n = 0; n < NUM_SAMPLES; n++)
{
    array_sdram[n] = n;
    array_dtcn[n] = n;
}
```



- Open project

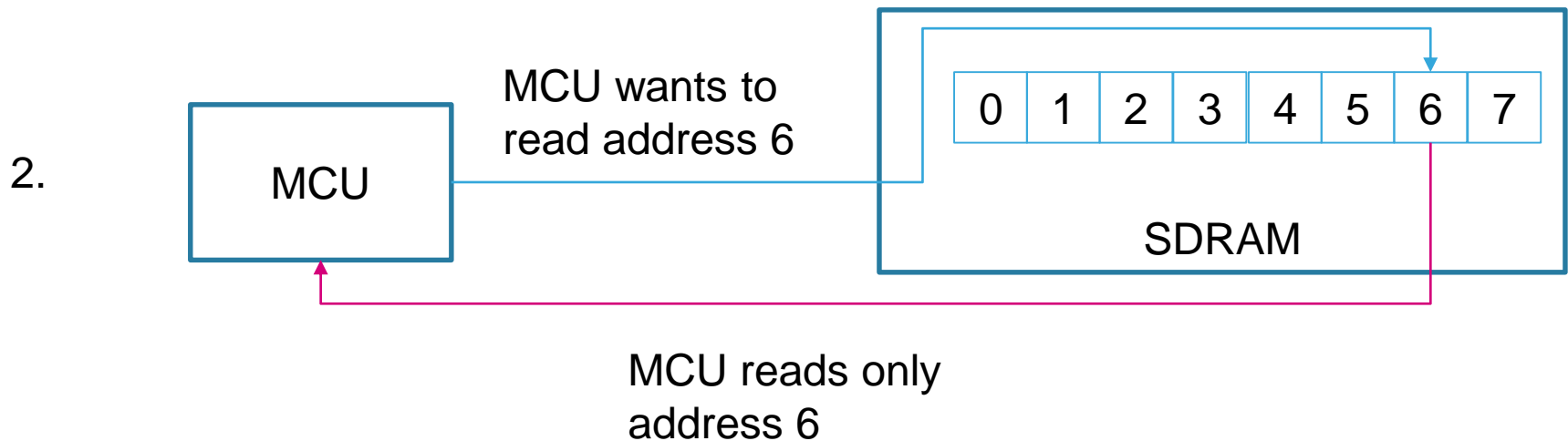
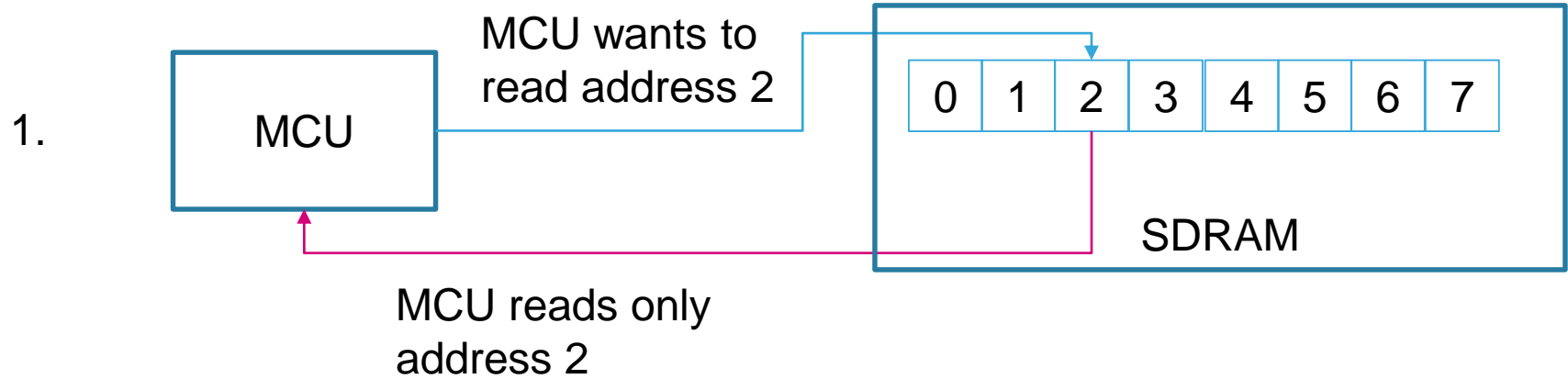
**C:\...\SILICA-STday2015\_M7\_PoliTO\HandsOn\01\_averageDataCache**

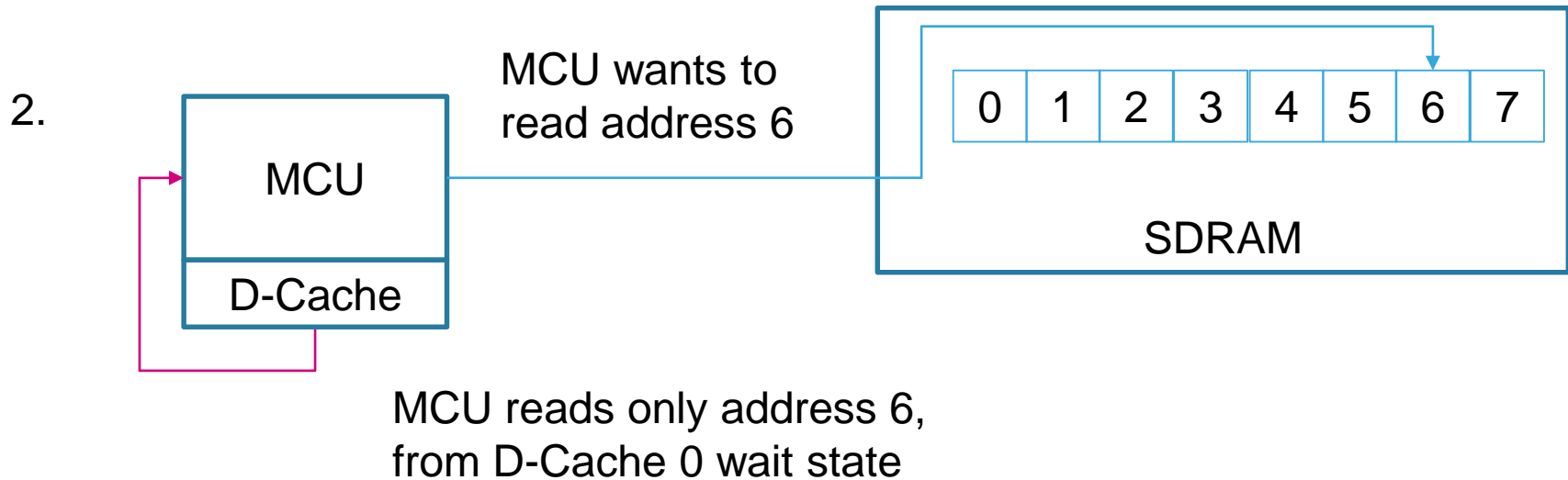
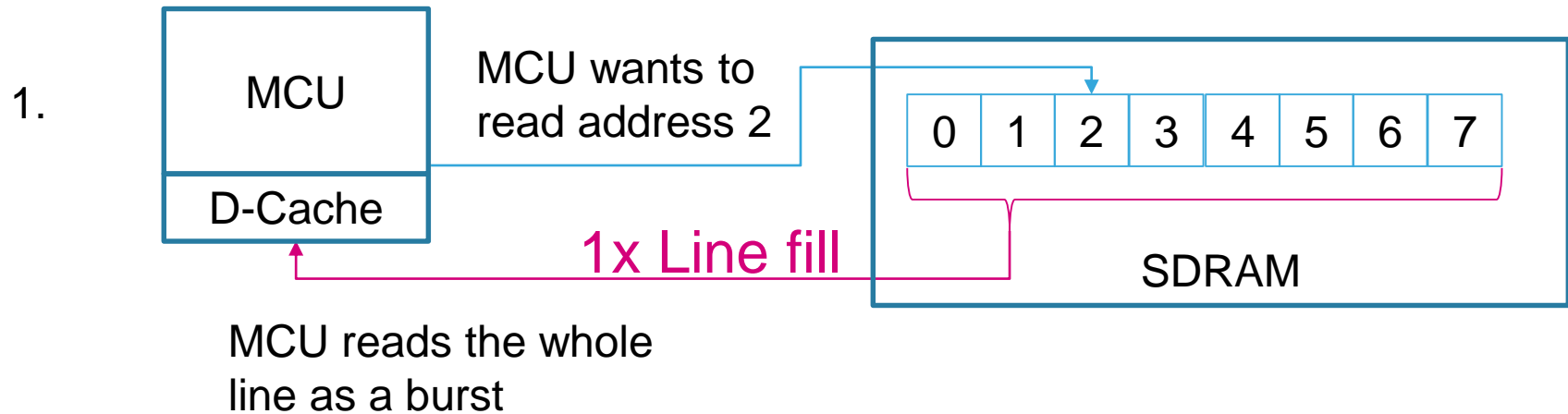
Data placement	D-Cache	Cycles for 500 iterations
DTCM	N/A	1015
SDRAM	Disabled	5605
SDRAM	Enabled 1 <sup>st</sup> run	2955
SDRAM	Enabled 2 <sup>nd</sup> run	1020

Conditions: System clock = 200MHz

# Read without cache

5





# Need more info ?

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For more info contact:

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(B.D.M.)





# Thank you

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