

Hands-On n.2 – Instruction Cache

Open the example:

C:\...\SILICA-STday2015_M7_PoliTO\HandsOn\03_averagelInstructionCacheComplex

Let's try with more complex code

```
for(n = 0; n < NUM_SAMPLES; n++)  
{  
    acc+= ((3*(array1[n] & 0x0F)+ 65) * (25*(array2[n] & 0x0F) + 71)) ;  
}
```

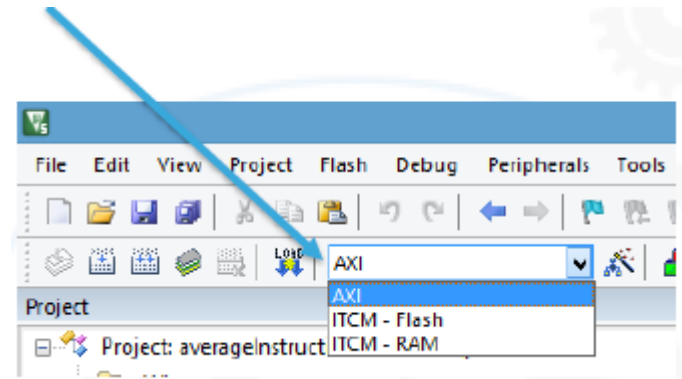
Select AXI or TCM flash through project configurations

This changes the linker options

Conditions:

System clock = 200MHz

Data placed in DTCM



Code placement	System Clock[MHz]	I-Cache or ART	Cycles for 500 iterations
ITCM - RAM	200	N/A	3762
AXI	200	ON	3789
ITCM – flash	200	ON	3786
M4 - Flash	16	ON	6522

ART and I-cache usage result in 0 wait state execution

Need more info ?

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For more info contact:

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Thank you

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