

# Cortex-M7 Training

## F7 architecture new peripherals

### QSPI

T.O.M.A.S. team

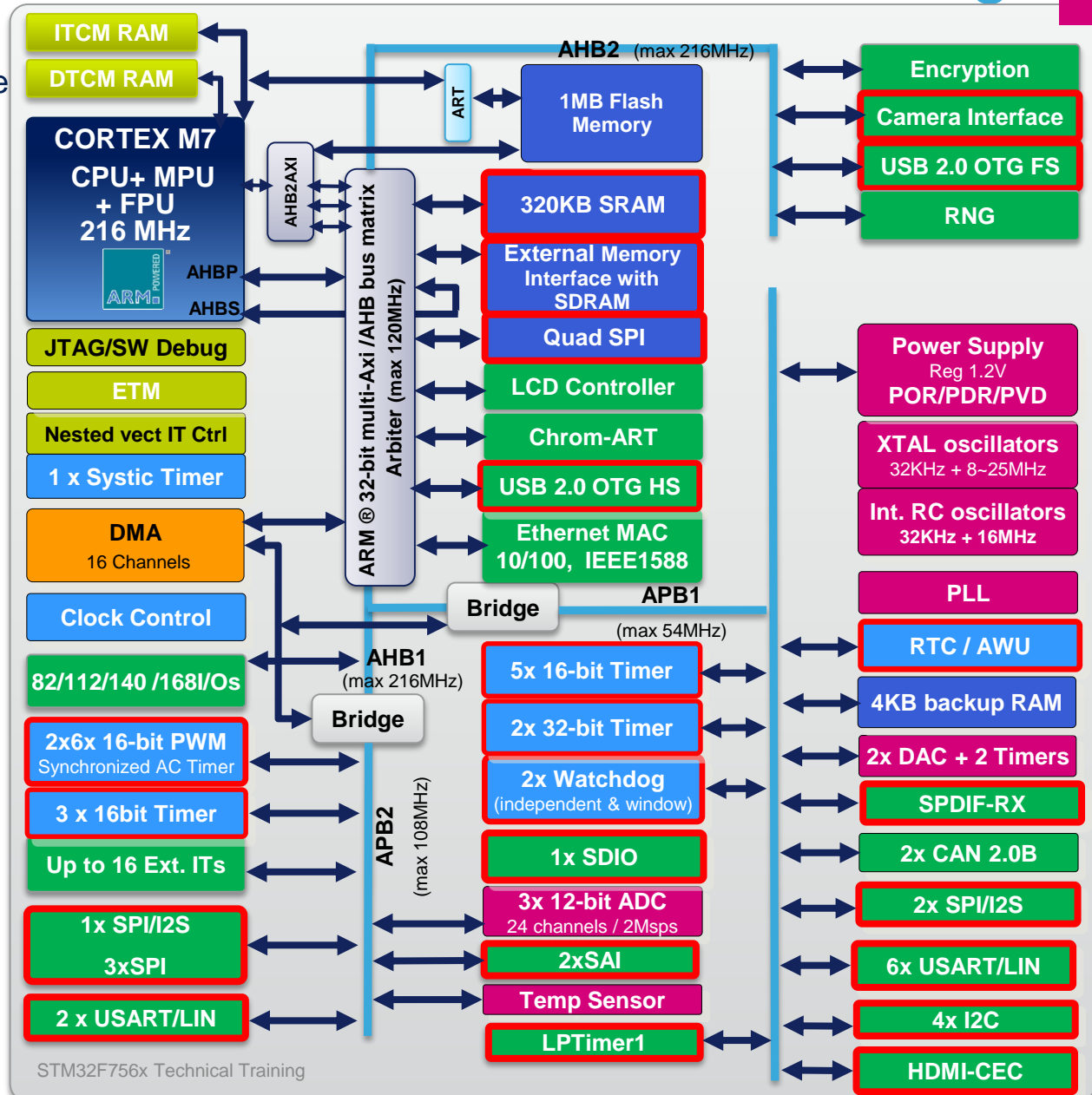


# STM32F7 block diagram

- Fully pin to pin compatible with F42x except for 100pin package
- Up to 216MHz with over-drive mode
- 1MB Flash
- 320KB RAM
- FMC with SDRAM 32-bit
- Audio PLL + Serial Audio I/F
- 100 pins to 216 pins
- 1.71V-3.6V Supply
- Same packages as F429
  - WLCSP143
  - LQFP100,144,176,208
  - BGA 176, 216



**New peripheral generation /  
new Features/ more peripheral  
instances**



# STM32F43x versus STM32F756x

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	STM32F4x 2MB	STM32F756x 1MB	SW compatibility
Power supply	1.71 ~ 3.6V with VBAT 2 Tamper pins	1.71 ~ 3.6V with VBAT Dedicated VDD_USB 3 Tamper pins	
Maximum Frequency	180MHz	216MHz	
Flash	2MB	1MB	
	Dual Bank (RWW)	Single Bank	
System	256KB RAM	320KB RAM	
	4KB Backup SRAM	4KB Backup SRAM	
	Backup-registers 20 x32-bit	Backup-registers 32 x32-bit	
New Peripherals generation	2x WDG	2x WDG	Yes
	1xFMC (+ SDRAM , 32-bit)	1xFMC (+ SDRAM , 32-bit)	Yes
	1xCRC	1xCRC ( programmable polynome)	Yes
	3x I <sup>2</sup> C (with adv features S/PMbus ) and digital filters	4xI <sup>2</sup> C (with adv features S/PMbus ) and digital filters	No

# STM32F43x versus STM32F756x

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	STM32F4x 2MB	STM32F756x 1MB	SW compatibility
New Peripherals generation	6x SPI ( 2xSPI/I2S) (42Mbit/s fixed data)  I2S full duplex	6x SPI (3xSPI/I2S) (45Mbit/s)  I2S Half duplex	No
	4x USART ( IrDa/mLin/iso) 4xUART	4x USART( IrDa/mLin/iso/ SmartCard T=1) 4xUART ( with Drive enable)	No
	1x USB 2.0 FS Device/host/OTG	1x USB 2.0 FS Device/host/OTG + LPM	Yes
	1x USB 2.0 HS Device/device/host/OTG	1x USB 2.0 HS Device/device/host/OTG + LPM	Yes
	2x PWM 16-bit MC timer 2xTim 16bit for DACs 2xTim 32bit / 4ch 2xTim 16bit / 4ch 2xTim 16bit / 2ch 4xTim 16bit / 1ch	2x PWM 16-bit MC timer 2xTim 16bit for DACs 2xTim 32bit / 4ch 2xTim 16bit / 4ch 2xTim 16bit / 2ch 4xTim 16bit / 1ch	Yes
Same peripheral with new features	1x RTC/AWU	1x RTC/AWU	Yes
	1xSAI	2xSAI ( With SPDIF Out)	Yes
	1xDCMI(14-Bit)	1xDCMI (14-Bit) with B&W	
	1xSD/MMC	1xSD/MMC + Fixed HW Flow control limitation	

14 x TIMERS !!!

# STM32F43x versus STM32F756x

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	STM32F4x 2MB	STM32F756x 1MB	SW compatibility
Peripheral same as STM32F42xx	16 - Stream DMA		Yes
	2x CAN 2.0B		Yes
	1xEthernet		Yes
	1xCrypto/Hash ( with GCM and SHA2)		Yes
	1xChrom-ARC Accelerator ( DMA2D)		Yes
	1xLCD-TFT controller		Yes
	3x ADC12bit/ 0.41µs/24ch		Yes (*)
	2x DAC 12bit		Yes
New Peripherals	NA	1xQuad SPI +dual flash mode	NA
	NA	1xHDMI_CEC	NA
	NA	1xSPDIF-RX	NA
Pinout	WLCSP143,, LQFP144, LQFP176, UFBGA176, LQFP208, BGA216: <b>Fully compatible</b> LQFP100: <b>Not compatible</b>		

(\*): Timer triggers are not compatible

# Smart-system architecture for performance

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- STM32 F7 uses 2 independent mechanisms to reach 0-wait execution performance:
  - ST ART Accelerator™ for internal Flash memory
  - L1 cache (4 Kbytes+ 4 Kbytes instruction and data cache) for internal and external memories
- AXI and Multi-AHB bus matrix with dual GP DMA controllers and dedicated DMA controllers for Ethernet, USB OTG HS and Chrom-ART graphic HW acceleration,
- Large SRAM with scattered architecture:
  - 320 Kbytes including 240 Kbytes + 16 Kbytes on the bus matrix and 64 Kbytes of Data TCM RAM
  - 16 Kbytes of instruction TCM RAM
  - 4 Kbytes of backup SRAM



All is AXI to AHB with copy paste of AHB part from F4

# Embedded SRAM

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- **ITCM-RAM**

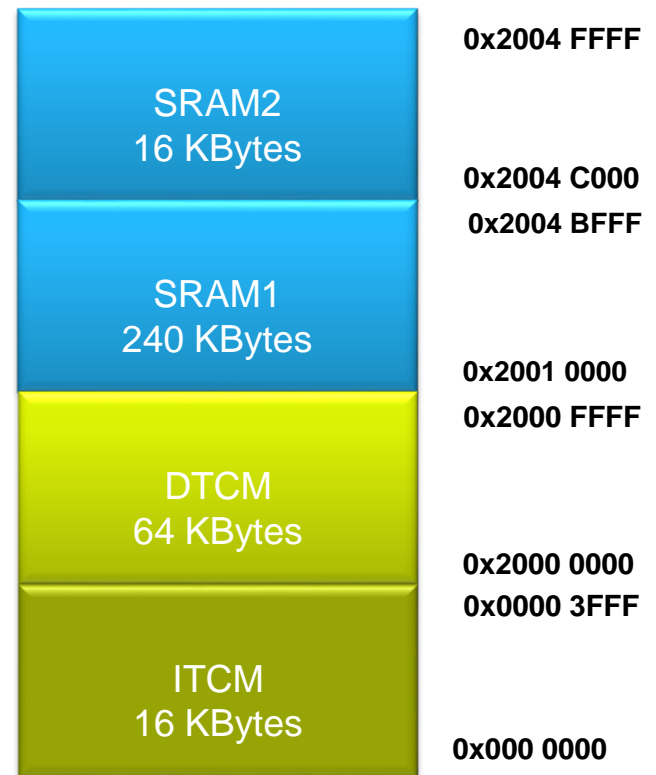
- Instruction RAM (ITCM-RAM) and accessible **only by CPU** for instruction/execution

- **DTCM-RAM**

- Accessible by all AHB masters from AHB bus Matrix through a specific **AHBS bus** of Cortex®-M7.

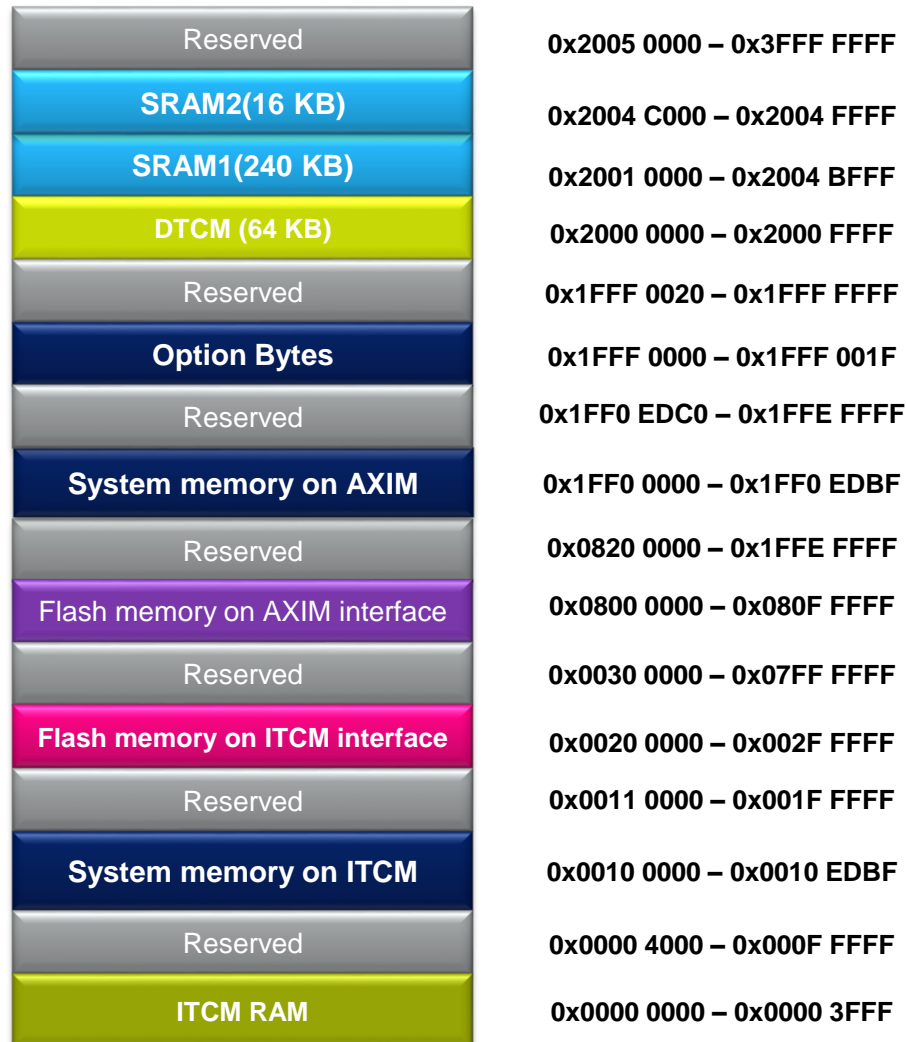
- **SRAM1 and SRAM2**

- Accessible by all AHB masters from AHB bus Matrix.



# STM32F756x - Memory mapping

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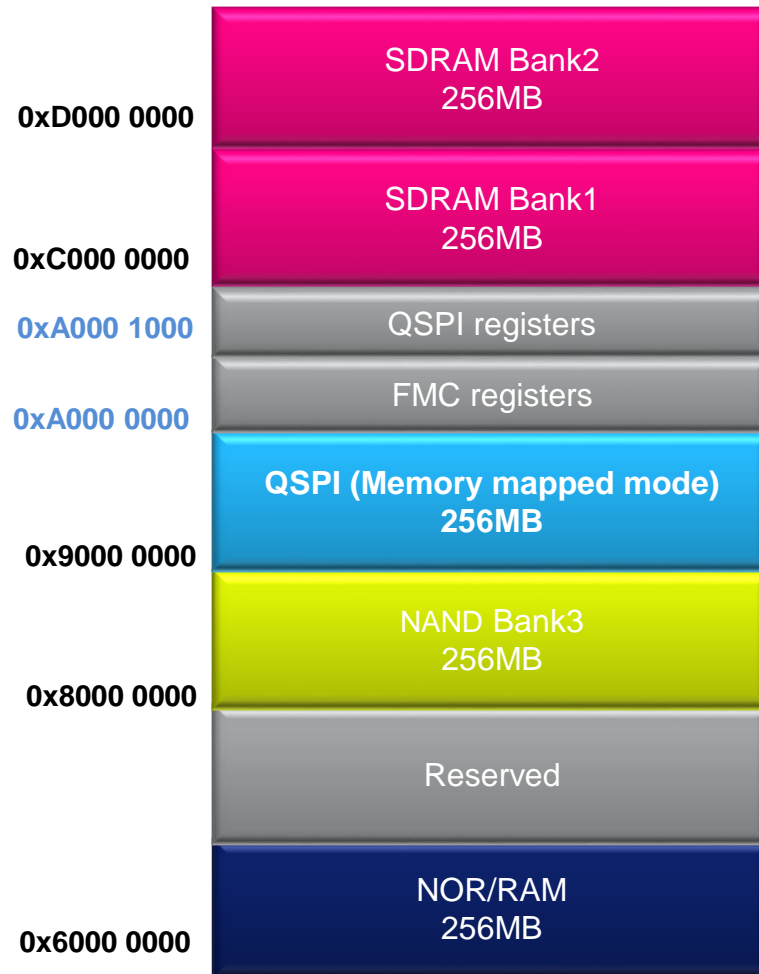




# STM32F756 – External memory mapping

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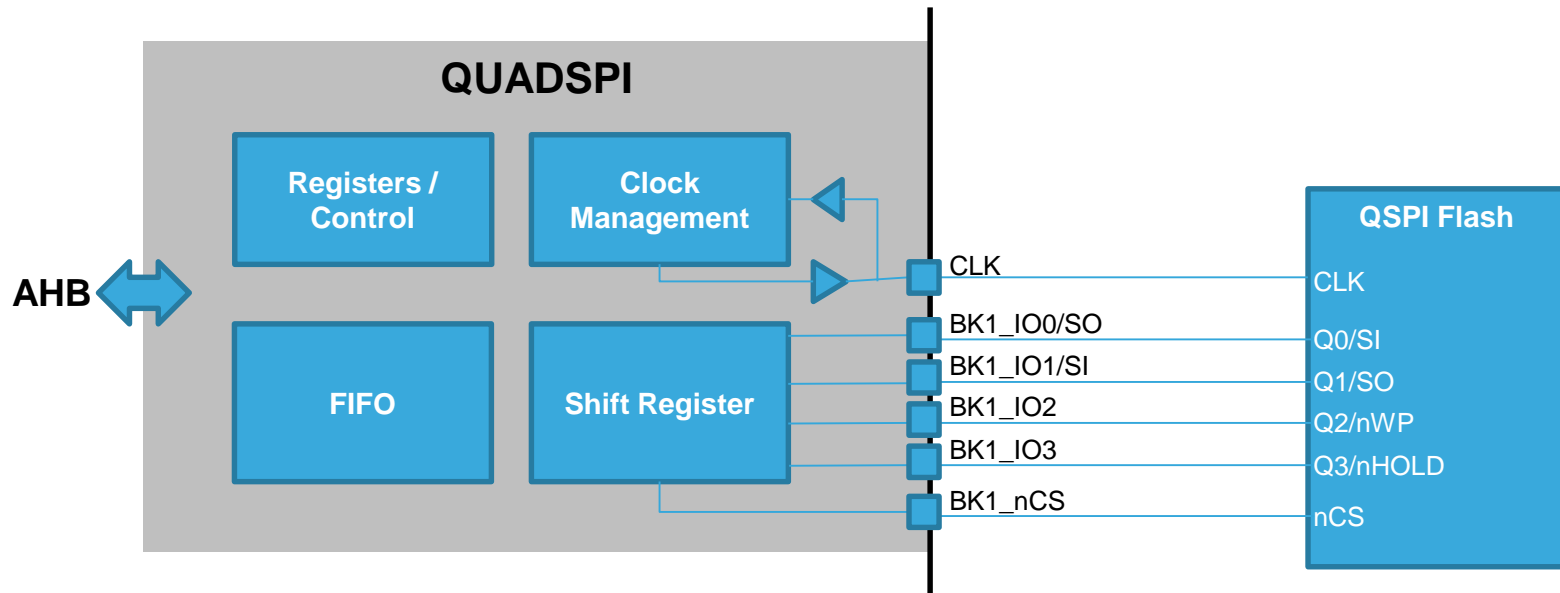
## External Memory mapping





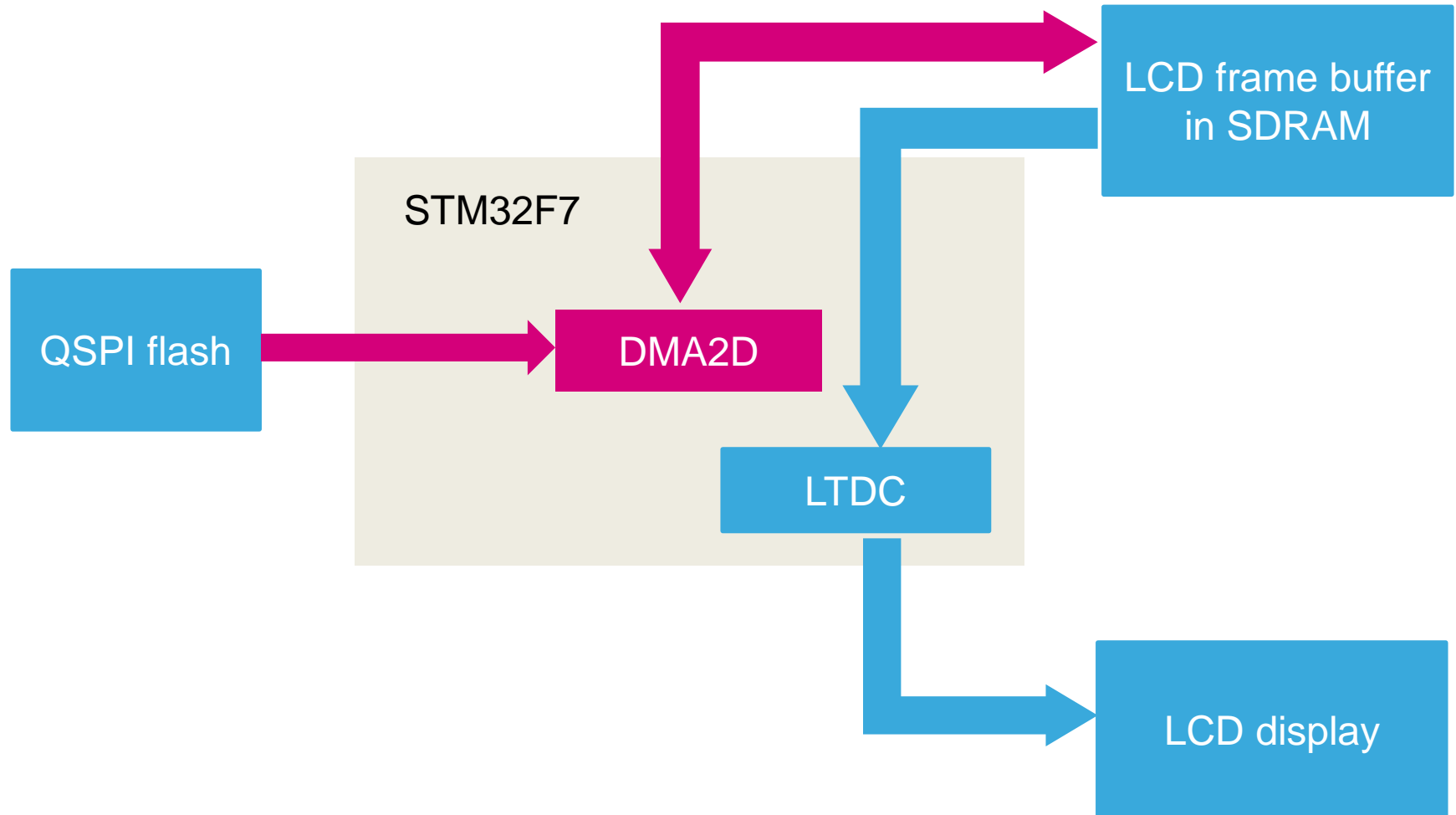
# QuadSPI

- Communication interface for single/dual/quad SPI flash memories



# QSPI graphical performance

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# QSPI graphical performance

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- To draw 4 images over each other → need of 4x do
  - Read QSPI image
  - Read SDRAM frame buffer
  - Blend together
  - Store back to frame buffer



# QSPI graphical performance

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- Total bytes read from QSPI

$$= X * Y * Bpp * NUM\_IMAGES = 480 * 272 * 2 * 4 = 1044480 \text{ bytes.}$$

- It's read in 21ms → **QSPI read is 46MB/s**
- At the same speed the DMA2D is able to blend images and SDRAM load& store to frame buffer
- LTDC is updating the TFT at 60Hz



# QSPI Main Features

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- Programmable data bus width
  - Single SPI mode (1-bit data bus)
  - Dual SPI mode (2-bit data bus)
  - Quad SPI mode (4-bit data bus)
  - Dual-Quad SPI mode (8-bit data bus)
- Three functional modes:
  - Indirect
  - Status-polling
  - Memory-mapped (read only)
- Increased data throughput
  - Dual-flash mode
  - Single Data Rate (SDR) and Double Data Rate (DDR) feature
- Integrated FIFO for reception and transmission
  - 8, 16, and 32-bit data accesses are allowed
  - DMA channel for indirect mode operations
- Low power feature
  - Advanced nCS (chip-select) signal handling
- Prefetch for both instruction and data
  - eXecute in Place (XiP)

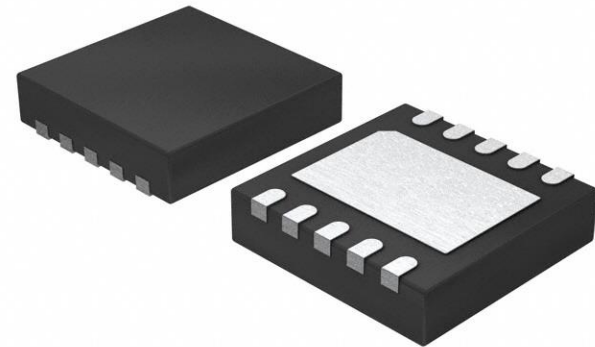
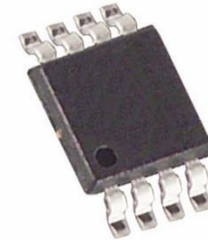


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- Integrated FIFO for reception and transmission
  - 8, 16, and 32-bit data accesses are allowed
  - DMA channel for indirect mode operations
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error
- Low power features
  - Advanced nCS (chip-select) signal handling
- Prefetch for both instruction and data
  - eXecute in Place (XiP)

- Low pin count
  - 6 pins used (nCS, CLK, IO1 – IO4)
  - Usually 8-pin or 16-pin packages
- Easier PCB design
- Small footprint
- Low cost memory solution
- Availability of both volatile (RAM) and non-volatile (ROM) memories
- Low access times
- High data throughput
- Growing amount of manufacturers
  - Spansion, Micron, Macronix, Everspin Technologies



# QSPI Performance overview

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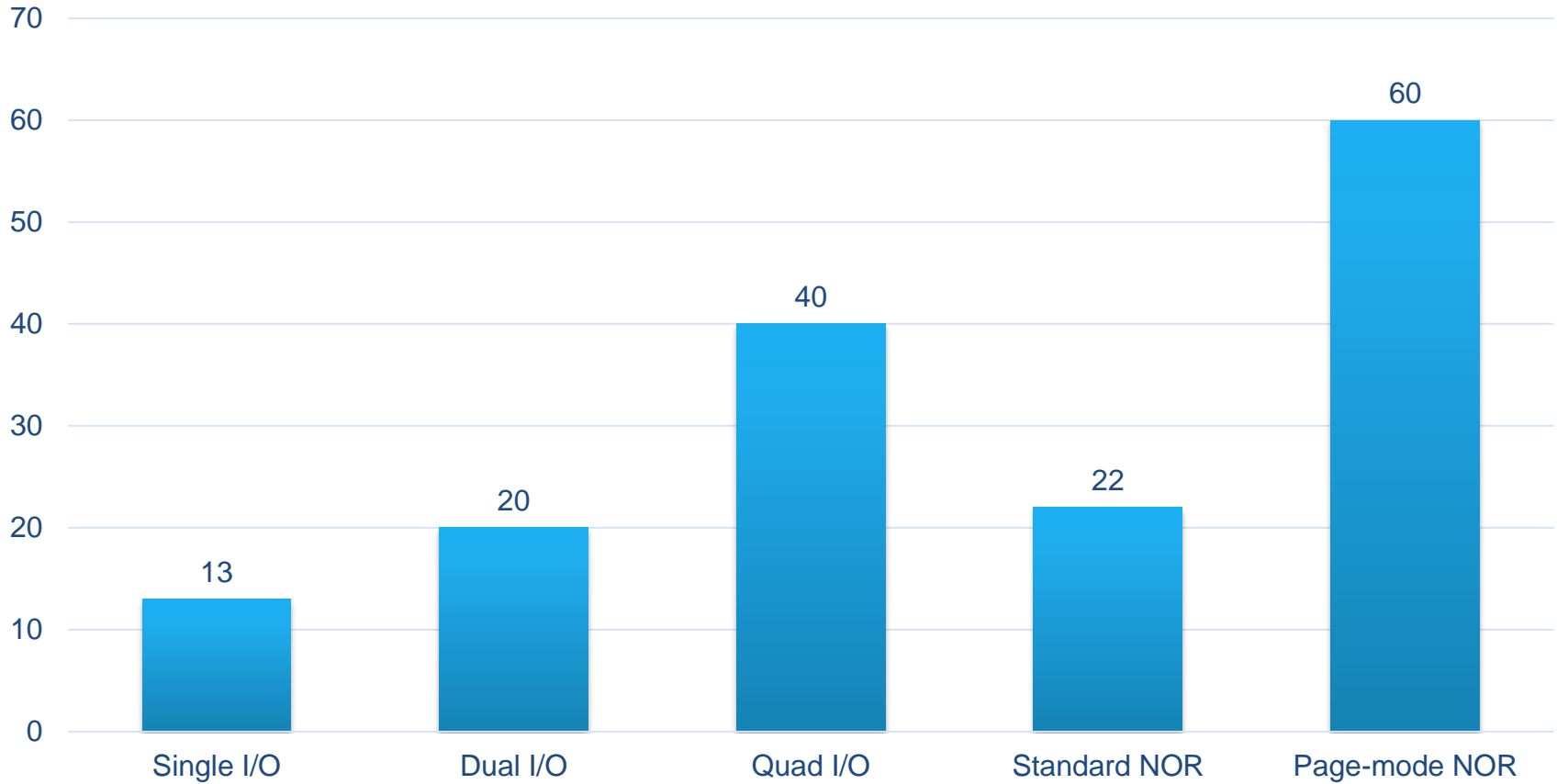
- Comparison of parallel and serial FLASH memories

INTERFACE (-)	MODE (-)	ACCESS TIME (ns)	CLOCK (MHz)	THROUGHPUT (MB/s)
Parallel	Byte (8)	90	11	11
Parallel	HalfWord (16)	90	11	22
Serial	Single I/O (1/1)	12.5	100	12.5
Serial	Dual I/O (2)	12.5	100	25
Serial	Quad I/O (4)	12.5	100	50

# Performance overview

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## Throughput comparison (MB/s)

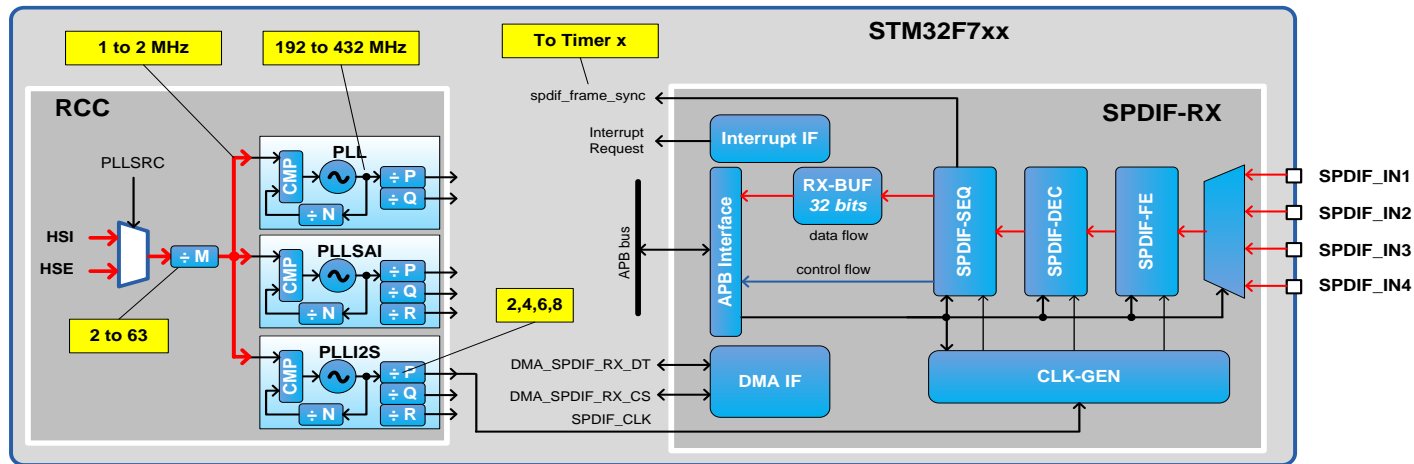




# Sony/Philips Digital InterFace receiver ( SPDIF-RX )

# SPDIF-RX Overview

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- Interface for receiving digitally encoded audio
- Up to Dolby Digital 5.1 channel audio decoding
- Widely used in consumer electronics
- Can be used for car multimedia and entertainment systems

The SPDIF-RX interface (**S**ony/**P**hilips **D**igital **I**nter**F**ace)

## Features List:

- Possibility to select the audio stream from 1 of the 4 inputs
- Stereo Stream **up to 192 kHz** supported
- Support Audio IEC-61937 (i.e. encoded audio stream such as Dolby Digital)
- The **SPDIF\_CLK frequency** must be **at least 11 times higher than the symbol rate** of the incoming audio stream
- The higher the SPDIF\_CLK frequency is, the more reliable the reception will be.

Sample Rate	Minimum SPDIF_CLK Frequency	Symbol Rate
48 kHz	33.8 MHz	3.072 MHz
96 kHz	67.6 MHz	6.144 MHz
192 kHz	135.2 MHz	12.288 MHz

# SPDIF-RX Benefits

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- Available metallic and optical physical link
- Decreasing the influence of noise on quality of audio signal
  - Eliminating the influence in case of optical link
- Automatic recovery from most frequented errors
  - Synchronization error
  - Data format error





# SPDIF-RX Clocking

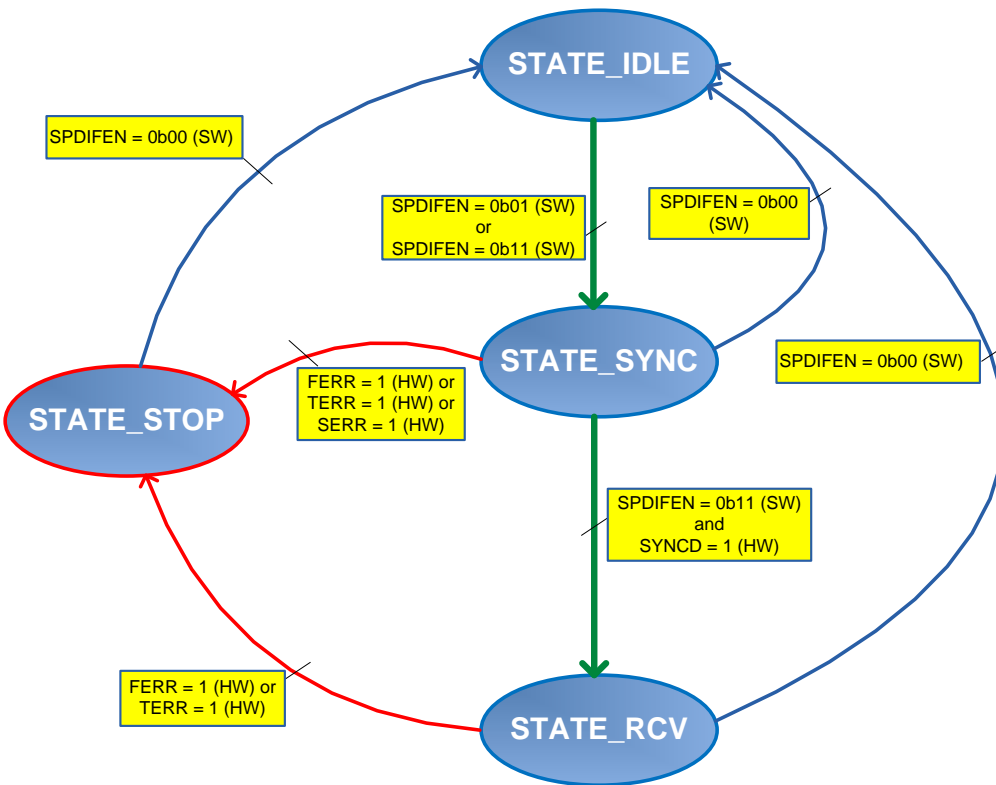
25

- The SPDIF\_CLK is used to sample the incoming S/PDIF stream
- The **SPDIF\_CLK frequency** must be **at least 11 times higher than the symbol rate** of the incoming audio stream
- The symbol rate is 64 times higher than the audio sampling rate (IEC 60958).

Sample Rate	Minimum SPDIF_CLK Frequency	Symbol Rate
48 kHz	33.8 MHz	3.072 MHz
96 kHz	67.6 MHz	6.144 MHz
192 kHz	135.2 MHz	12.288 MHz

- The higher the SPDIF\_CLK frequency is, the more reliable the reception will be.

The SPDIF-RX can transition between 4 STATES:



## STATE\_IDLE:

The peripheral is disabled (SPDIFEN = 0)

## STATE\_SYNC:

The peripheral is **synchronized** to the input stream, **thresholds are updated regularly**.

The user and channel status **can be read**.

The audio samples are not provided to receive buffer.

## STATE\_RCV:

The peripheral is **synchronized** to the input stream, **thresholds are updated regularly**.

The user and channel status **can be read**.

**Data are provided** to the receive buffer

## STATE\_STOP:

Error(s) occurred.

The user, channel status and data **reception is stopped**.

The user shall switch the peripheral to STATE\_IDLE

# Low Power Timer LPTIM

- Asynchronous running capability

- Ultra low power-consumption

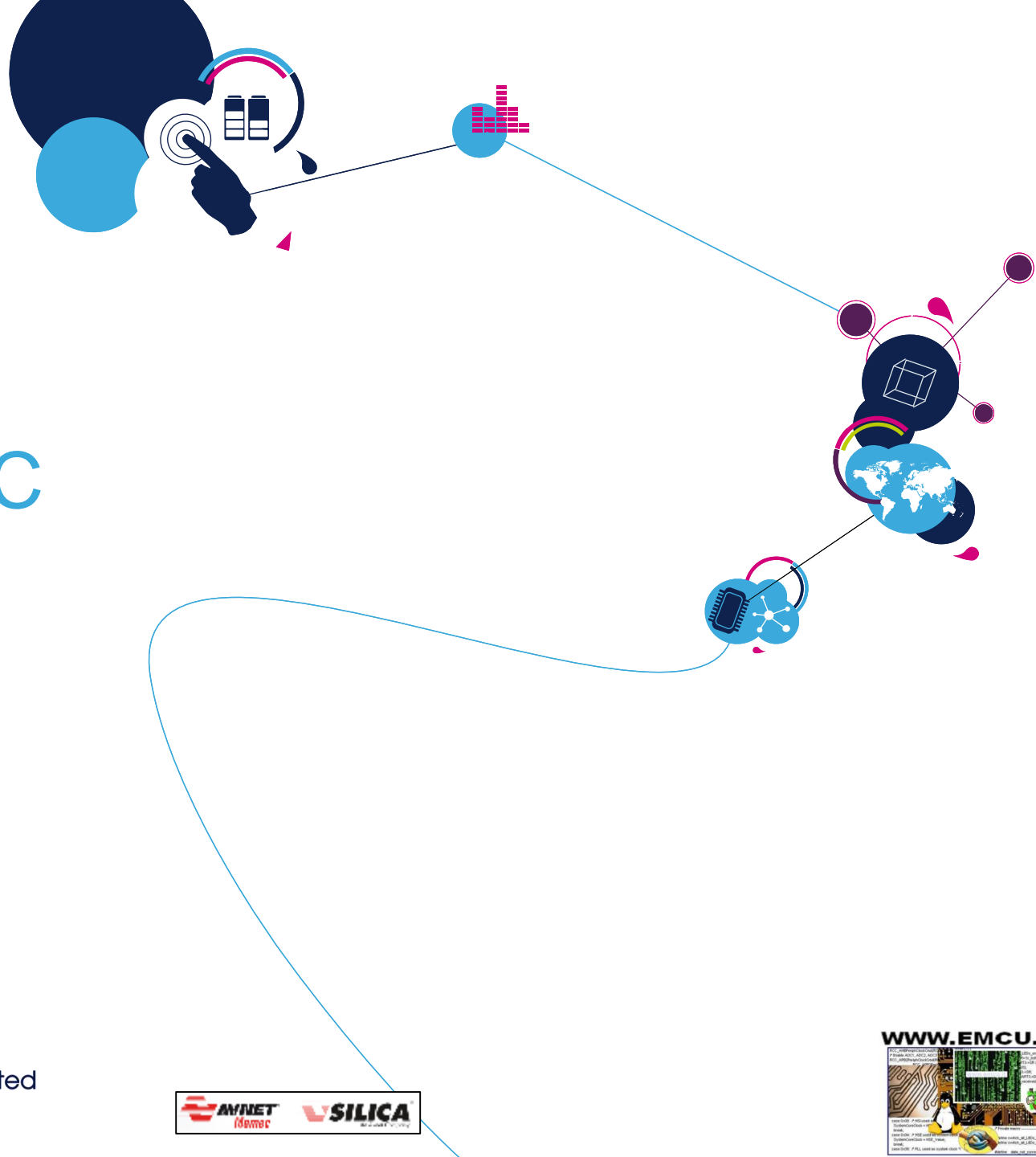


- Timeout function for wakeup from low power modes

- Up to 5 clock sources to achieve lowest power consumption
  - APB clock
  - LP oscillators: LSE, LSI
  - External clock
    - With configurable active edge: **Rising edge**, **Falling edge** and **Both edges**
    - When both edges configuration is chosen, an auxiliary clock source is needed with a frequency 4 times bigger, at least, than the external signal
- Operating modes
  - Continuous mode: free running mode; many counter overruns are possible
  - One Shot mode: Counter stops counting when the overrun value is reached
  - PWM mode: Generates PWM signal

- Can be Asynchronous
  - No internal clock needed
  - Clocked by external clock
- Designed for low power applications
  - Running in any low power mode (STOP, SLEEP, ...)
  - Can generate up to 6 interrupts, each int. can wake up the MCU
- Used case:
  - Wake up the MCU after 600 pulses counted on external clock pin
    - Configure the LPTIM to generate an interrupt when counter value reaches 600
    - Set the MCU to STOP mode
    - Wait for the interrupt in STOP mode and save a lot of energy...

# HDMI-CEC



# HDMI-CEC v2 Controller Overview

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- Fully compatible with HDMI-CEC v1.3a standard
  - Electrical specifications
  - Messages (Frame formats, bits timings...)
  - Full Arbitration: Signal Free Time (SFT), Header Arbitration
- Consumer electronics Control (CEC)
  - Allows to control TVs, DVDs, Set-Top Boxes via HDMI connector
  - Doesn't provide video or audio signal

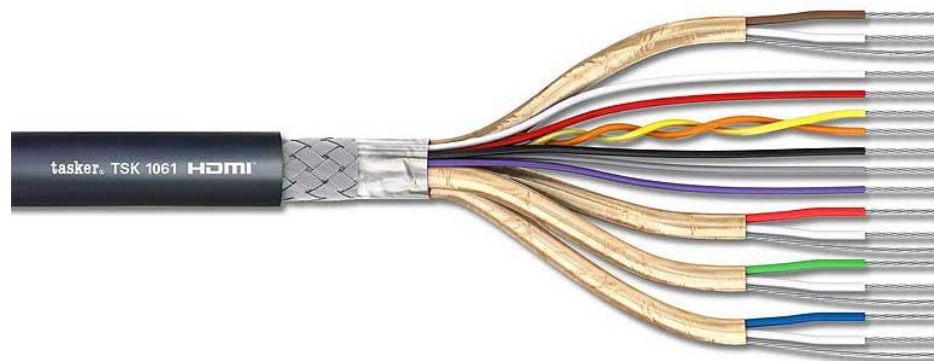




# HDMI-CEC v2 Controller Features

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- 32kHz kernel running from LSE or HSI/244
- Works in STOP mode
  - Can generate an interrupt to wake up the MCU
- Supports listen mode
- Configurable error handling with selectable extended timing tolerance
- Selectable signal free time (SFT) before transmission – HW or SW



# HDMI-CEC v2 Controller Benefits

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- Mandatory for many of the consumer electronics applications
- In combination with **SPDIF-RX** and **SAI** provides wide range of possible multimedia application



# Need more info ?

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For more info contact:

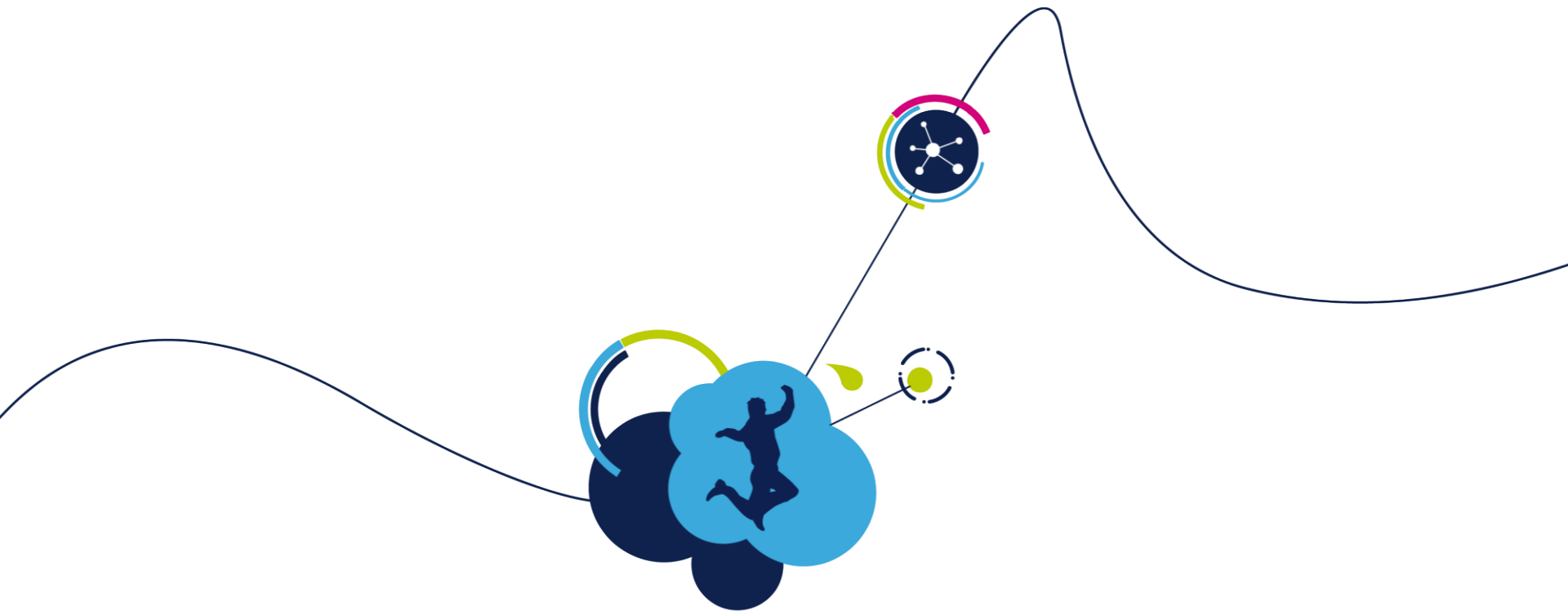
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(Digital FAE for STM - MCU, WireLess (IoT), MEMS, PLM, etc)

**[roberto.rossetti@avnet.eu](mailto:roberto.rossetti@avnet.eu)**

(B.D.M.)





# Thank you

[www.st.com/stm32](http://www.st.com/stm32)