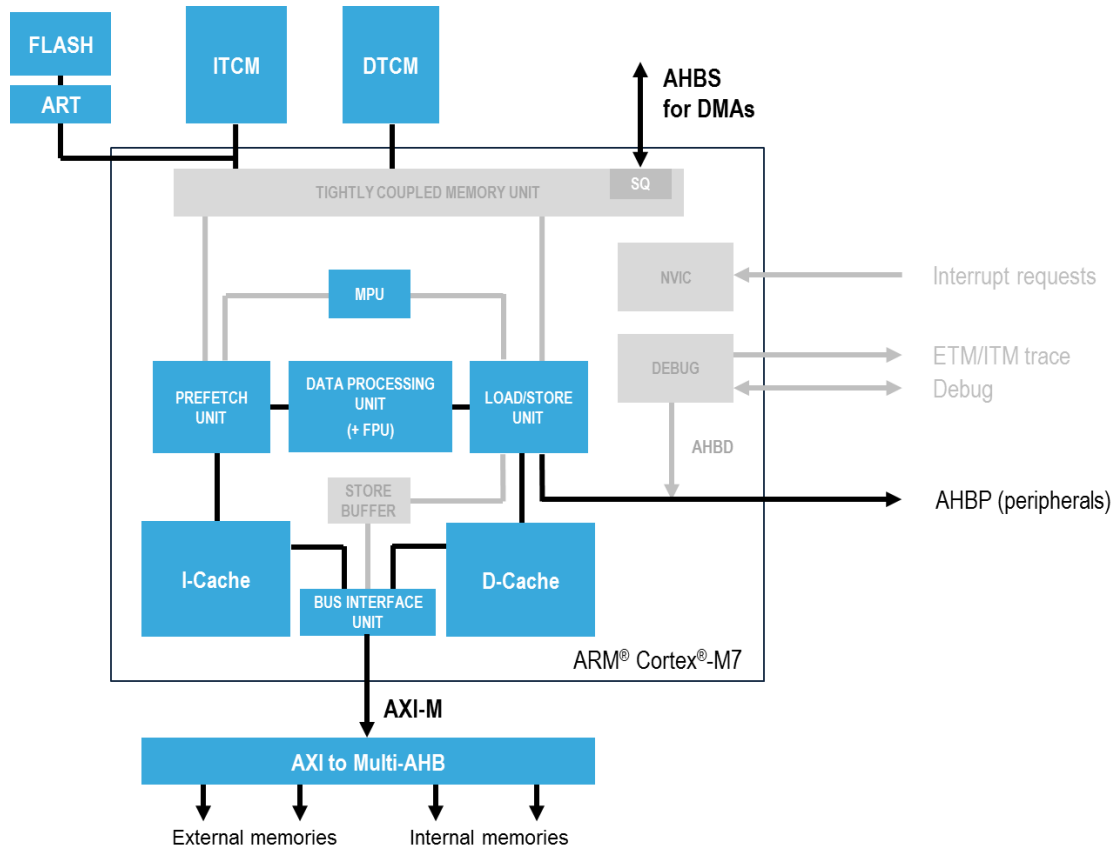


STM32F7 dictionary



Internal memory mapping

Reserved	0x2005 0000
SRAM2(16 KB)	0x2004 C000
SRAM1(240 KB)	0x2001 0000
DTCM (64 KB)	0x2000 0000
Reserved	0x1FFF 0020
Option Bytes	0x1FFF 0000
Reserved	0x1FF0 EDC0
System memory on AXIM	0x1FF0 0000
Reserved	0x0820 0000
Flash memory on AXIM interface	0x0800 0000
Reserved	0x0030 0000
Flash memory on ITCM interface	0x0020 0000
Reserved	0x0011 0000
System memory on ITCM	0x0010 0000
Reserved	0x0000 4000
ITCM RAM	0x0000 0000

External memory mapping

SDRAM Bank2	0xD000 0000
SDRAM Bank1	0xC000 0000
QSPI registers	0xA000 1000
FMC registers	0xA000 0000
NAND Bank3	0x9000 0000
Reserved	0x8000 0000
NOR/RAM 256MB	0x6000 0000

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MPU Cache Attributes



TEX	C	B	Description	Memory type
000	0	0	Strongly Ordered	Strongly Ordered and shared
000	0	1	Shared Device	Device
000	1	0	Cacheable, write-through, no write allocate	Normal
000	1	1	Cacheable write-back, no write allocate	Normal
001	1	1	Cacheable write-back; write and read allocate	Normal
010	0	0	Non-shared device	Device

Default STM32F7 Memory Cache Attributes

Address	Name	Memory Type	XN?	Cache	Description
0x0000 0000 0x1FFF FFFF	Code	Normal		WT	Typically ROM or flash memory. Memory required from address 0x0 to support the vector table for system boot code on reset
0x2000 0000 0x3FFF FFFF	SRAM	Normal	-	WBWA	SRAM region typically used for on-chip RAM
0x4000 0000 0x5FFF FFFF	Peripheral	Device	XN	-	On chip peripheral address space
0x8000 0000 0x9FFF FFFF	RAM	Normal	-	WT	Memory with write-through cache attribute
0xC000 0000 0xDFFF FFFF	Device	Device, non-shareable	XN	-	Non-shared device space

Cache terminology

Cache line → Smallest cache portion of data.

Cache hit → Lookup finds desired entry cache.

Cache miss → Lookup does not find desired entry in cache.

Cache allocation → Put a new entry (cache line) into the cache. Occurs on cache miss.

Write-allocate → allocate on reads and writes

Read allocate → allocate on reads only

Line fill → Read request on the bus for an entire cache-line. This line, once available, will be subsequently be allocated to cache

Eviction → Write of an entire cache line on the bus. Occurs when a dirty cache line is replaced by a new cache line

Because it is dirty, the new data needs to be written back to physical memory.

Write-back → Write data to cache only marking appropriate cache lines 'dirty'. On eviction, its data are written to next level memory.

Write through → Write data to both cache and next level memory at the same time. Lines can never be 'dirty'

ALU = Arithmetic Logic Unit

SIMD = Single instruction, multiple data

MPU = Memory Protection Unit

MAC = multiply–accumulate operation

LSU = load store unit

DPU = data processing unit

DTCM & ITCM = The memory system includes support for the connection of local Tightly Coupled Memory called ITCM (16K) and DTCM (64K)

STB = store buffer

BUI = Bus Unit Interface

TCU = Tightly-Coupled interface Unit

EPPB = External Private Peripheral Bus-The APB External PPB

Superscalar architecture first appeared on Intel Pentium 5 in 1993 => it means it is able to process multiple instructions in parallel (in our case, Cortex M7, up to 2, that's why **dual-issue**)

Coremark® is now industry standard of CPU benchmarking.

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