Power 'n Motors

Critical aspects in power applications
design, proper component selection
& experimental results

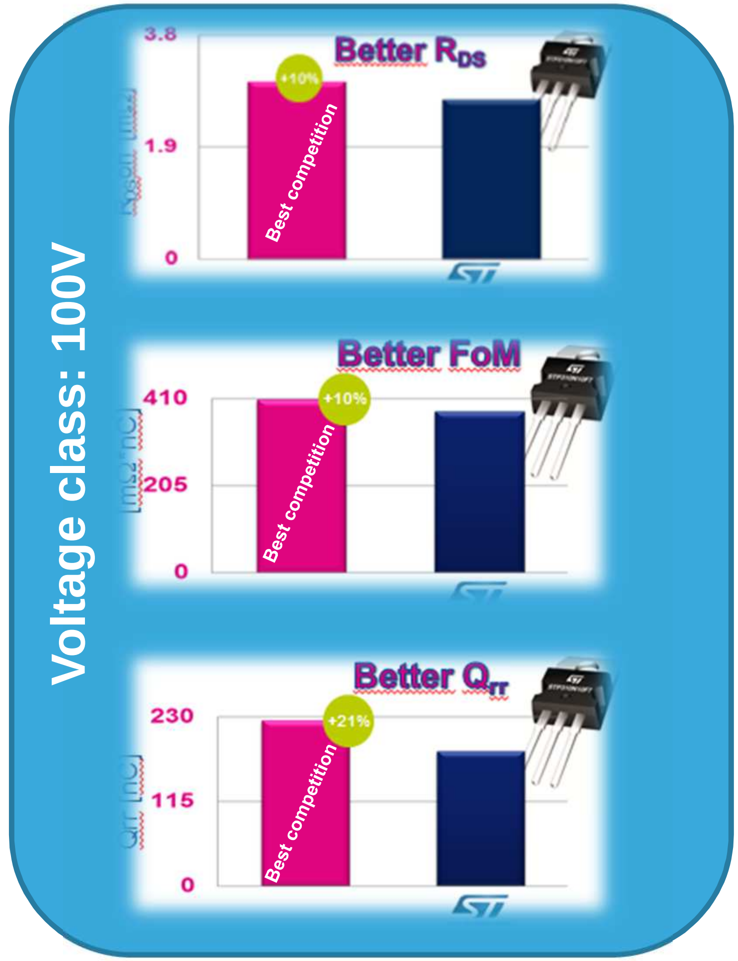
STripFET family overview

Broad portfolio of LV MOSFETs

- ❑ **STripFET H6/F6:**
  - 30V; 40V; 55V; 60V; 70V; 80V
- ❑ **STripFET H7/F7:**
  - 30V; 40V; 60V; 80V; 100V; 120V; 150V

Best in class LV MOSFETs @100V

- ❑ **Lowest R_{DS}(on) in high power packages i.e. TO-220 & H^2PAK**
- ❑ **Best parasitic diode performances for higher efficiency and lowest EMI**
- ❑ **Optimal capacitance C_{rss}/C_{iss} ratio for lowest EMI**



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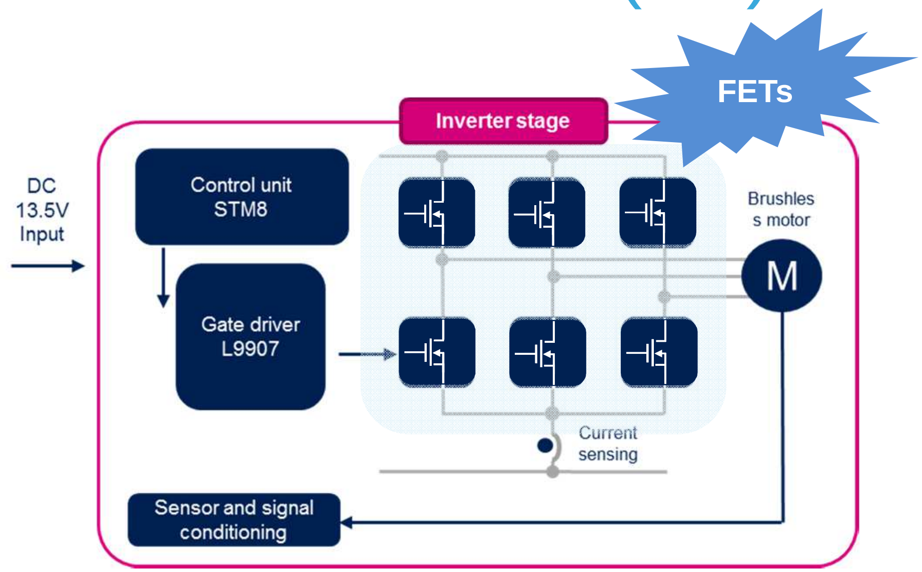
BLDC motor (1/2)

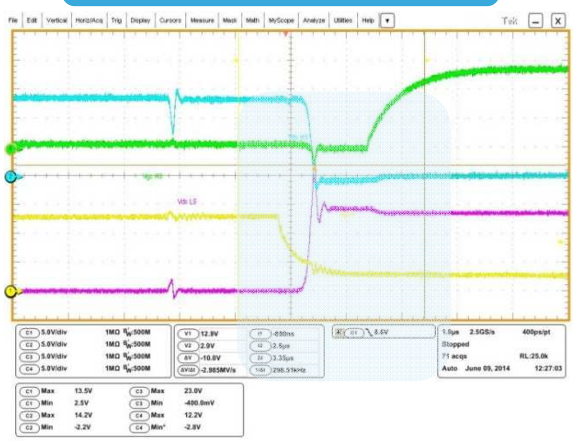
Automotive motor control

F7
40V
NEW

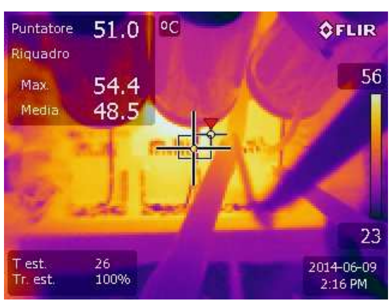
- **STripFET F7 technology** does show excellent R_{DSon} perfomances, aligned with the best competitors
- Optimized Q_{rr} and intrinsic capacitances for **improved EMI performances**



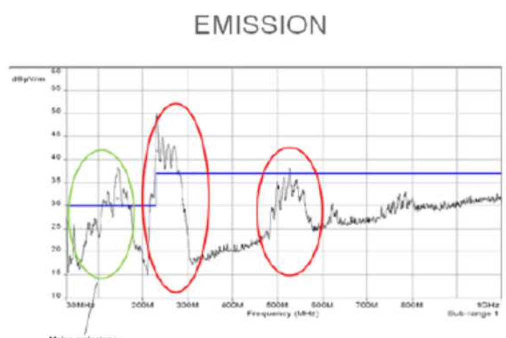
Turn-off waveforms



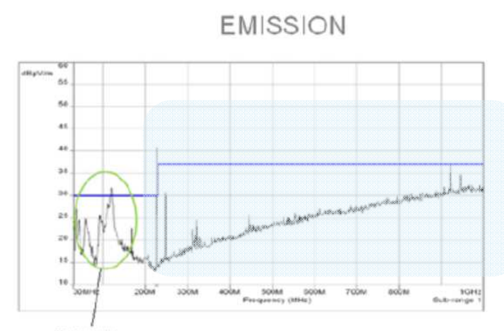
Thermal capture



F7 vs. old technology : EMI performance comparison



Previous tech.



F7 technology

Let’s have a look in additional details…..

The aim of the benchmark

- The aim of benchmark is to compare the performance of various types of 40V MOSFETs in a typical motor control application

- The performances compared in:
  - Switching performance
    - Voltage ringing on the gates during MOSFET turn-on and turn-off
  - EMI conducted emissions in frequency range according to CISPR-25 specification measured on the supply line of the motor control power stage
  - Thermal performance of the MOSFET:
    - Measuring temperature on the MOSFET case. Lower case temperature shows lower power losses thus higher efficiency of the application

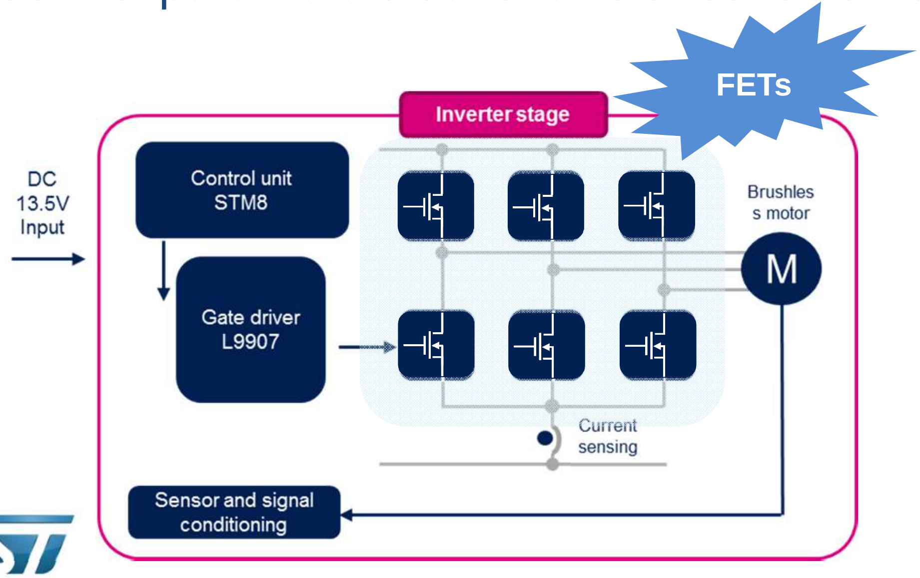
- As power stage used 3 phase inverter evaluation board L9906 version 2.3 (parasitic inductance optimized version with SMD footprints for main switches)

  3 phase inverter for high current and low voltage application assembled with driver **L9907**

- As motor used high power high speed 2 pole-pairs motor

- Driving control method is scalar (six-step) method; driving signals provided from STM8 universal board

- Control parameters set over GUI console from an PC



Test Conditions

- Switching frequency; F_{sw} = 15.6 kHz
- PWM duty cycle; D = 50%
- Supply voltage; V_{in} = 13.5V
- Gate voltage; V_{gate} ~ 12V
- Ambient temperature; T_{amb} = 25 ˚C
- OUT phase current I_{phase} = ~ 60A
- Output motor power P ~280W
- Motor RPM ~ 5600

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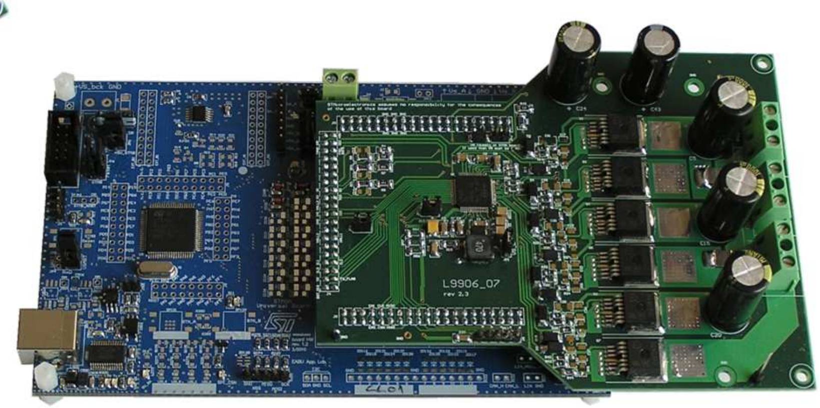
L9906 evaluation board version 2.3

- Updated version of L9906 evaluation board with H2PAK-6 footprint for power MOSFETs



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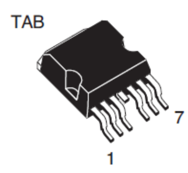
MOSFET type used in benchmark

- **STH410N4F7 — 40V 1.1mΩ power MOSFET**
- Competitor 1 — 40V 2.1mΩ power MOSFET
- Competitor 2 — 40V 1.5mΩ power MOSFET
- Competitor 3 — 40V 1.3mΩ power MOSFET
- Competitor 4 — 40V 0.55mΩ power MOSFET
- Competitor 5 — 40V 3.0mΩ power MOSFET
- Competitor 6 — 40V 1.8mΩ power MOSFET



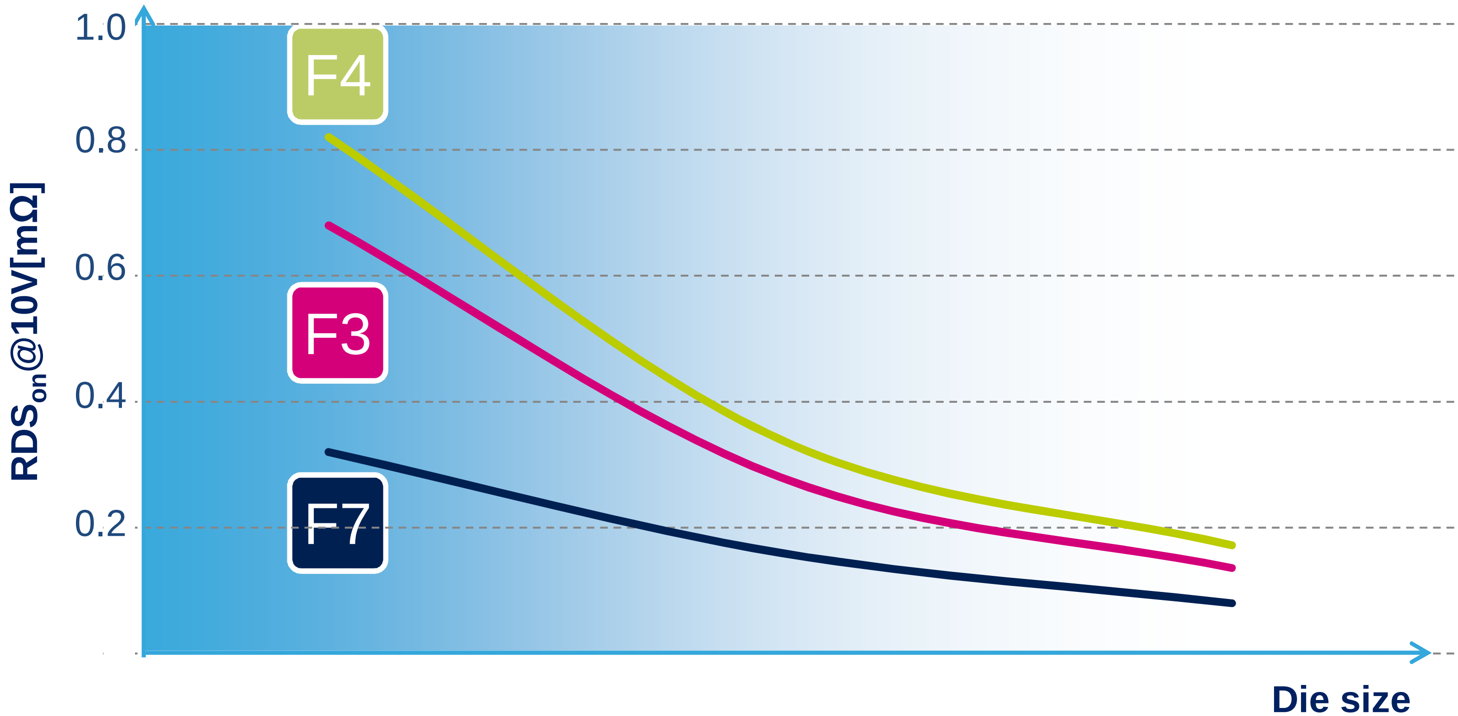
H^2PAK-6

STripFET^{TM} VII DeepGATE^{TM} **F7 Series**

Technology Capability in terms of $R_{DS(ON)}$

BV_{DSS}=100V

F7 vs ST previous Generations



More than 50% $R_{DS(ON)}$ reduction vs ST Planar F3 Techno

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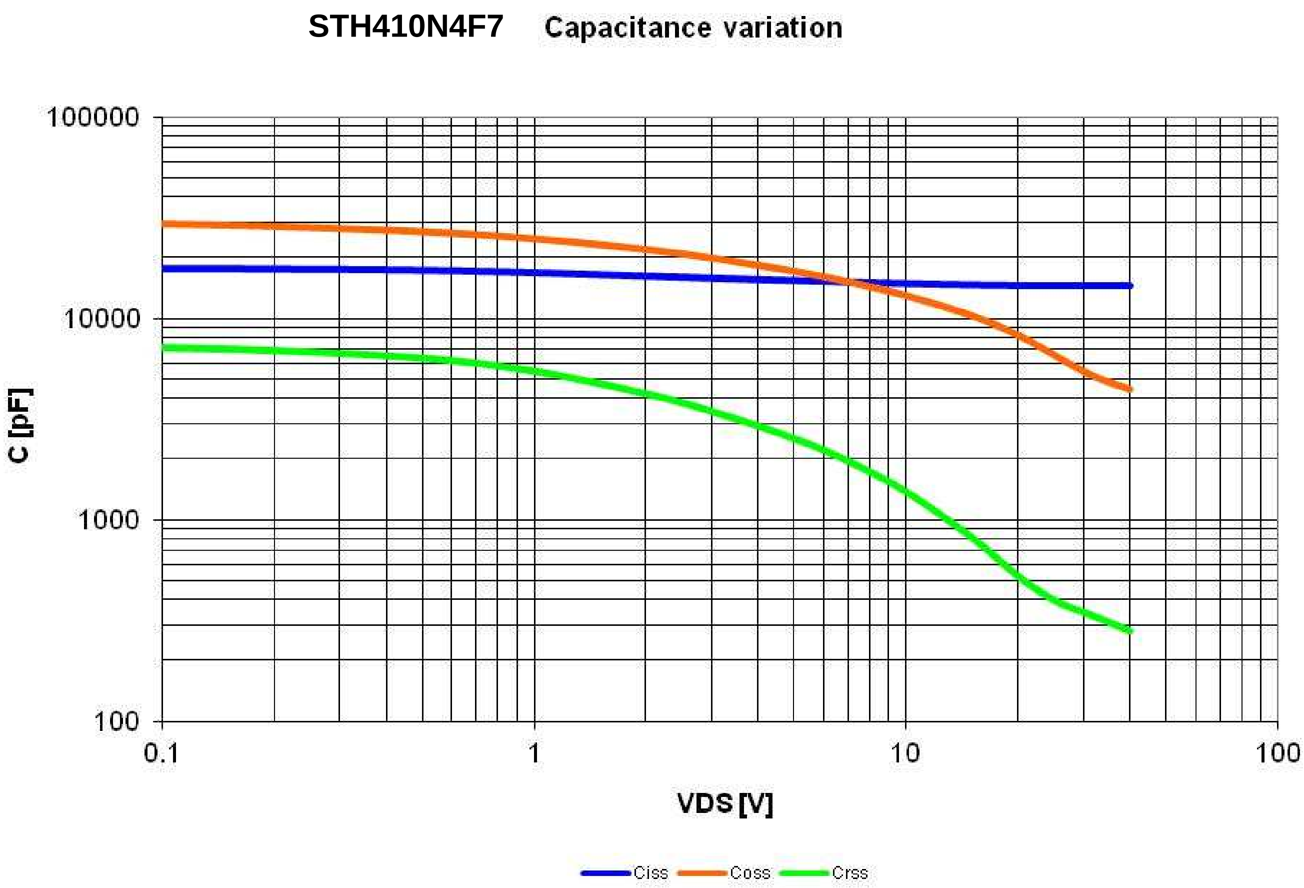
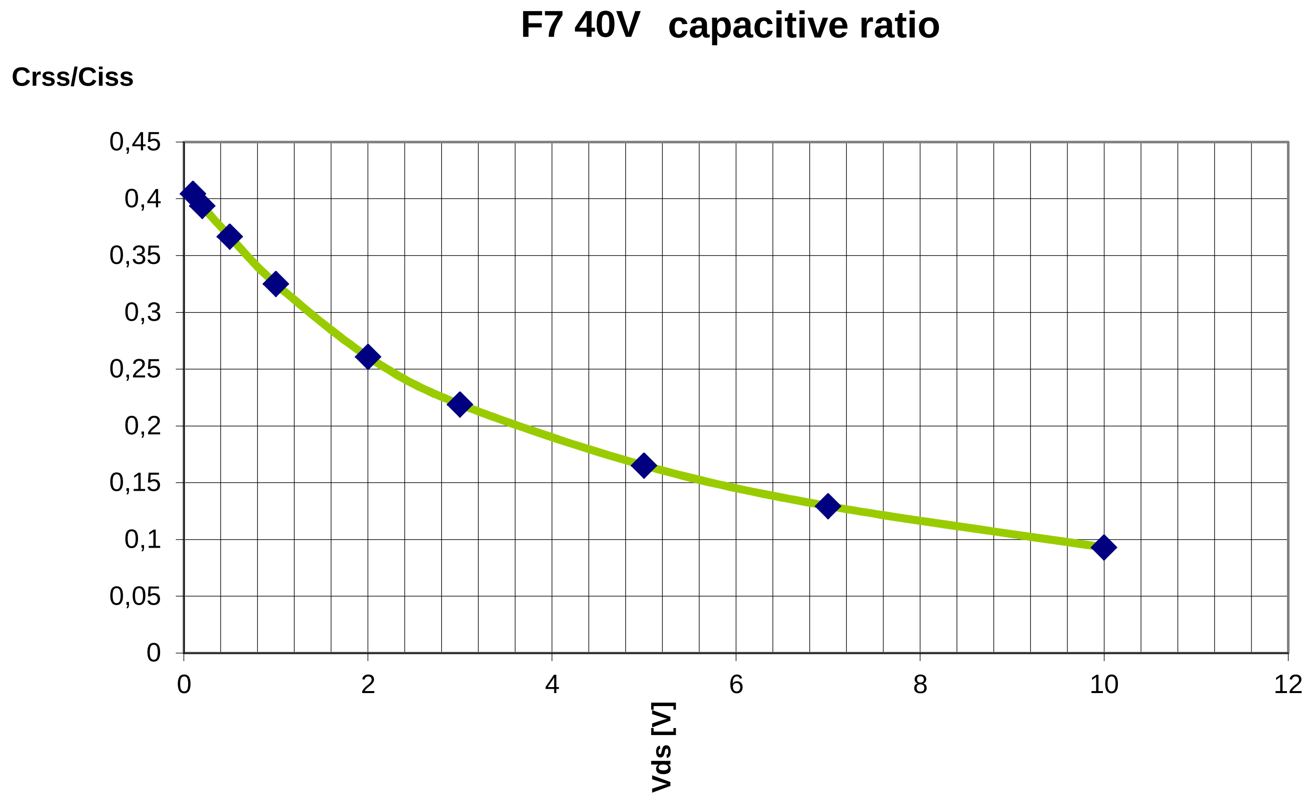
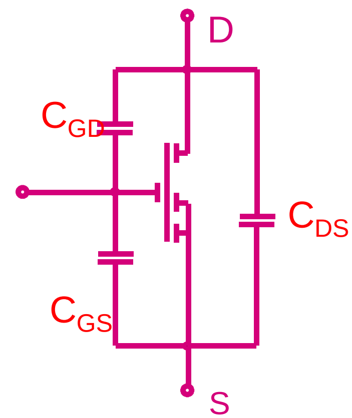
Capacitance values



C_{rss}/C_{iss} capacitance ratio





$C_{iss} = C_{GD} + C_{GS}$
$C_{oss} = C_{DS} + C_{GD}$
$C_{rss} = C_{GD}$

- Crss (reverse transfer capacitance) / Ciss (input capacitance) ratio. The variation is minimum and very smooth over V_{DS} variation
- This is thanks to the lower Miller capacitance with respect to the input capacitance

STH 410N4F7 device parameters

	BV_{dss} [V] @250µA	V_{th} [V] @250µA	V_{sd} [mV] @50mA	$R_{on\ typ}$ @10V /30A [mΩ]	R_g[Ω]	C_{iss} [pF] @10V	C_{rss} [pF] @10V	C_{oss} [pF] @10V
STH410N4F7	**44.35**	**4.2**	**558**	**0.9**	**3.7**	**14700**	**1120**	**11700**

Driver features:

4.5.6 MOSFET drivers

The device is operated in the specified operating range, unless otherwise specified (V_{CC} = 3.20 V to 5.25 V, VB = 6 V to 54 V, T_j = -40 °C to 150 °C).

Table 14. MOSFET drivers electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{GS}(L)	Low level output voltage	VGx-VSx @ I= 50 mA	-	100	250	mV
V_{GS}(H)	High level output voltage	VGx-VSx @ I= -5mA	7.5	-	15	V
I_{Gxx_1}	Turn-on/off current with GCR = 1 kΩ	IG_1,IG_0 = 11 100% Imax	450	600	750	mA
		IG_1,IG_0 = 10 75% Imax	337	450	563	mA
		IG_1,IG_0 = 01 50% Imax	225	300	375	mA
		IG_1,IG_0 = 00 25% Imax	112	150	188	mA
I_{Gxx_2}	Turn-on/off current with GCR = 6 kΩ	IG_1,IG_0 = 11 100% Imax	75	100	125	mA
		IG_1,IG_0 = 10 75% Imax	56	75	94	mA
		IG_1,IG_0 = 01 50% Imax	37	50	63	mA
		IG_1,IG_0 = 00 25% Imax	18	25	32	mA
I_{SLSx}(1)	Low side driver SLS output current	GCR = 1 kΩ , PWM signals low	-	-	3.3	mA
I_{SHSx}(1)	High side driver SHS output current	GCR = 1 kΩ , PWM signals low	-	-	3.3	mA
GCR_STG	Gate driver over current protection	-	-	-	880	Ω
GCR_OL	Gate driver under current protection	-	22			kΩ

Maximum gate current for turning ON/OFF the FETs

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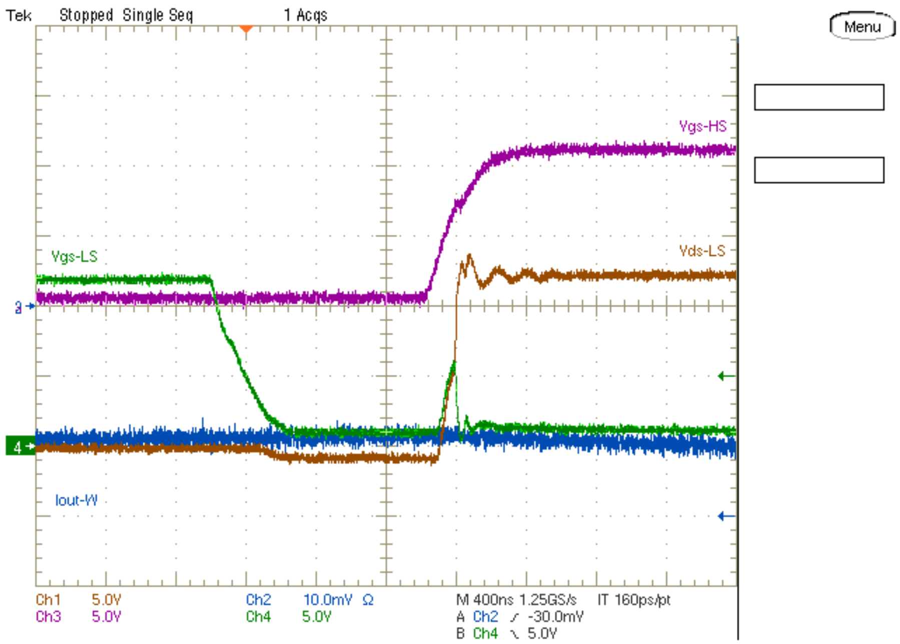
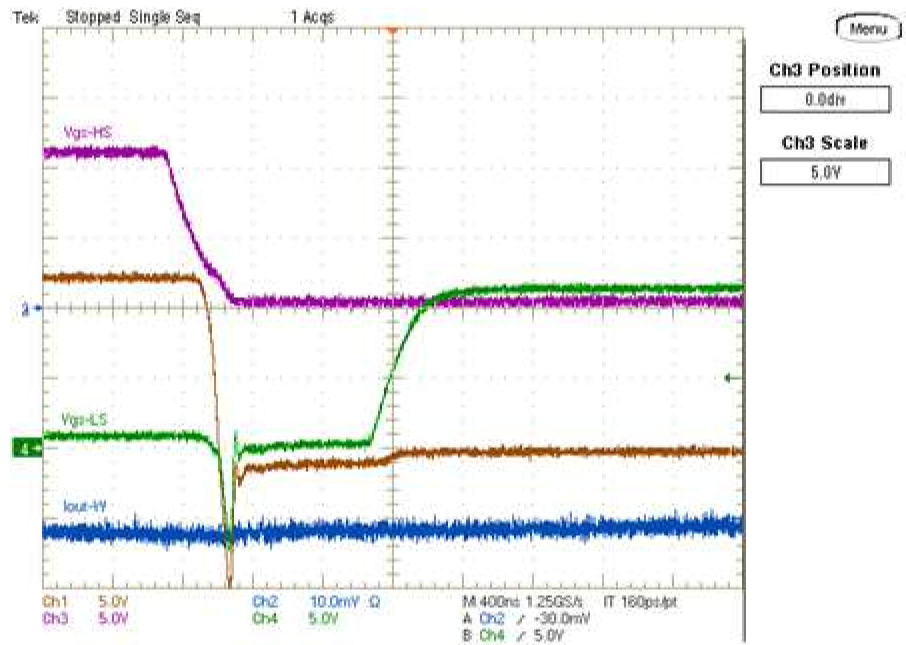
STH410N4F7 – HS Ton/ Toff
LS V_{GS} +HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF



1 LS drain-source voltage

2 Phase current

3 HS gate-source voltage

4 LS gate-source voltage

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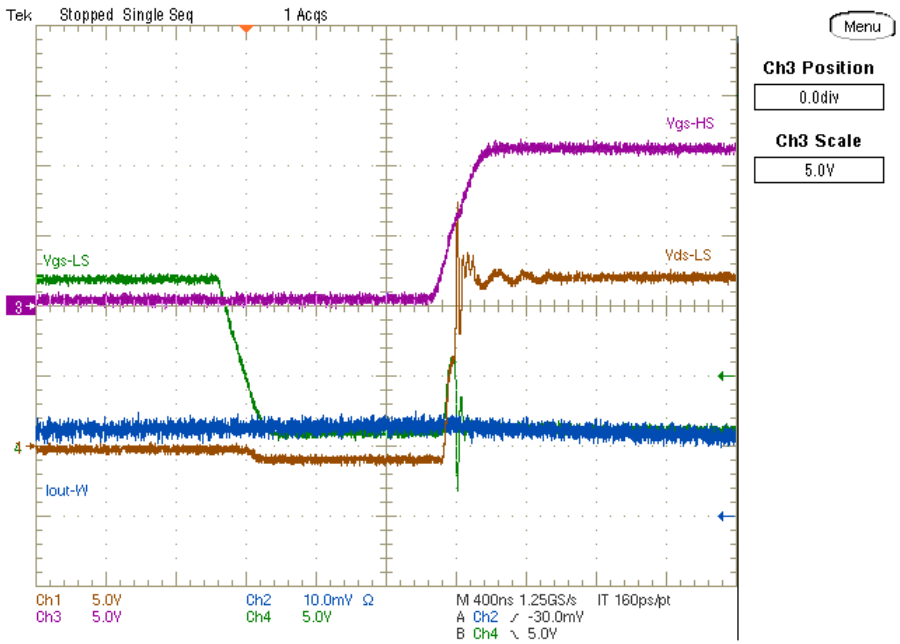
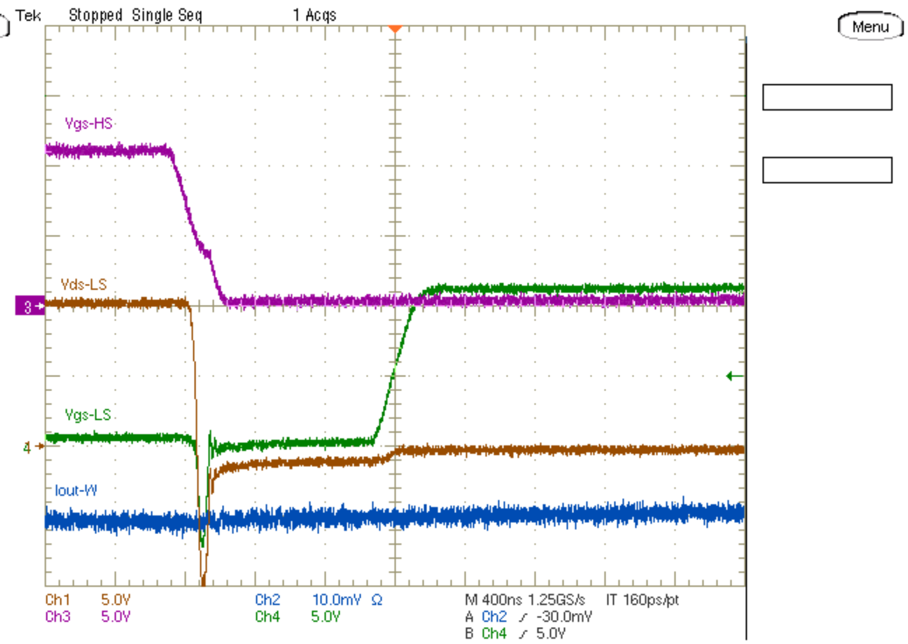
Competitor_1 – HS Ton/ Toff
LS V_{GS}+HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF



1. LS drain-source voltage
2. Phase current
3. HS gate-source voltage
4. LS gate-source voltage

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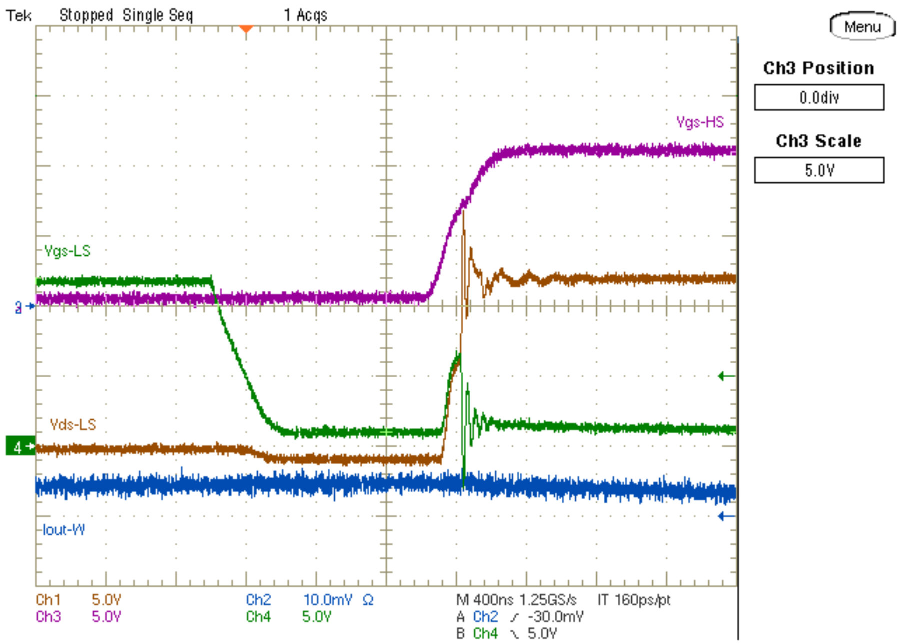
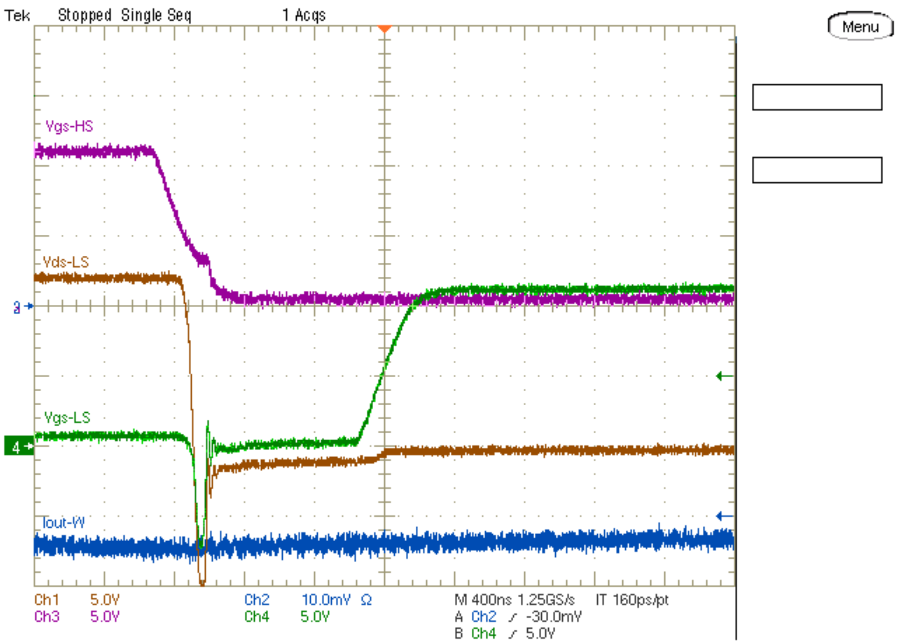
Competitor_2 – HS Ton/ Toff LS V_{GS}+HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF

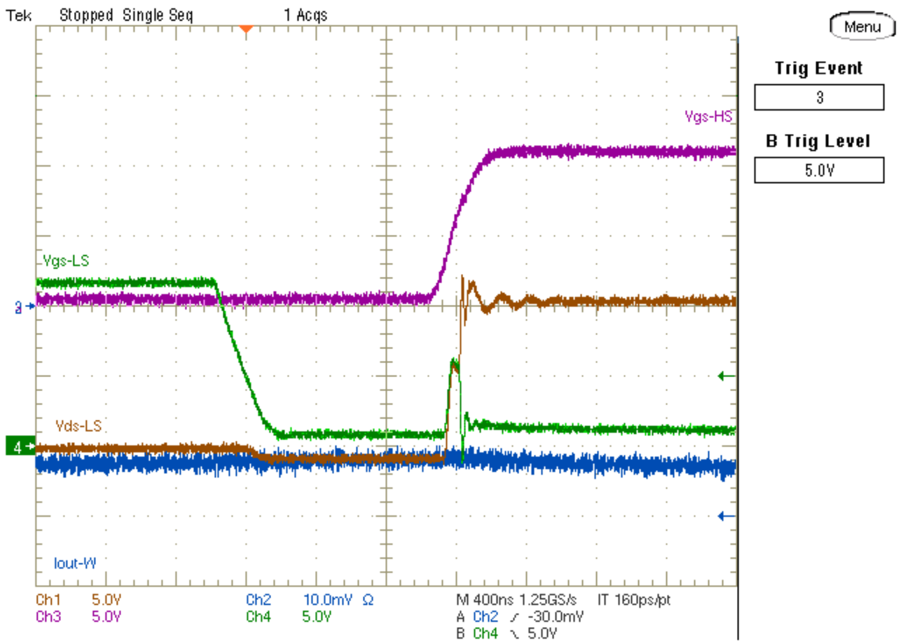


1 LS drain-source voltage
2 Phase current
3 HS gate-source voltage
4 LS gate-source voltage

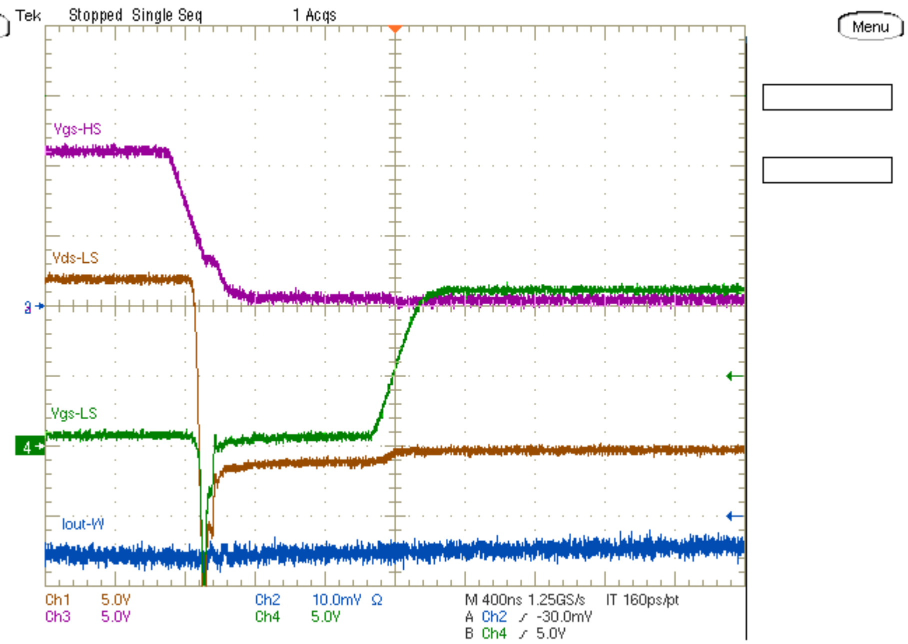
Competitor_3 – HS Ton/ Toff LS V_{GS}+HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF



1 LS drain-source voltage

2 Phase current

3 HS gate-source voltage

4 LS gate-source voltage

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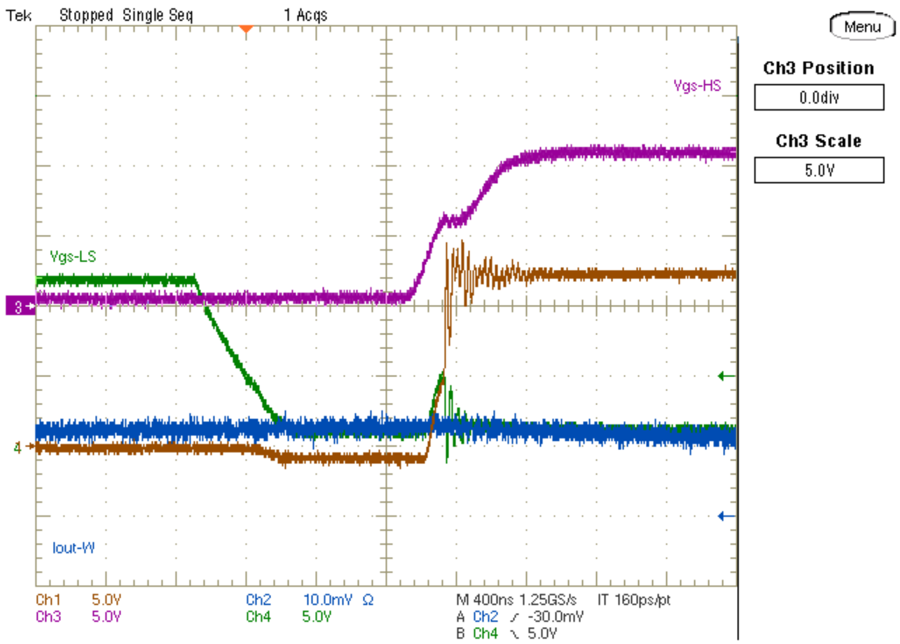
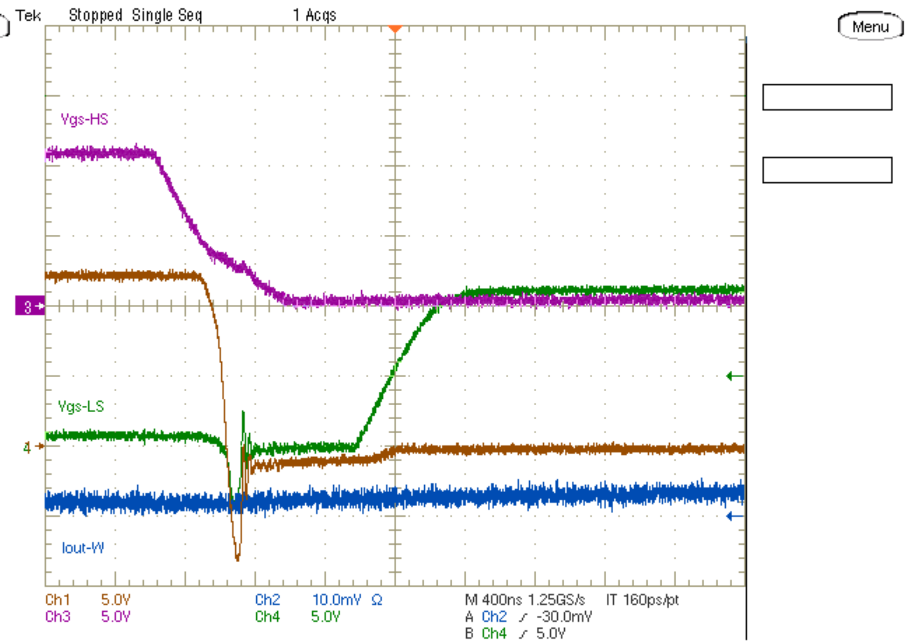
Competitor_4 – HS Ton/ Toff LS V_{GS} +HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF



1 LS drain-source voltage

2 Phase current

3 HS gate-source voltage

4 LS gate-source voltage

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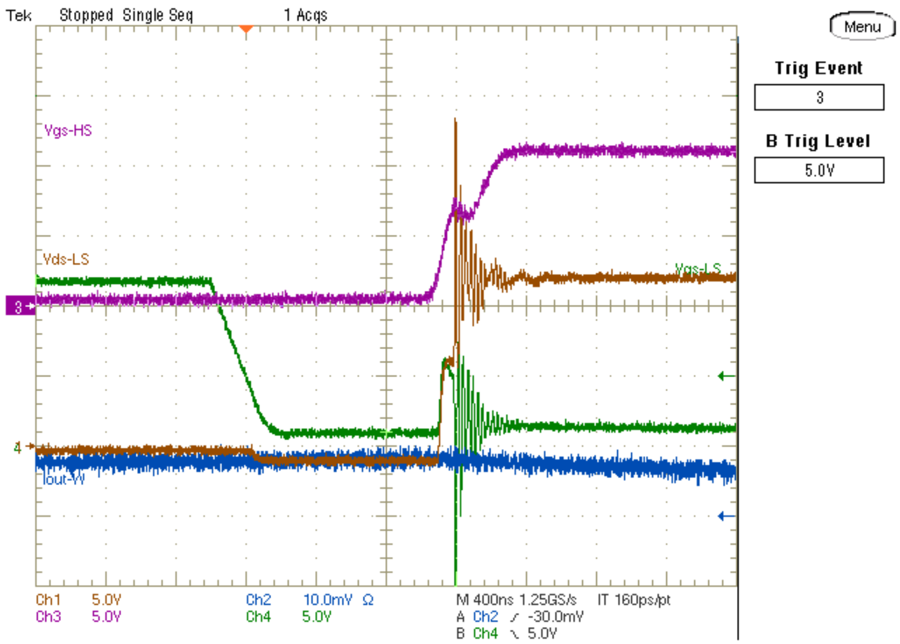
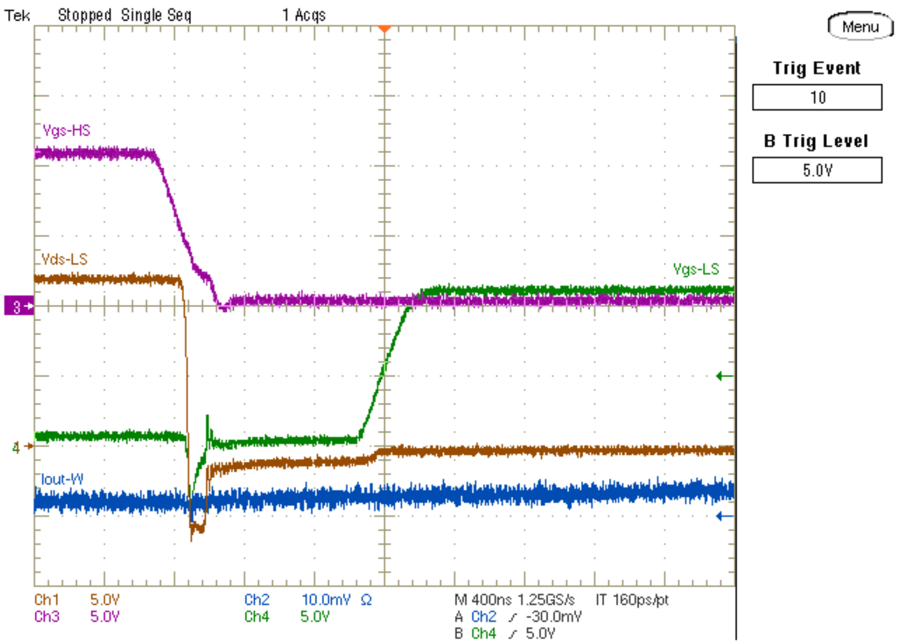
Competitor_5 – HS Ton/ Toff LS V_{GS}+HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF

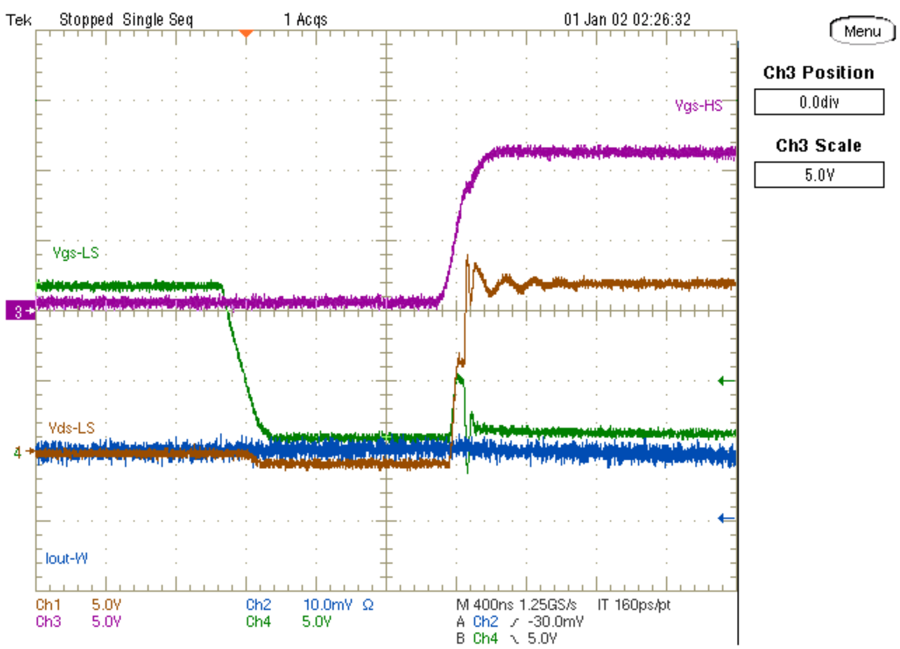


1 LS drain-source voltage
2 Phase current
3 HS gate-source voltage
4 LS gate-source voltage

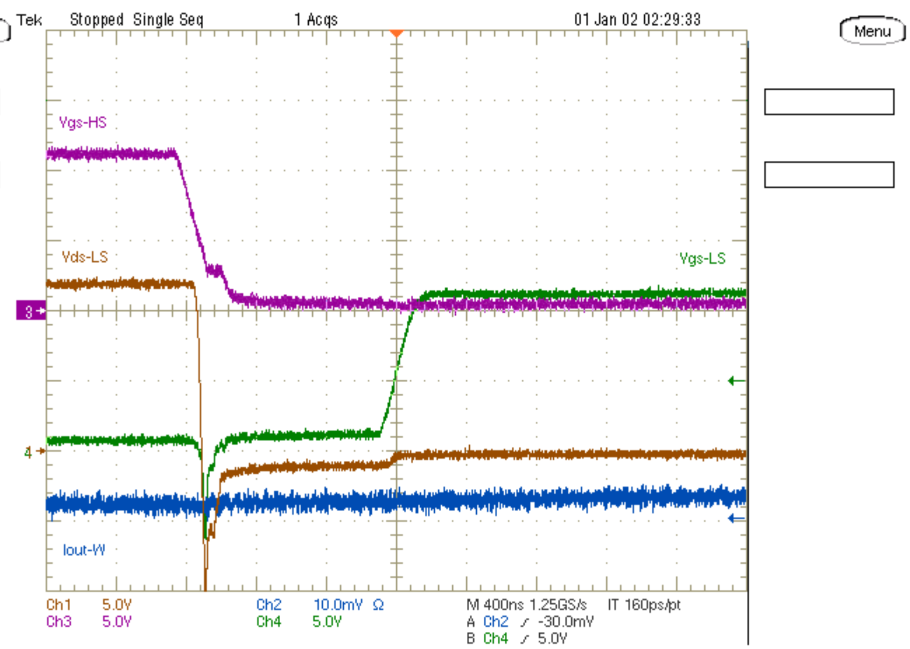
Competitor_6 – HS Ton/ Toff LS V_{GS}+HS V_{GS}

- HS V_{GS}, LS V_{GS}; LS V_{DS}; phase OUT current

Turn ON



Turn OFF



1. LS drain-source voltage
2. Phase current
3. HS gate-source voltage
4. LS gate-source voltage

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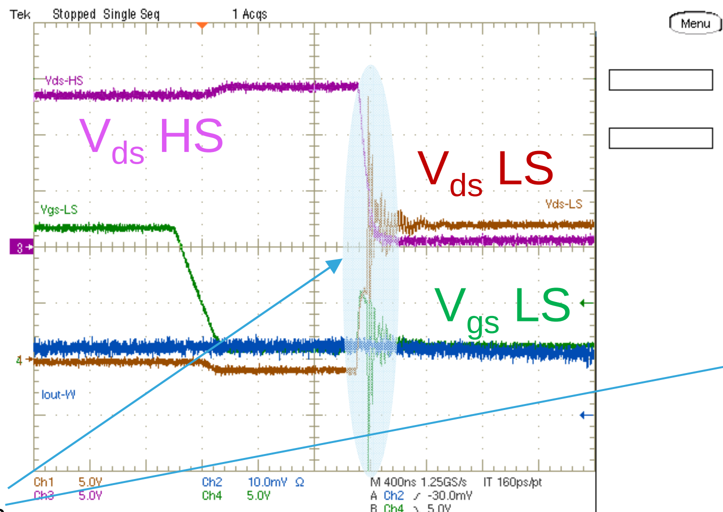
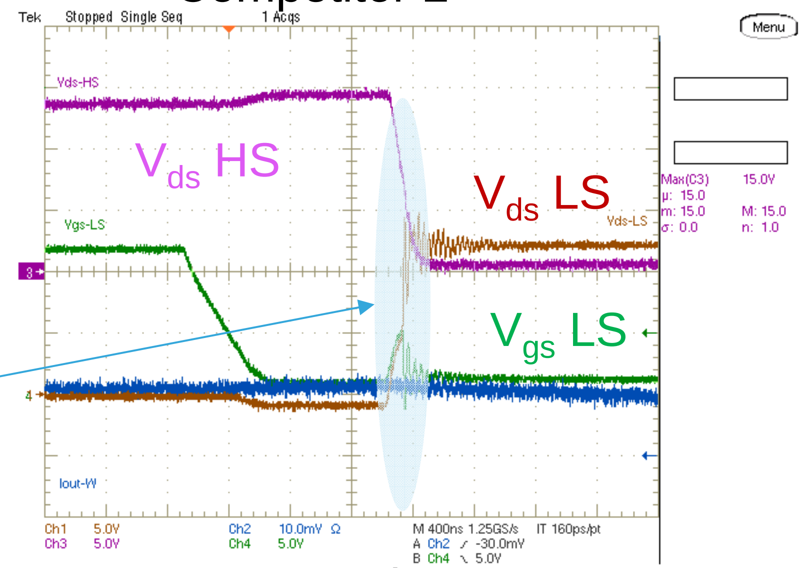
LS turn OFF switching comparison

Competitors 1 and **2** show high frequency ringing that affects the EMI behavior of the FETs while **competitor 3** has higher LS Vgs bounging and slightly higher ringing

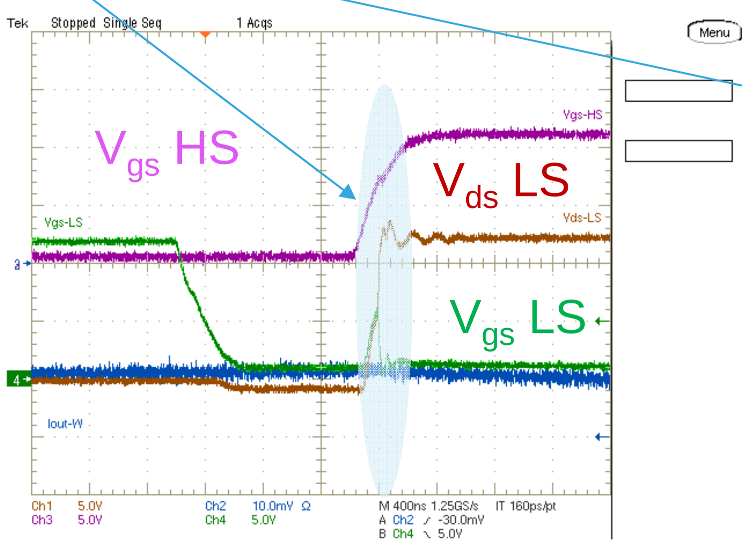
Competitor 1



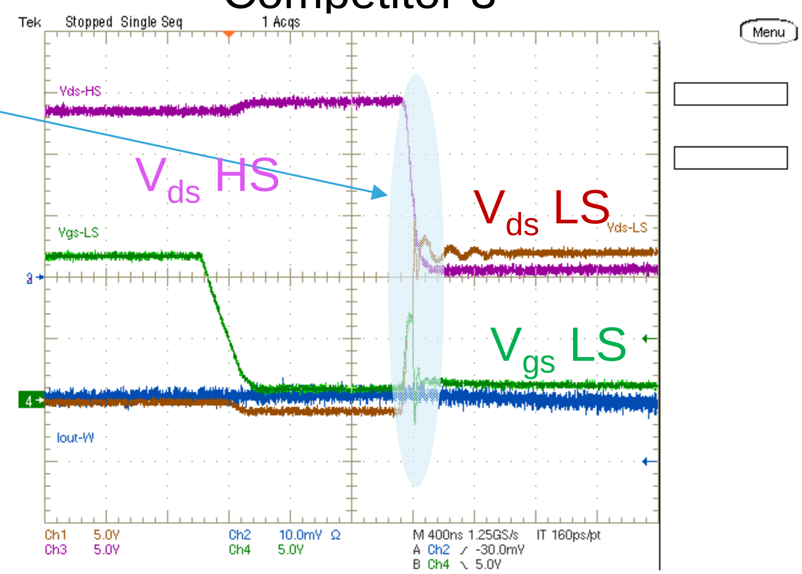
Competitor 2



STH410N4F7



Competitor 3



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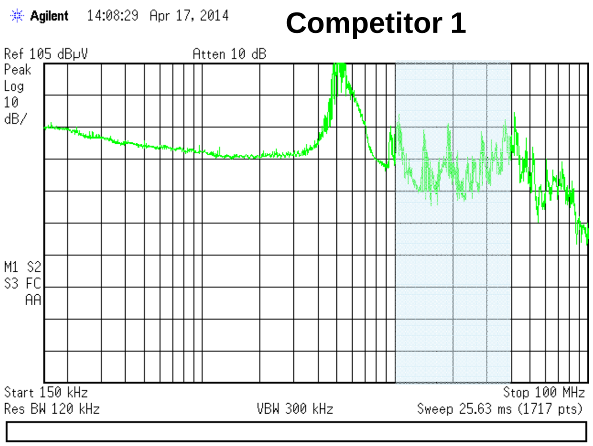
CISPR-25 conducted emissions

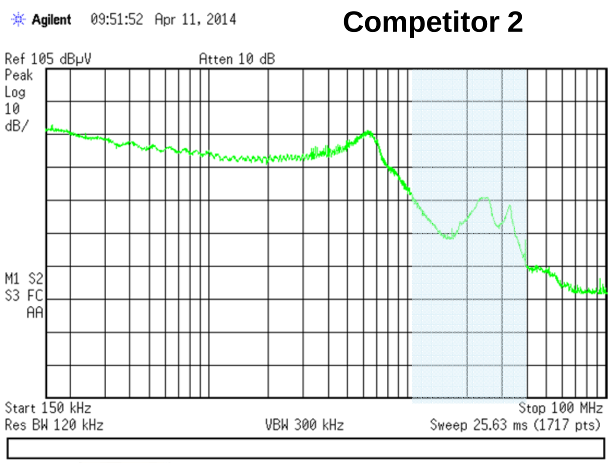
Test Equipment

- Agilent E7402A EMI test receiver
- Laboratory power source 0-20V/ 1.5A
- Laboratory power source 0-60V/ 20A
- L9906 V2.3 eval board power stage + STM8 control board
- LISN 150kHz-100MHz

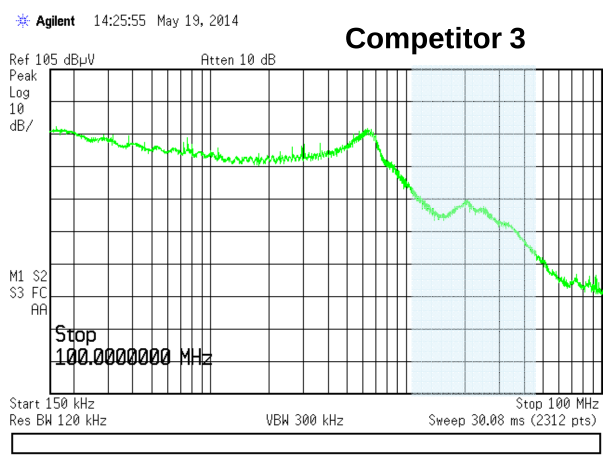
Conducted emissions benchmark Summary	
Power Transistor	**Positioning (From TOP the lowest emissions)**
STH410N4F7	1.
Competitor 3	2.
Competitor 2	3.
Competitor 1	4.



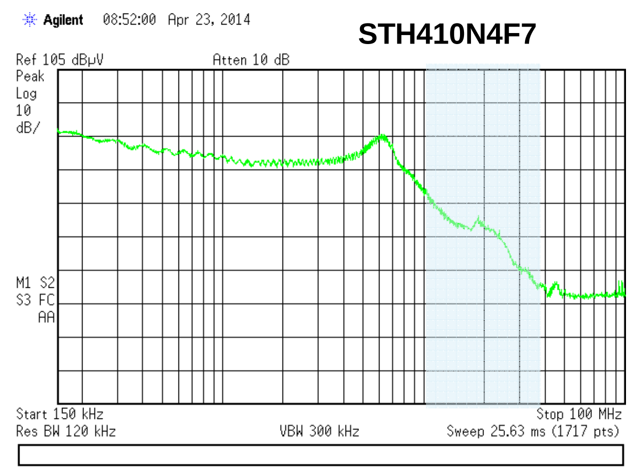
Competitor 1



Competitor 2



Competitor 3



STH410N4F7

- New STH410N4F7 shows the best EMC performance over all tested components

Thermal performance test conditions

Test Set-up

- Temperature measured directly on package (drain-wing) on LS MOSFET
- Thermal measurement done with L9906 board placed in to plastic cover to eliminate cooling with outcome air stream
- **Temperature read after** certain time when temperature of the MOSFETs was fully stabilized – no further temperature increasing.
- To have comparative results the MOS temperature was read after end of the test cycle which consist from continues ~ **16 min motor running** with 25% PWM duty cycle
- Gate current set to 100% L9907 capability ~ 600mA
- External **gate resistance 0Ω**

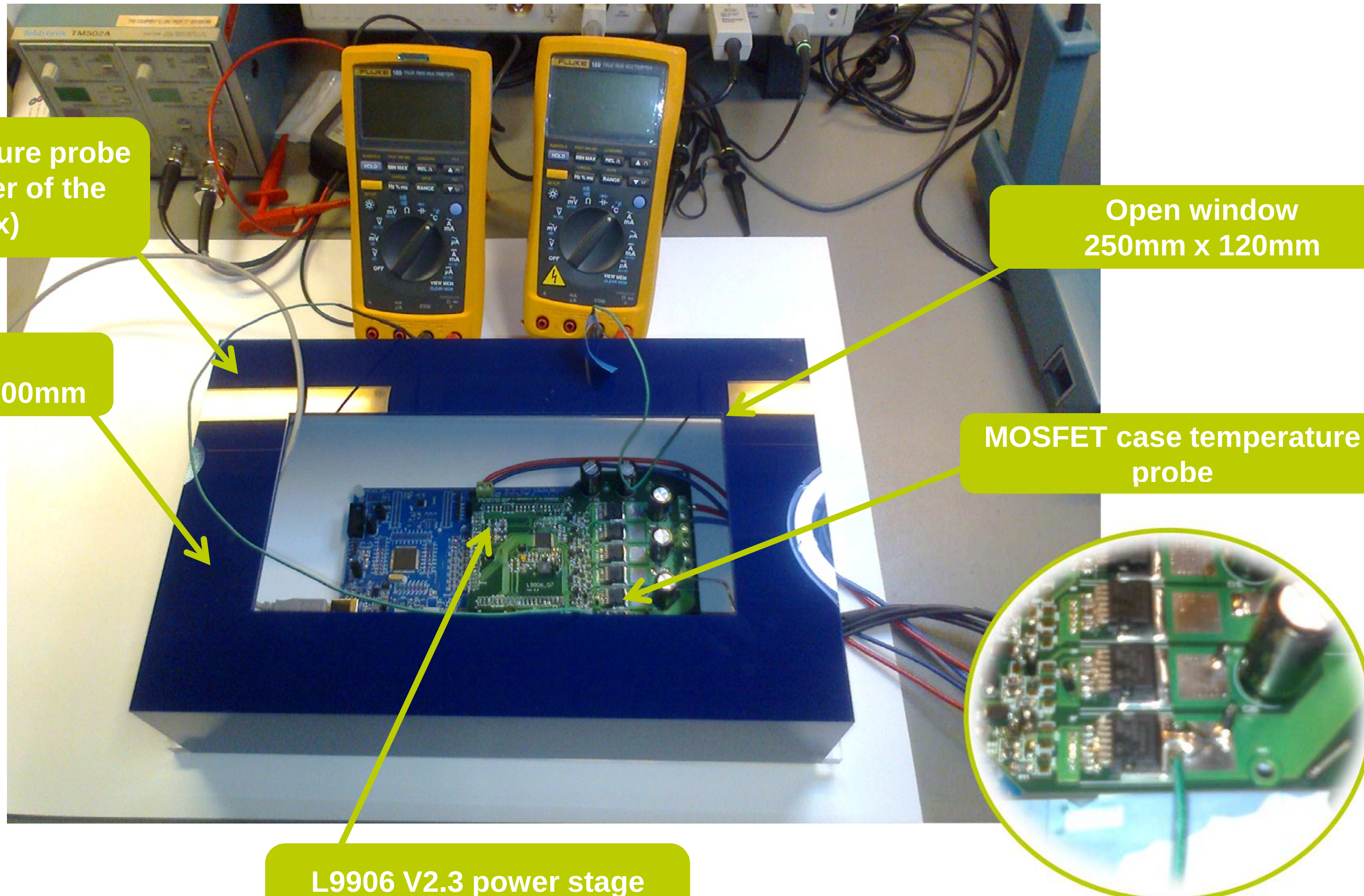
Test Conditions for thermal measurements

Switching frequency;	F_{sw} = 15.6 kHz
PWM duty cycle;	D = 25%
Supply voltage;	V_{in} = 13.5V
Gate voltage;	V_{gate} ~ 12V
Ambient temperature;	T_{amb} = 25 ˚C
Motor power	P ~100W
Motor RPM	~ 2500 RPM

Test Equipment

- 2x Fluke 189 multimeter with thermal probe
- Laboratory power source 0-20V/ 1.5A
- Laboratory power source 0-60V/ 20A
- L9906 V2.3 eval board power stage + STM8 control board

Thermal performance test set-up



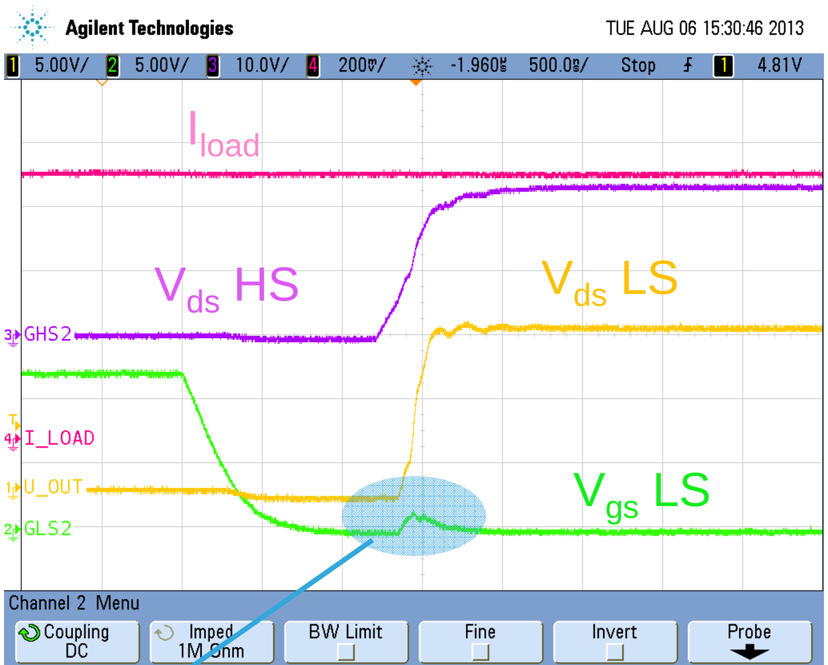
Thermal performance measurements

Thermal benchmark Summary			
Power Transistor	**$T_{ambient}$**	**MOSFET T_{case}**	**Positioning (From TOP the lowest power losses)**
STH410N4F7	**23.9**	**74.5**	**1.**
Competitor_2	24.2	77.6	**2.**
Competitor_4	24.1	83.4	**3.**
Competitor_3	21.8	84.2	**4.**
Competitor_2	22.7	88.5	**5.**
Competitor_6	23.1	91.4	**6.**
Competitor_5	X	X	**Didn't pass the test ***

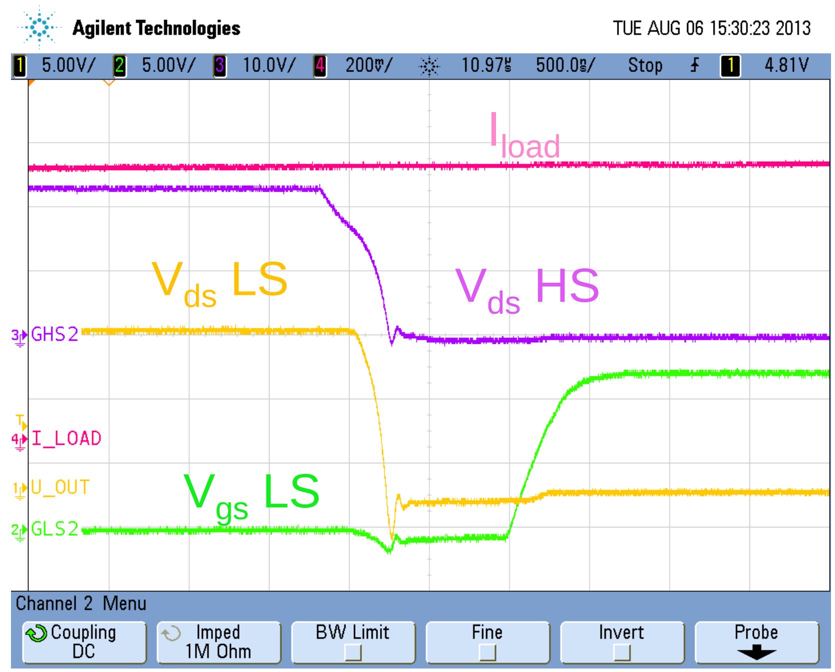
* Due to high level of produced EMI noise by D.U.T. was SPI communication quite disturbed resulting in failure of board functioning

STH410N4F7, Gate charge = 100%, R_g_ext = 5 ohm

LS turn OFF waveforms



LS turn ON waveforms



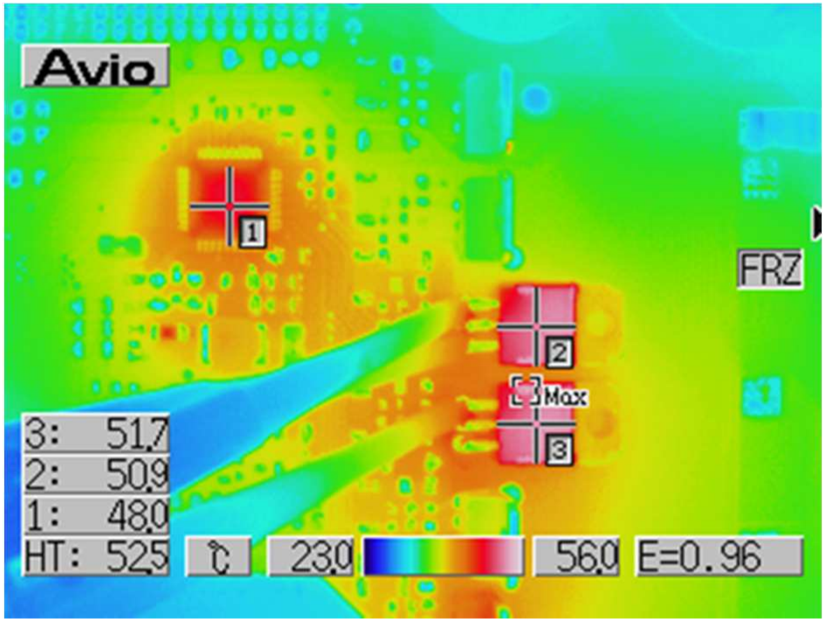
LS V_{gs} bouncing is negligible

Load current = 10A
V_{dd} = 12.5V
PWM frequency = 18.75kHz
PWM duty cycle = 25%

The picture shows the turn ON/OFF curves: V_{ds} HS (purple trace), V_{gs} LS (green trace), I_{load} (pink trace and the V_{ds} LS (yellow trace). For this trial the gate charging is unlimited up to 100% of the driver source/sinking capability and a 5 Ohm external gate resistor is used. The turning ON/OFF is fast, there is not any oscillation on both V_{gs} and V_{ds} and the small value of R_g is minimizing the Miller effect reducing the gate-source V_{gs} bouncing (negligible).

STx410N4F7, Gate charge = 100%, R_{g_ext} =5 ohm

Thermal picture



Temperature measurements:
L9907 (driver) = 48°C
HS = 50.9°C
LS = 51.7°C

The picture shows the steady state thermal picture of the single branch of the power controller (HS switch plus LS switch **without heat-sink**) plus the driver.
Because of the small external gate resistor, with the gate current provided by the driver fixed at 100% of its capability, the switching is quite fast and submitted to high switching losses. The driver temperature is quite low, while the LS is slightly hotter.

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Remarks

• The devices show good switching behavior in term of noise on both V_{gs} and V_{ds} waveforms by using a 5 Ohm driving network and setting the I_{gate_max} = 600mA (100% gate current).

• There is not any cross conduction risk even using 50% of the driver gate current sourcing / sinking capability (~ 300mA) and 15 Ω external gate resistor (worst case testing conditions) due to the high V_{th} (~ 4V for bridge configuration this is an advantage).

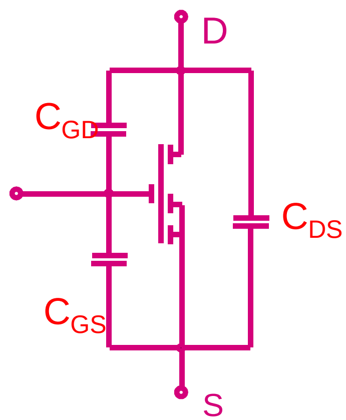
• The measured temperature are quite low, never overcoming 60°C, switching a 10A load, even without heat-sink.

STripFET^{TM} VII DeepGATE^{TM} **F7 Series**

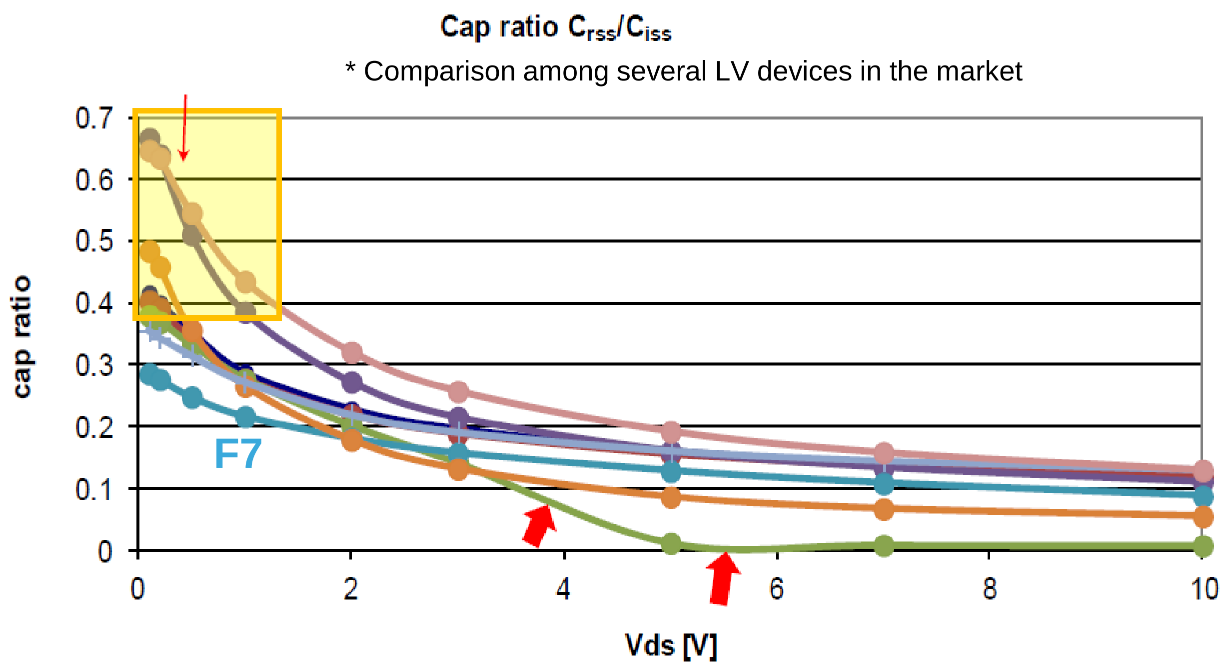
EMI consideration

➢ **Most important MOSFET parameter for good EMI erformances:**

- Crss/ Ciss ratio
- Crss/ Ciss variation



$C_{iss} = C_{GD} + C_{GS}$
$C_{oss} = C_{DS} + C_{GD}$
$C_{rss} = C_{GD}$

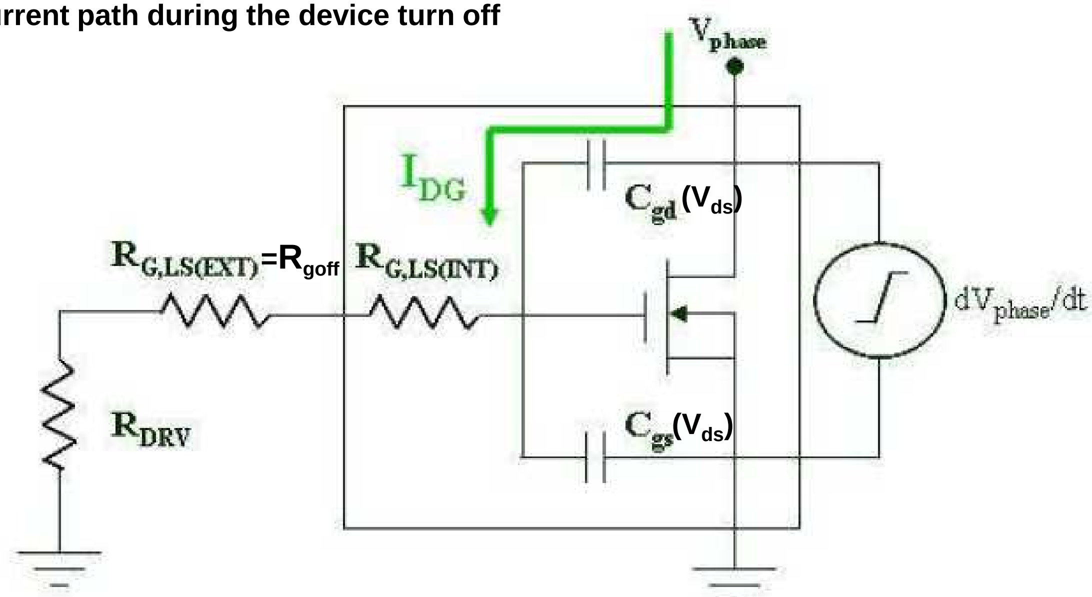


F7 is well optimized in respect to EMI

- Low Crss/Ciss (<0.4)
- Well contained Crss/Ciss variations (0.1 ÷ 0.3)

Theoretical explanation

Typical current path during the device turn off



A smaller C_{gd} and bigger C_{gs} will minimize the residual V_{gs} (capacitive divider) when device is off.
The V_{gs} bouncing, produced by the dV/dt on the motor connection point (source of HS FET connected to the drain of LS FET of the H bridge), where the **V_{gs} bouncing** is just the **$V_{gs}=R_{g\_tot} * C_{gd} * dV/dt$**, ($R_{g\_tot}$ is the sum of the intrinsic R_g plus the external gate resistor R_{goff} plus the output driver resistance RDRV), if next or over the FET V_{th}, can produce a sub-threshold conduction of the FET that is the **root of the noise**. Therefore the gate-source capacitive fine tuning and the R_{g_off} reduction are addressed to minimize the bouncing on the gate. The layout has an impact (different bridges' behavior) because the PCB tracks have spurious inductances that affect the di/dt and therefore the oscillation as well (RCL resonant circuit).
R_{g_ext} and IC driver next to the gate pin can improve the switching of the FET. This means L stray minimization and smoothing of oscillations that are the source for EMI.

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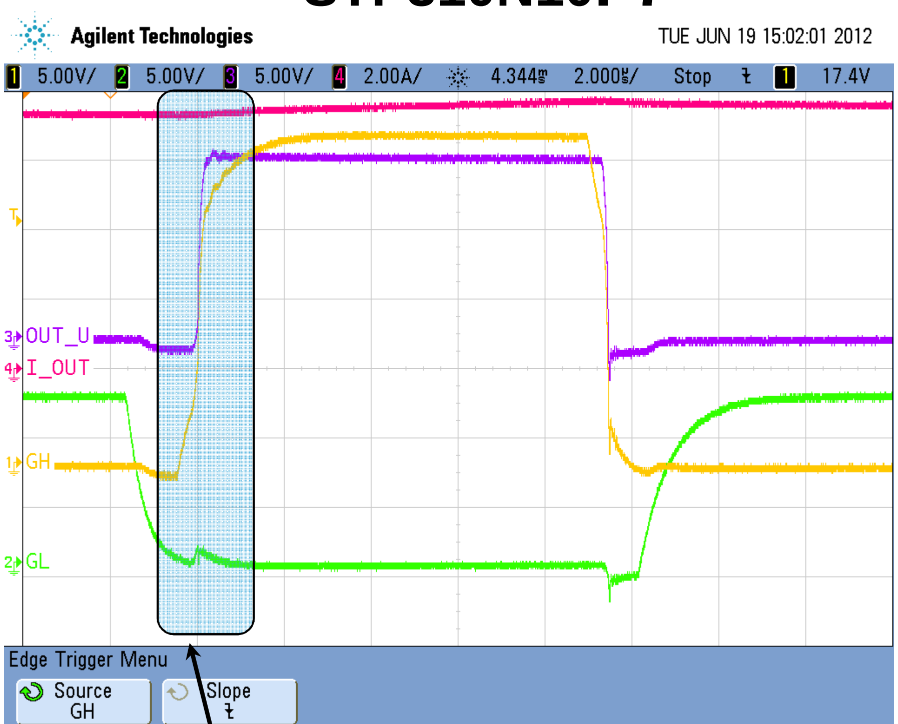
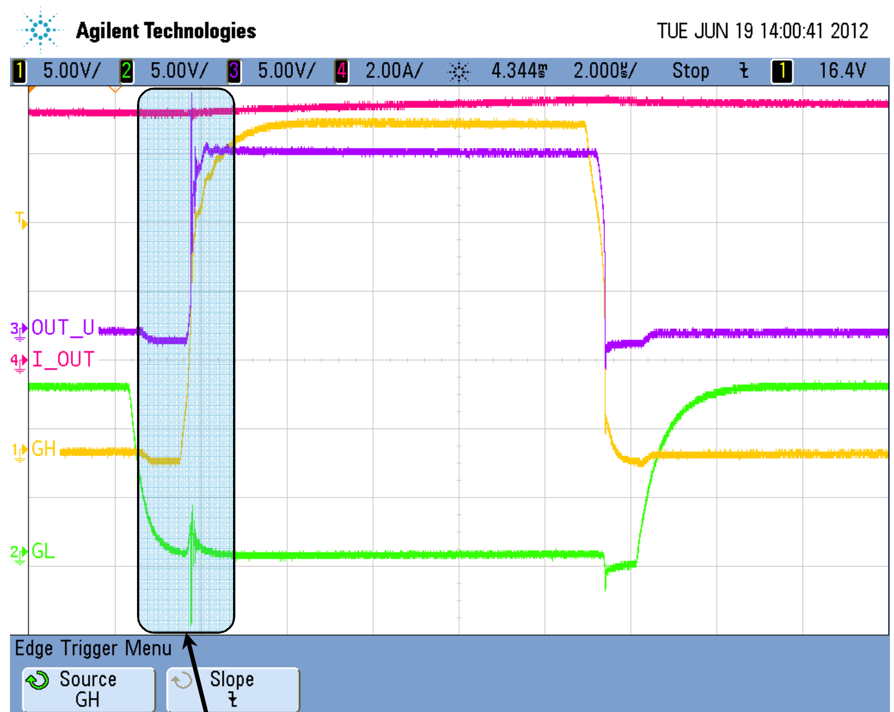
Waveforms at HS turn ON/OFF

STP310N10F7



V_{gs} and V_{ds} low side smoothed waveforms

STP180N10F3



V_{gs} Low side bouncing plus V_{ds} overshoot

1. Due to the better capacitance ratio and diode recovery behavior, STP310N10F7 shows a better switching behavior than STP180N10F3.
2. The smoothed noise during turn on/off minimize also the EMI of the system (direct measurement should confirm last statement) even with 0 Ohm external gate resistor.

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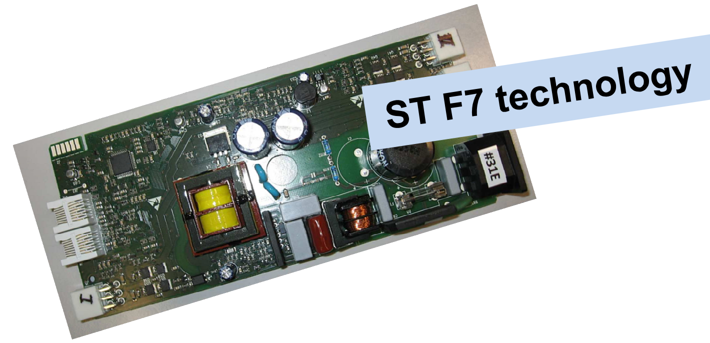
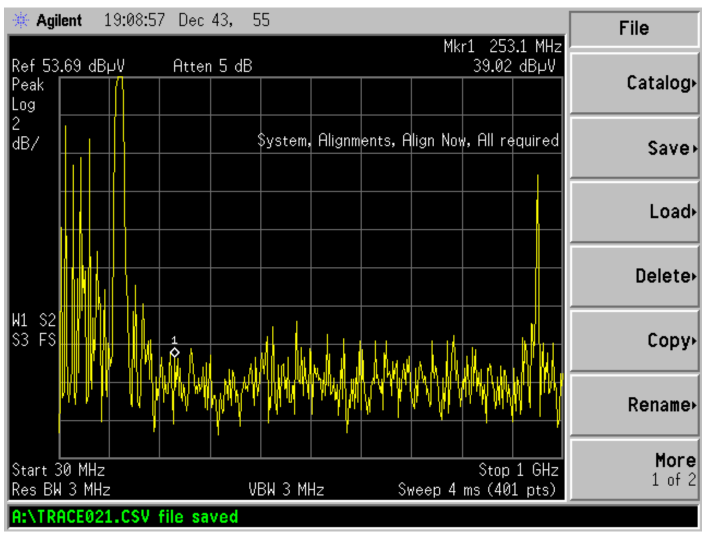
H-bridge configuration

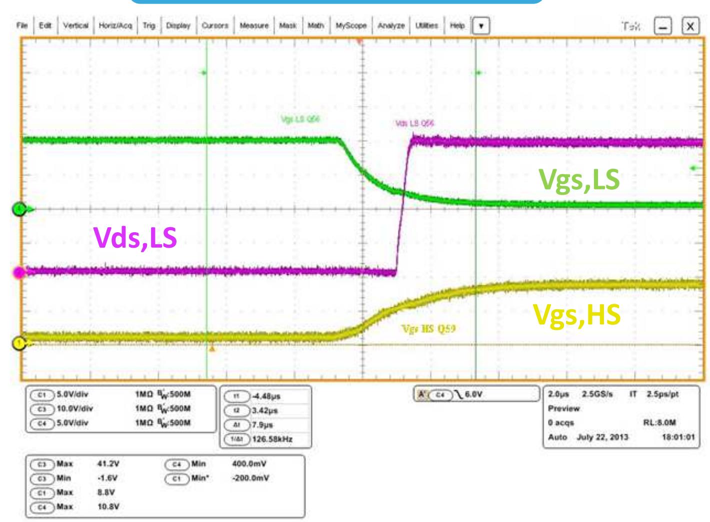
F7
80V-100V
NEW



- **STripFET F7 technology** matches very well application requirements:
  - **Improved switching behavior**
  - **No high frequency ringing between gate and source**
  - **Entire system EMI performance enhacement**



Low Side turn-on

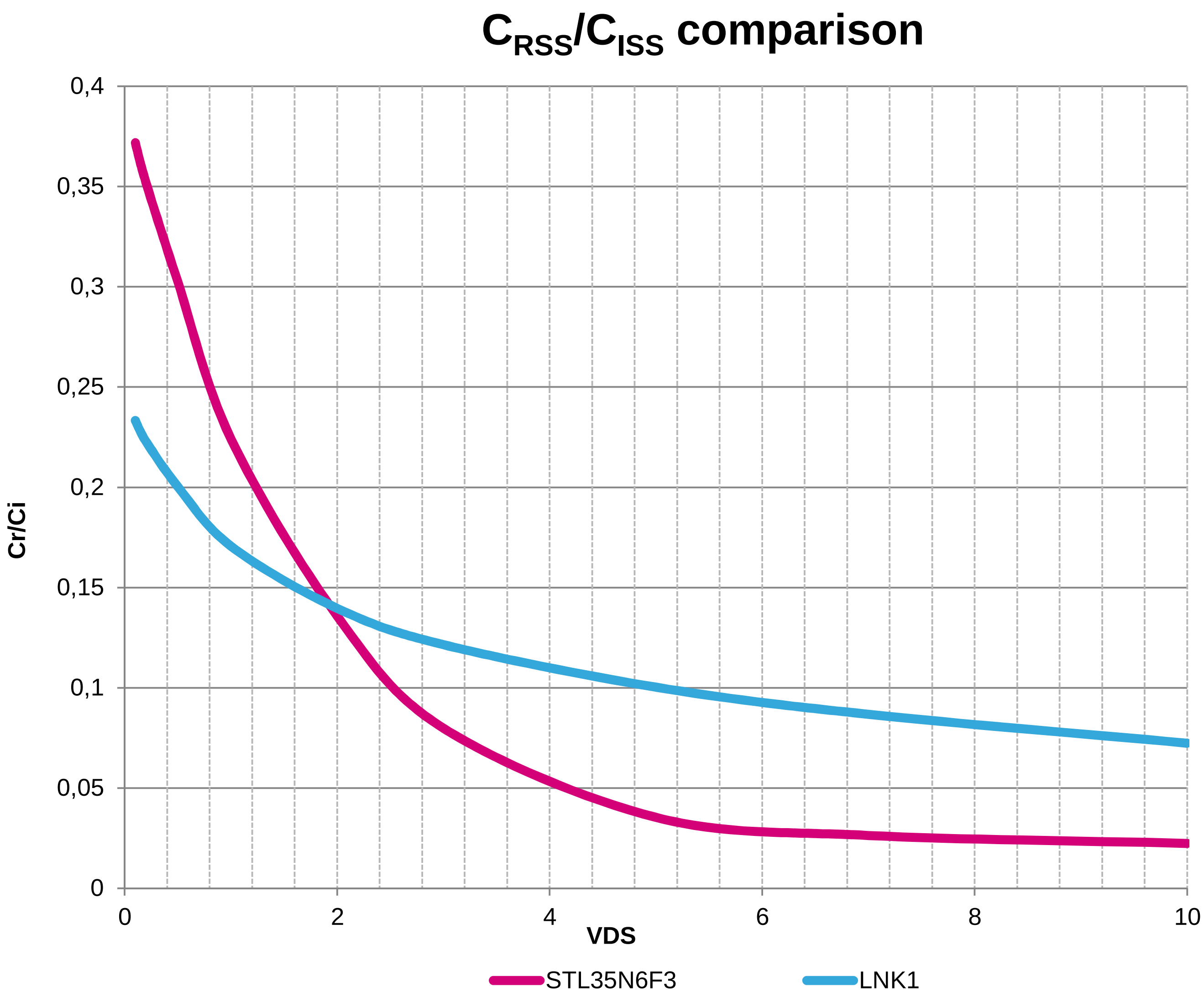


Main electrical parameters' comparison

	V_{th} @250µA [V]	BV_{dss}@250µA [V]	V_{sd} @25mA [mV]	R_{on} @10V /10A [mΩ]	C_{iss} @25V [pF]	C_{oss} @25V [pF]	C_{rss} @25V [pF]	*R_{g_int} [Ω]
STL35N6F3	3.13	68.9	624	18.1	763	173	16	3.24
LNK1	3.5	> 60	630	19.5	1280	499	49	2.25

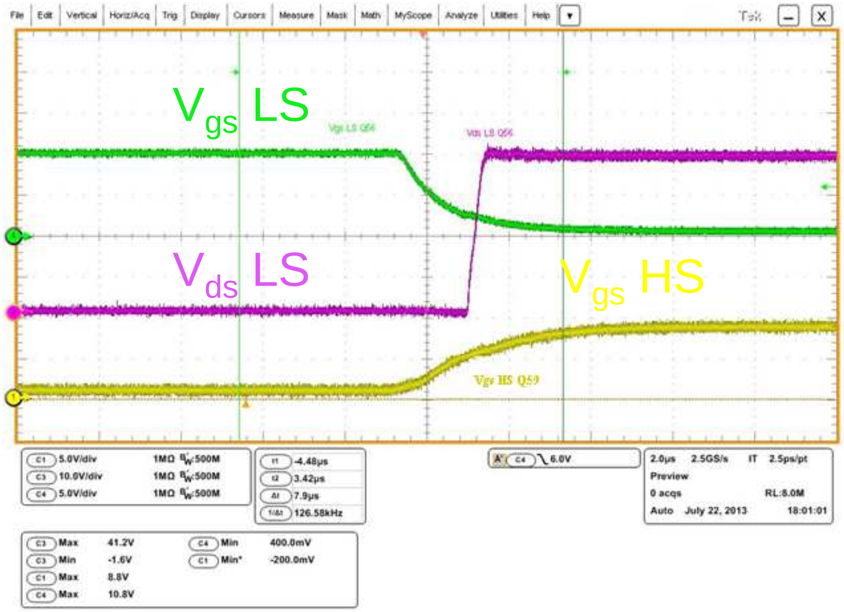
This measurement was performed at 1MHz by LCZ meter and by curve tracer

Capacitive ratio comparison

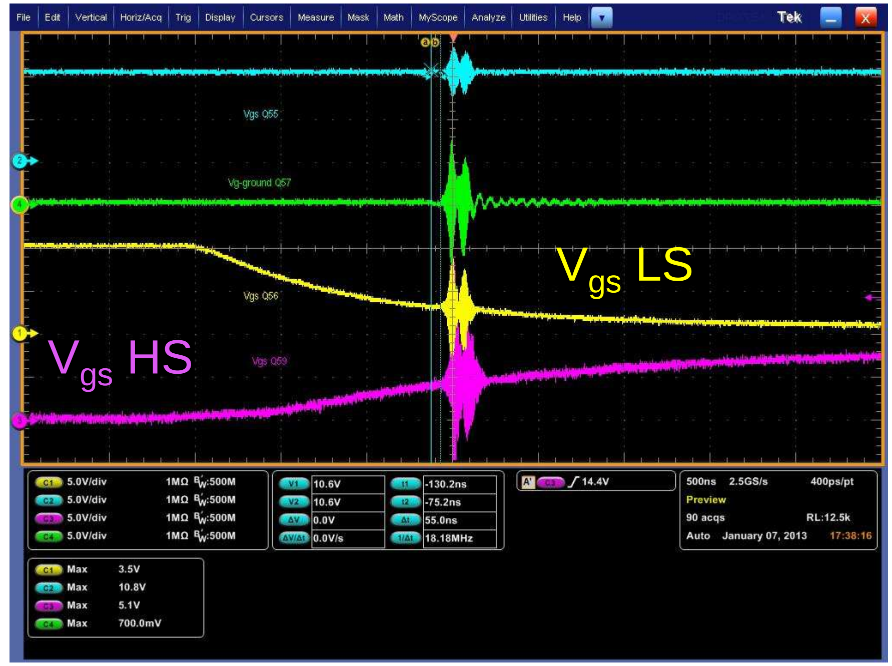


Waveforms comparison at LS Turn OFF

F7 switching LS turn OFF



F3 switching LS turn OFF



1. The waveforms are not affected by any voltage oscillation.

Because of the better **capacitive ratio** and proper V_{th} value, even using the original customer set up, LNK1, new F7 technology ST device, didn't show any voltage oscillation during the reverse motor movement. This electrical behavior during the switching improves the EMI sensitiveness of the whole system.

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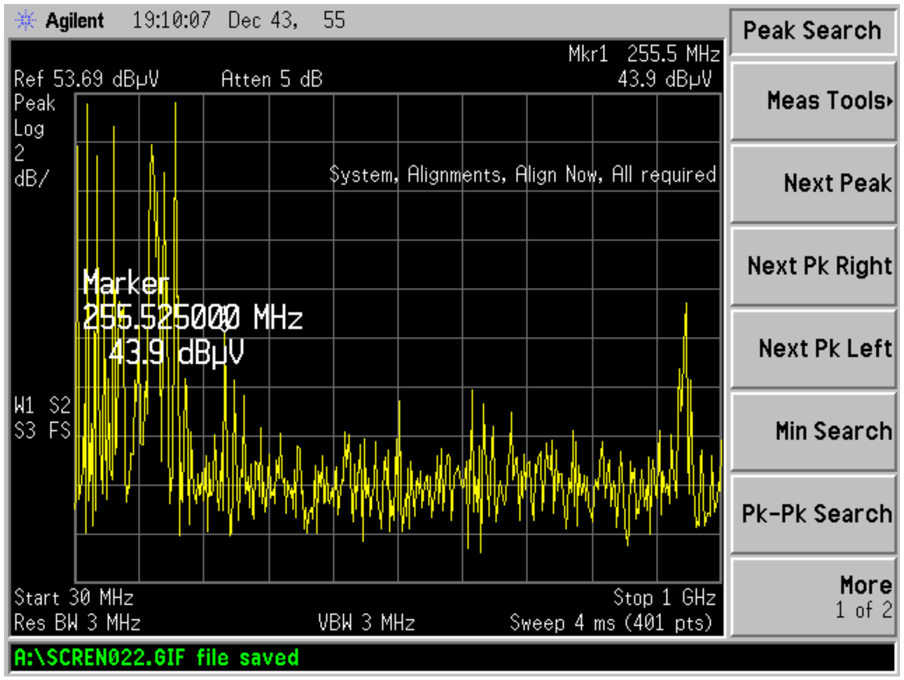
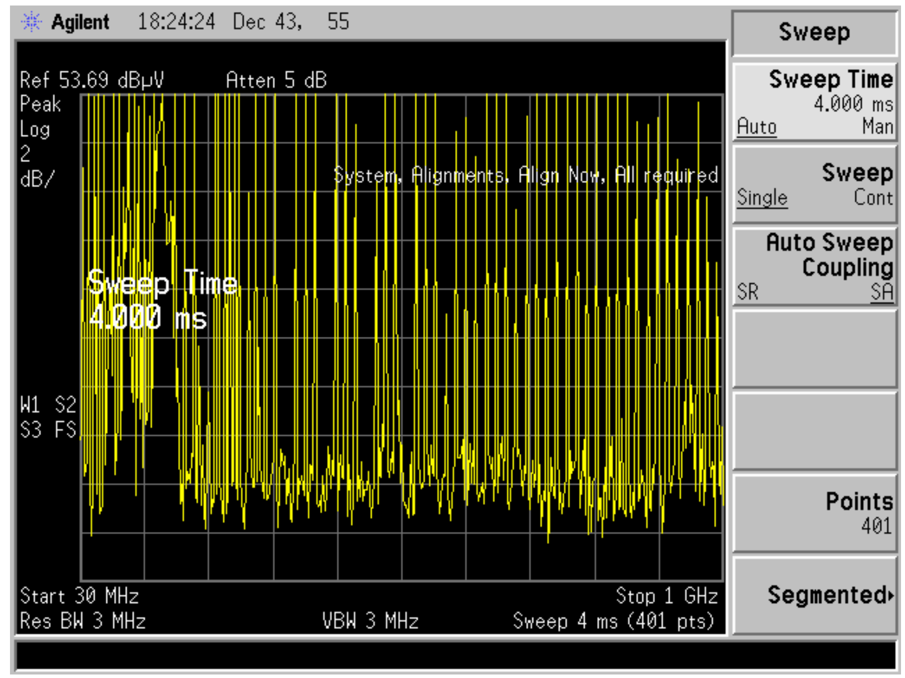
ST technologies’ EMI measurement comparison

Down movement with F7



Down movement with F3



The down movement is heavily affected by EMI;
Measurement performed by AGILENT E4402B 100Hz-3 GHz spectrum analyzer and RSH 400-1 probe SET HZ-15 (0÷3GHz) -20dB attenuation ROHDE SCHWARZ

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40V-60V STripFET F6 with mono Schottky

F6
40V-60V

- **Monolithic Schottky diode** improves overall MOSFET peformances in bridge configurations:
  - **Reverse recovery process optimization** (smaller I_{RRM} and lower Q_{rr}, V_{DS} spike reduction)
  - **Lower diode power dissipation**
  - **Efficiency improvement**

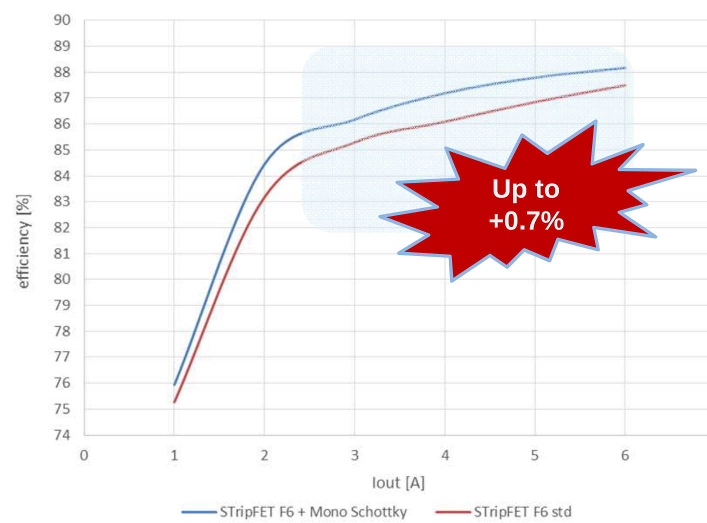
Turn-off waveforms

Mono Schottky vs. std :parameters overview

Tech.	Irm (A)	Qrr (nC)	Tirm (ns)	Trr (ns)
F6 std.	2.56	70.6	34.4	55.25
F6 + Schottky	1.92	47.9	31.5	49.75

-24%

-10%

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