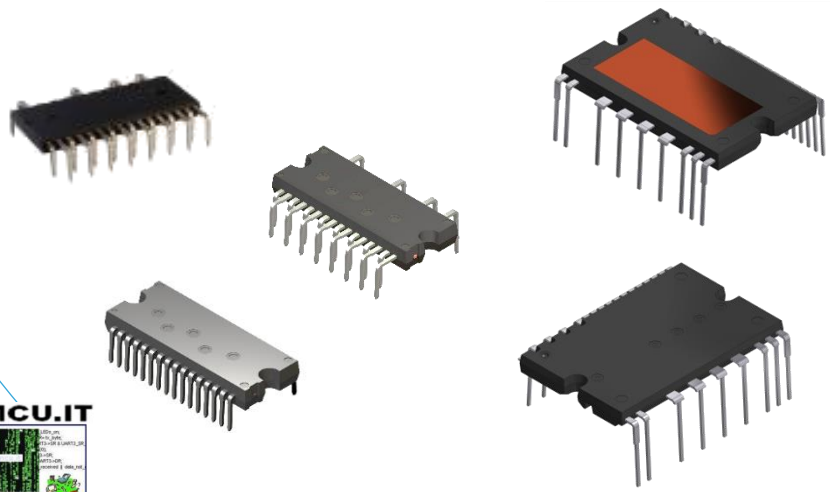
SLLIMM™ Series

Small Low-Loss Intelligent Molded Module

Power Transistors Division



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SLLIMM series: Facts

- Well recognized in Home Appliance Market (Discrete and IPM)

MARKET

- # 3 Front-end for IGBT (6” and 2X 8” Catania and S’pore)

Front-END

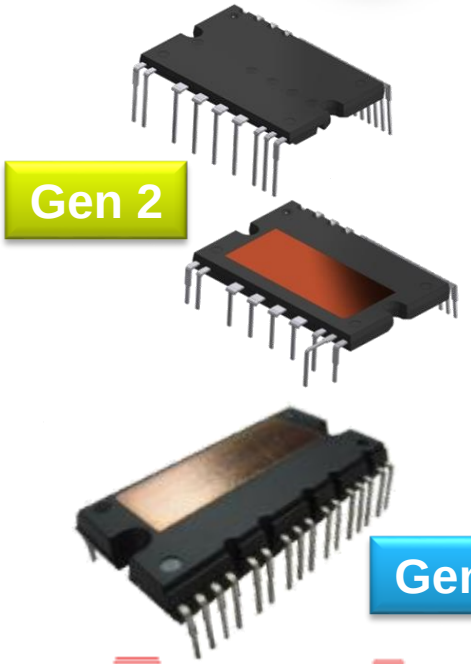
- # Own Back-End for SLLIMM™ (IPM) production + 1 for nano (subcon)

IPM Back-End

- # UL certification for SLLIMM™ (#1557)

Cerification

SLLIMM™: 100% ST (F/E & B/E)



AVNET Memec

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Current SLLIMM™ portfolio

Up to 100W in free-air

SLLIMM-nano

- Dishwashers
- Refrigerators
- Fans & pumps, …

nDIP-26L

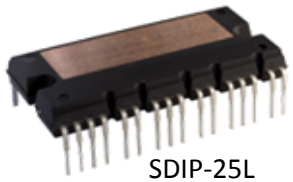
SLLIMM

- Washing machine
- Air-conditioner
- Dryer, …..

From 500W to 2.5kW

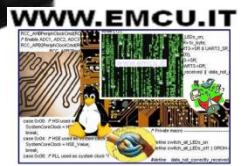
PN	I_C (@ 25°C) [A]	Package	NTC	Bootstrap Diode	Rth [°C/W]	Std input driving
STGIPN3H60A	3	NDIP-26L	No	Yes	50*	STGIPN3H60AT
STGIPN3H60	3	NDIP-26L	No	Yes	50*	STGIPN3H60(T)-H
STGIPS10K60A	10	SDIP-25L	Yes	Yes	3.8	
STGIPS10K60T	10	SDIP-25L	Yes	Yes	3.8	STGIPS10K60T-H
STGIPS10C60	10	SDIP-25L	Yes	Yes	3.8	STGIPS10C60(T)-H
STGIPS14K60	14	SDIP-25L	No	Yes	3.0	
STGIPS14K60T	14	SDIP-25L	Yes	Yes	3.0	STGIPS14K60T-H
STGIPL14K60	15	SDIP-38L	Yes	Yes	2.8	
STGIPS15C60	15	SDIP-25L	Yes	Yes	3.0	STGIPS15C60(T)-H
STGIPS20K60	18	SDIP-25L	No	Yes	2.4	
STGIPS20C60	**20**	SDIP-25L	No	Yes	2.7	STGIPS20C60(T)-H
STGIPL20K60	20	SDIP-38L	Yes	Yes	2.2	
STGIPS30C60	**30**	SDIP-25L	No	Yes	2.4	STGIPS30C60(T)-H
STGIPL30C60	**30**	SDIP-25L	No	Yes	2.2	

* Value referred to Junction- ambient



SDIP-25L

SDIP-38L



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Main Customer using ST IPMs

In production:

- Electrolux
- Whirlpool
- BSH
- GE
- Fujitsu General
- Emerson Climate
- EGO
- Regal Beloit
- Papst
- Kinetec pumps
- Sanyo Hefei
- Fisher& Paykel

In qualification:

- Miele
- Haier
- Sanjo Denki

Over 40% Share in US & Europe

Electrolux

embraco

GREE

Miele

B/S/H/

Whirlpool

LG Life's Good

FUJITSU FUJITSU GENERAL

E·G·O High-tech since 1931.

SAMSUNG

EMERSON Climate Technologies

SANYO 合肥三洋

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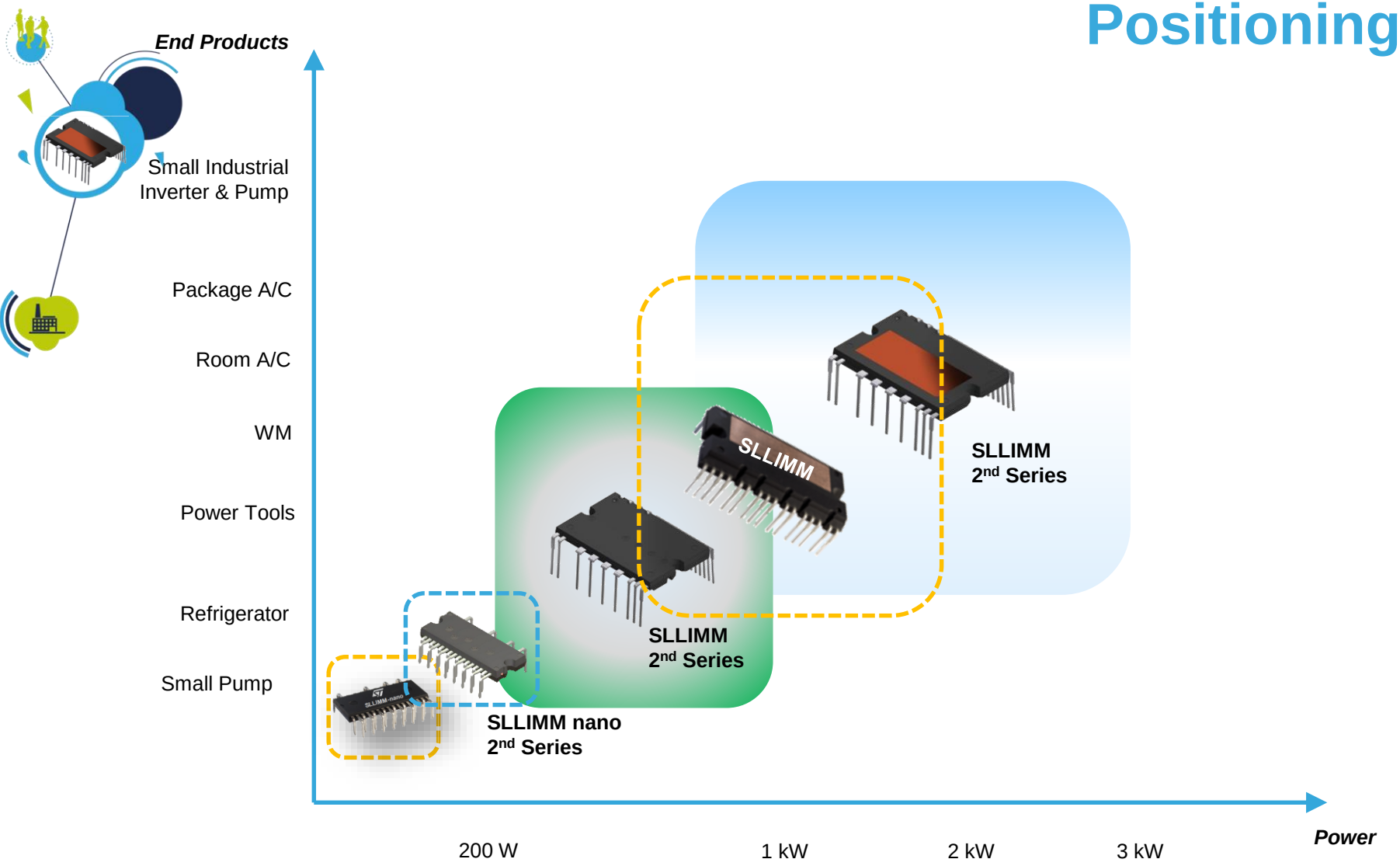
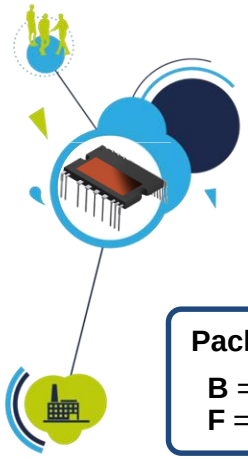
SLLIMM Series: Positioning



SLLIMM 2nd series: Nomenclature



Package
B = DBC
F = Full Molded

IGBT based

IGBTs Technology Speed
CH = drives (4 ÷ 32 kHz)
M = up to 20KHz

Temperature sensing/protection
T = NTC on board option
S = Temperature sensing

ST **G** **I** **x** **5** **CH** **60** **yz** **-** **L**

SLLIMM™
(Intelligent Power Module)

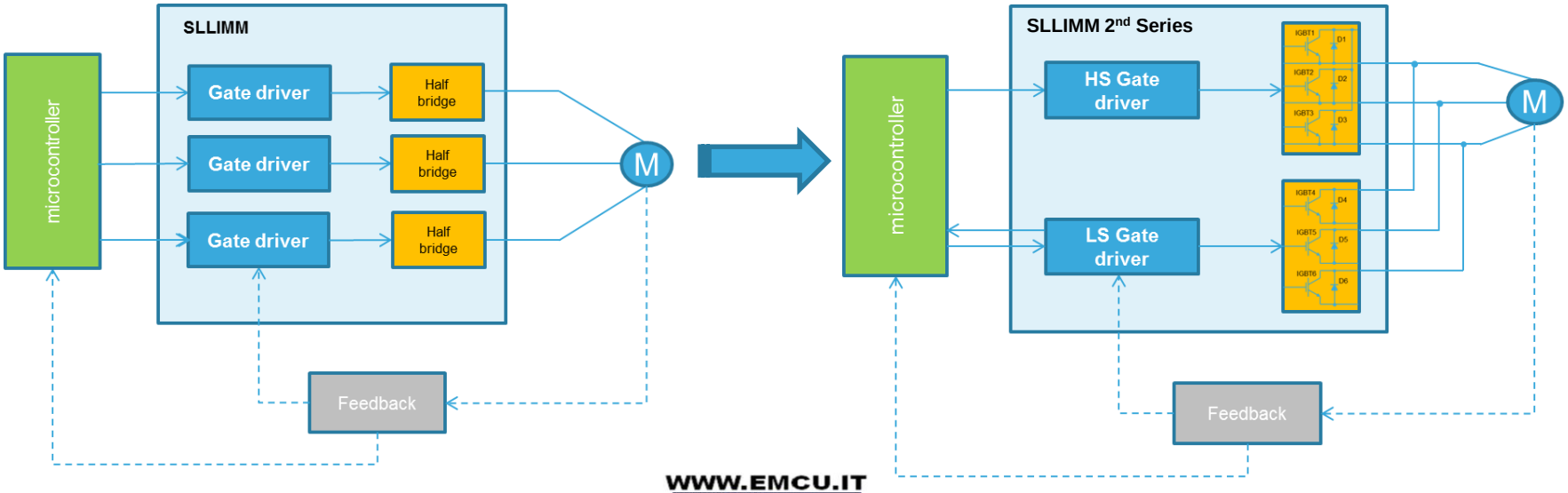
Max Continuous Current (DC) @ 80˚C

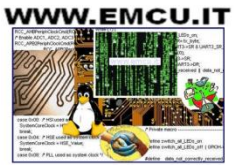
Leads finish option
E = Short leads and emitter forward
L = Long leads

Breakdown Voltage / 10

SLLIMM 2nd series: introduction

The SLLIMM series, small low-loss intelligent molded module family of intelligent power modules combine IGBT power switches in a 3-phase IGBT inverter stage configuration with freewheeling diodes, control Ics for gate driving, protections and other optional features in a single package, replacing more than 10 discrete devices.
The **SLLIMM 2nd series** has been designed using a new internal configuration with only two drivers, one high side driver and one Low side driver.
This new approach allows a more compact package and new advanced protection functions, thanks to the new features showed by Low side driver.
Two IPM versions are available, the Full Molded and the DBC (Direct Bond Copper) both compatible each other.
The products belonging to the new SLLIMM 2nd series show the best compromise between conduction and switching energy with an outstanding robustness and EMI behavior, making the new product ideal to enhance the efficiency of compressor, pumps, fans and low power motors working up to 20 kHz in hard-switching circuitries.
This series will complement and overcome the already available SLLIMM series in term of features, packages' types and flexibility.





SLLIMM 2nd series: Package Technology

General Features

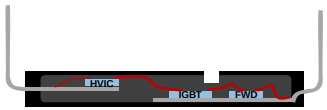
- DIP Molded Package (26 leads*)
- Lead frame for signal stage
- Enhanced creepage
- Improved pin out for easier BOARD design
- 2 leads options:
  - Short leads and emitter forward
  - Long leads
- 2 package options:

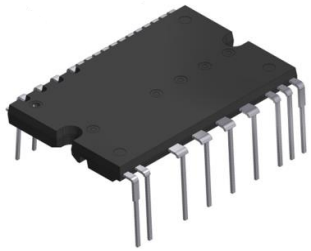
***26 for NTC on board version**
25 for no NTC on board version
Lead n°1 is cut

ST G I B x CH 60 TS - L

ST G I F x CH 60 TS - L

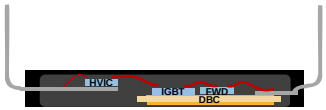
Full Molded

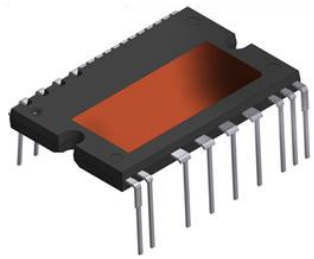




- ideal choice for low/medium power platforms

Direct Bond Copper



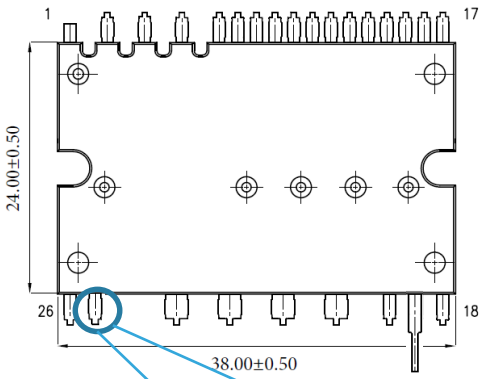


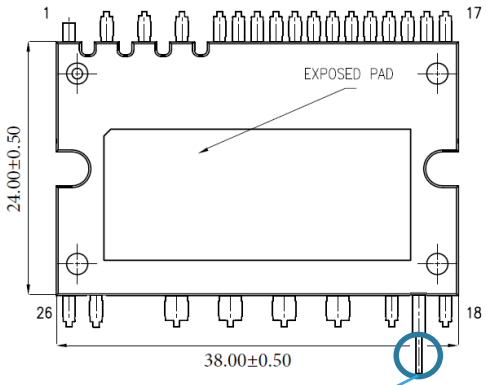
- Improved DBC for power side for a better thermal dissipation
- Vacuum soldering process to improve the die attach

SLLIMM 2nd series: Package Options

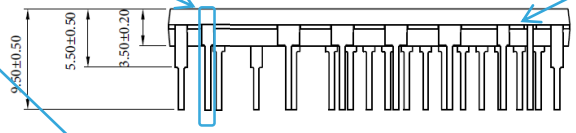
FM

DBC

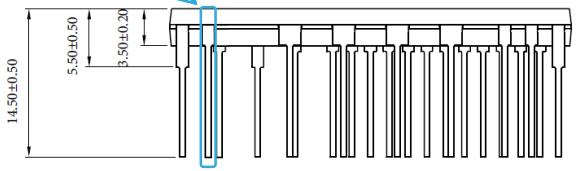




NTC

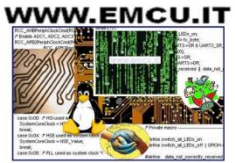


Short Leads and emitter forward

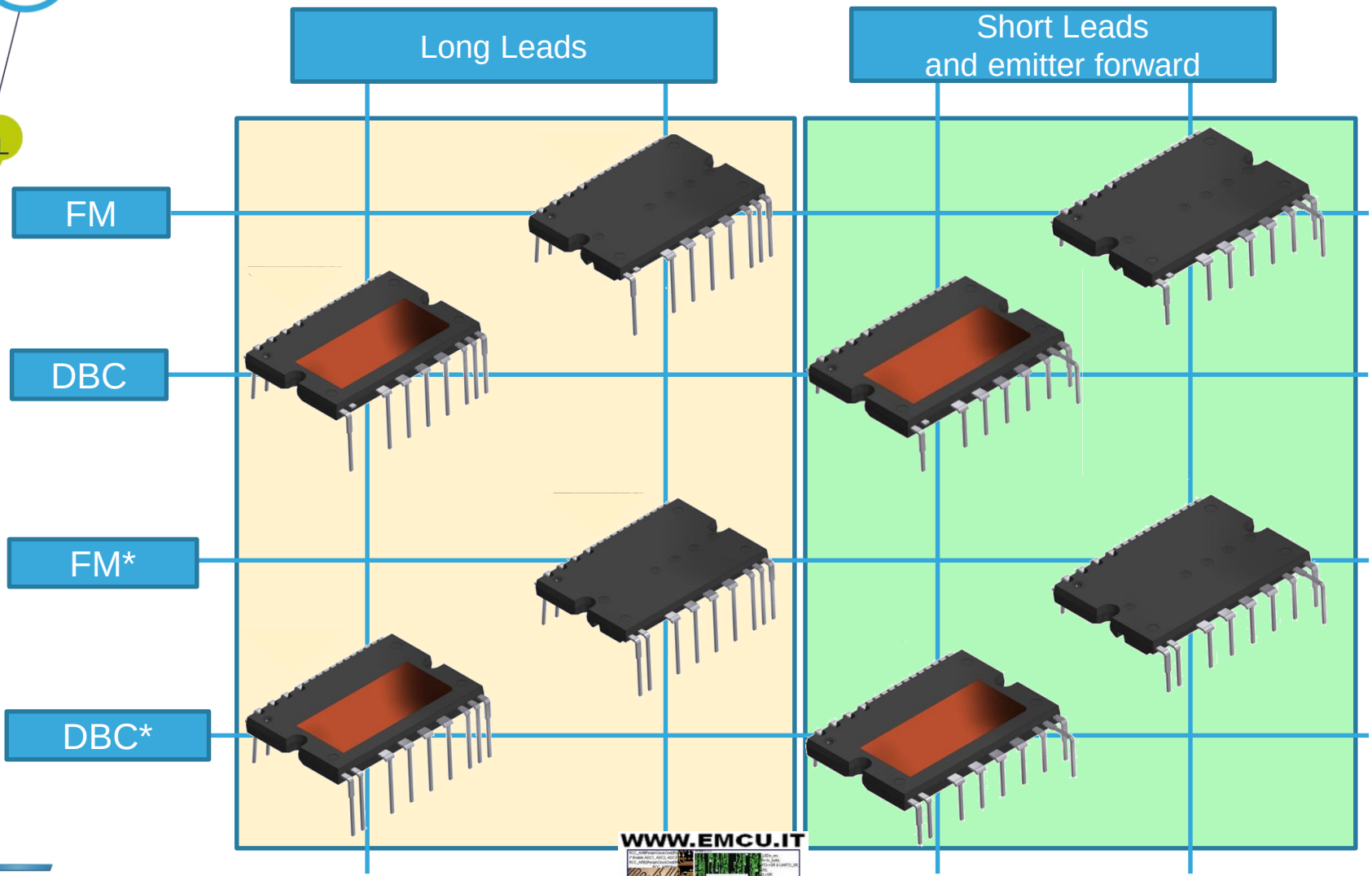


Long Leads

All measures are in mm



SLLIMM 2nd Series : Package options



*SLLIMM 2nd series with NTC

SLLIMM 2nd Series : Pin Out + Internal Circuit

High voltage pins away from low voltage pins

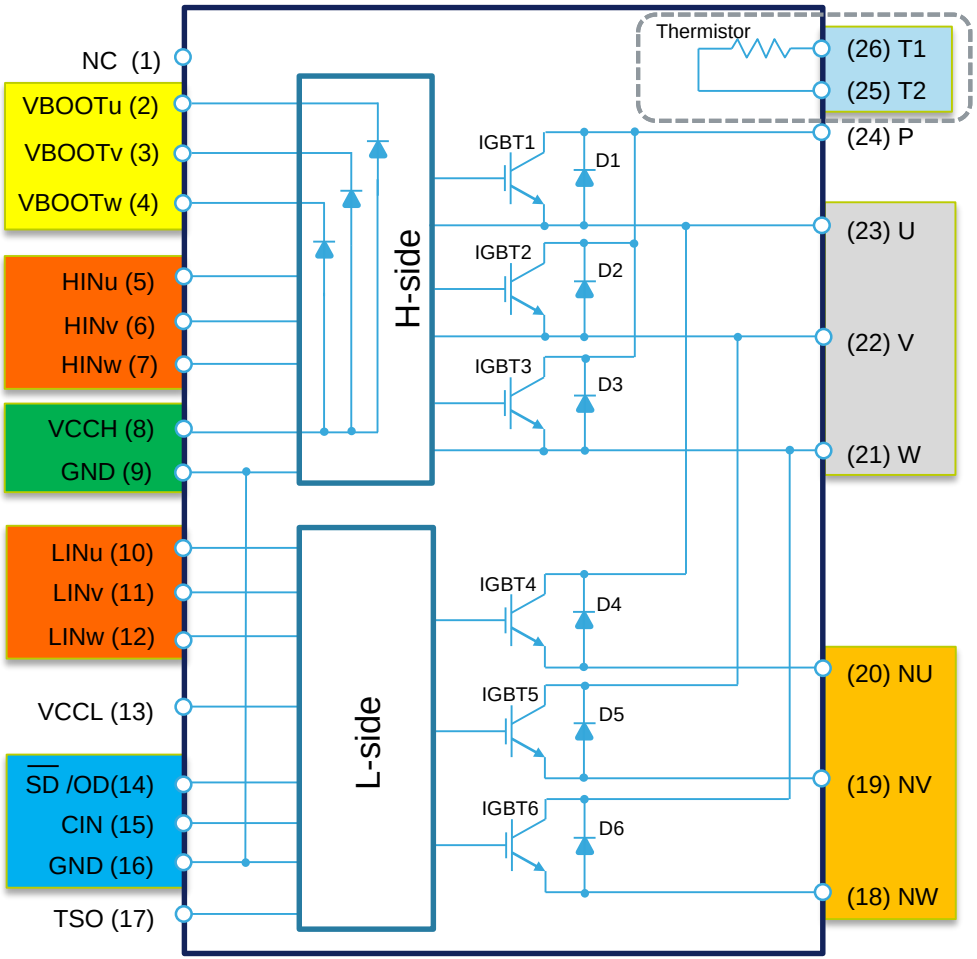
High side input close each other

VCC close to GND to reduce the stray inductance

Low side input close each other

GND close to critical pins (SD and CIN) for an easy filtering

Integrated sensor temperature output



NTC option on power side for a better temperature monitoring

Outside pins close each other for a simplified PCB routing

Emitter pins close each other for a simplified PCB routing for both single and three shunt solutions

SLLIMM 2nd series: Product Features

FM/DBC fully isolated packages

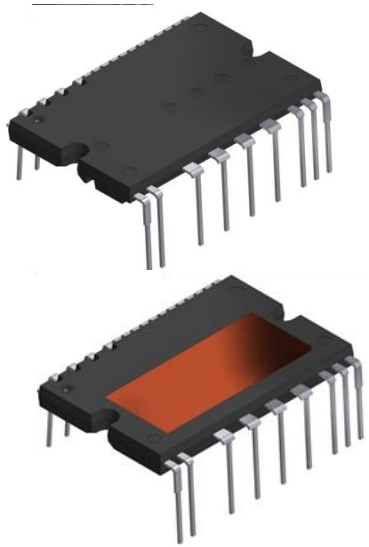
cover a bigger range of power requirement

UVLO

Malfunctioning and fault prevention for Vcc and Vboot

Integrated Bootstrap diode

Reduce BOM and simplified layout



Sense comparator

Fault protections: over current and short-circuit

Smart shut down

High speed fault condition info for the MCU to shut down internally the Nside IGBTs

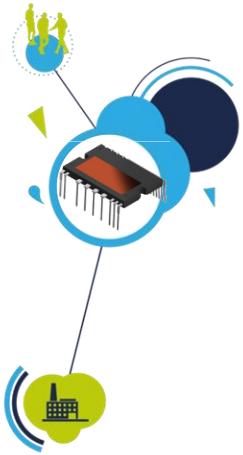
Thermal Sensor Output

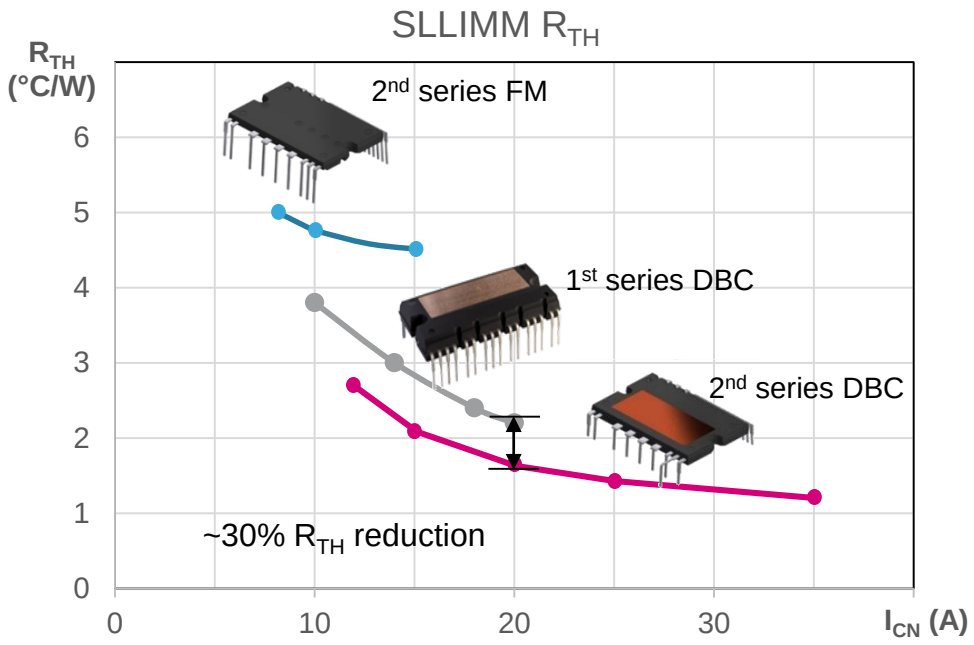
Temperature sensor integrated to monitoring on the low side section

NTC thermistor

Temperature monitoring placed on the power side

SLLIMM 2nd Series: IGBT $R_{TH(J-C)}$ curves

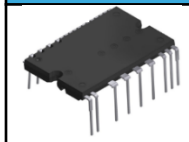
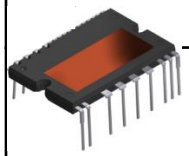




2nd series $Rth_{(j-c)}$ simulated values

PN	SLLIMM series		I_{CN} @ 25°C	$R_{TH(J-C)}$ IGBT
STGIF5CH60x	2nd	FM	8A	5.0 °C/W
STGIF7CH60x			10A	4.8 °C/W
STGIF10CH60x			15A	4.6 °C/W
STGIB8CH60x		DBC	12A	2.9 °C/W
STGIB10CH60x			15A	2.1 °C/W
STGIB15CH60x			20A	1.7 °C/W
STGIB20CH60x			25A	1.45 °C/W
STGIB30CH60x			35A	1.25 °C/W
STGIPS10K60	1st	DBC	10A	3.8 °C/W
STGIPS14K60			14A	3 °C/W
STGIPS20K60			18A	2.4 °C/W
STGIPL20K60			20A	2.2 °C/W

SLLIMM 2nd Series: Synoptic table

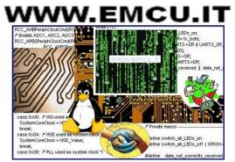
Package	Part Number	Ic @ 25°C (@ 80°C)	Voltage	Vce(sat) @ 25°C	Rthj-c (max)	Viso	Max T_J	Samples (Mass Prod)
 SDIP2F-26L	STGIF5CH60TS-L(E)	8A (5A)	600V	1.6V	5.0 °C/W	1500V	175°C	Done
	STGIF7CH60TS-L(E)	10A (7A)	600V	1.6V	4.8 °C/W	1500V	175°C	wk 29 (wk30)
	STGIF10CH60TS-L(E)	15A (10A)	600V	1.6V	4.6 °C/W	1500V	175°C	wk 30 (wk31)
 SDIP2B-26L	STGIB8CH60TS-L(E)	12A (8A)	600V	1.6V	2.9 °C/W	1500V	175°C	wk 33 (Q3 '15)
	STGIB10CH60TS-L(E)	15A (10A)	600V	1.6V	2.1 °C/W	1500V	175°C	wk 31 (wk32)
	STGIB15CH60TS-L(E)	20A (15A)	600V	1.6V	1.7 °C/W	1500V	175°C	wk 31 (wk 32)
	STGIB20M60TS-L(E)	25A (20A)	600V	1.6V	1.45 °C/W	1500V	175°C	wk 33 (Q4 '15)
	STGIB30M60TS-L(E)	35A (30A)	600V	1.6V	1.25 °C/W	1500V	175°C	wk 33 (Q4 '15)

Temperature sensing/protection

T = NTC on board
S = Temperature sensing

Leads finish option

- **E** = Short leads and emitter forward
- **L** = Long leads



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SLLIMM-nano: Overview

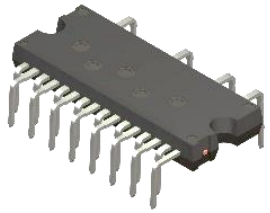
Today

- STGIPN3H60A (L6388 based)
- STGIPN3H60 (-H,E) (L6390 based features)
- STGIPN3H60T-H (L6390 based features)
- STGIPN3H60AT (L6388 based)

Coming soon…

STGIPQ3H60T-H(Z/L)

3A, 600V, NTC
IGBT Planar silicon based

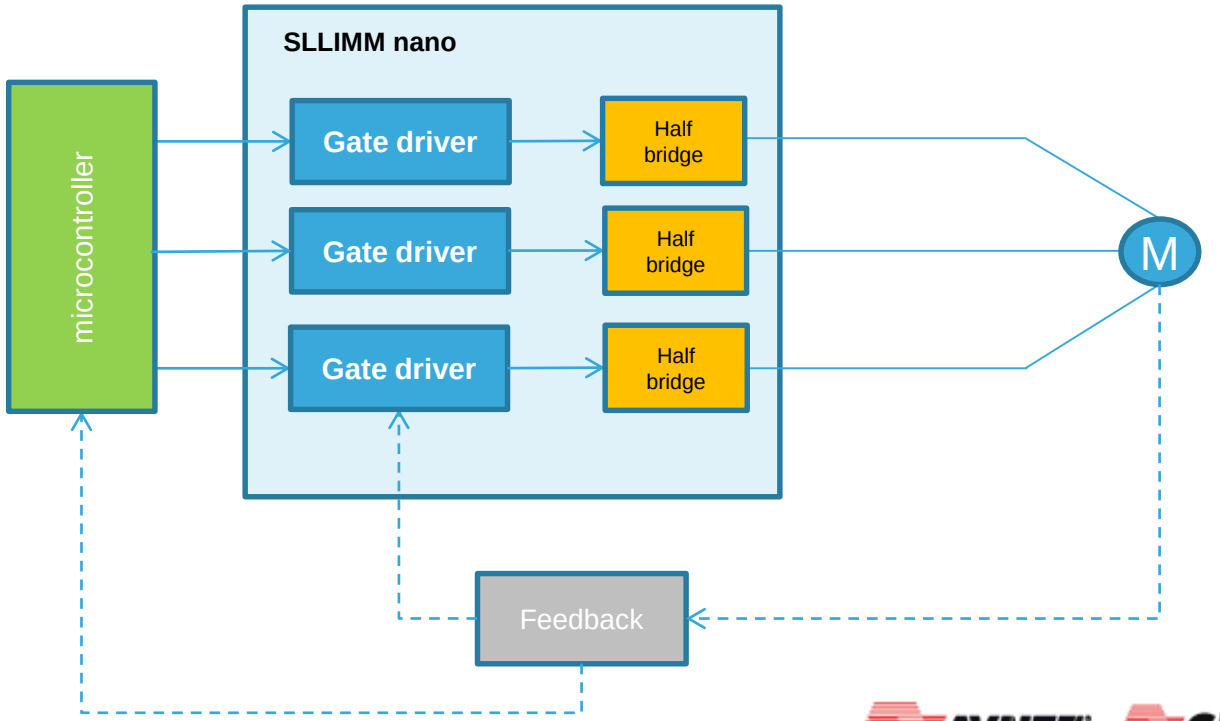


STGIPQ5C60T-H(Z/L)

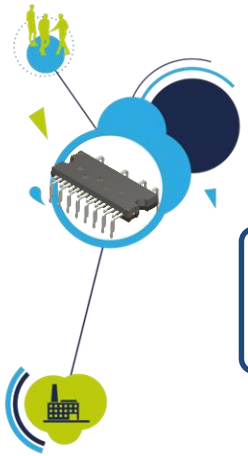
5A, 600V, NTC
IGBT TFS silicon based

SLLIMM nano series: introduction

The **SLLIMM nano** has been designed using an internal structure of the inverter stage that includes three half-bridge HVICs for gate driving and six IGBTs with freewheeling diodes.
In add to the first series of this product a new series has been introduced, **the new series shows a new package solution with mounted slots to allow a better and easy screw on heatsink.**
In add the in line version and the option with and without stand-off leads' packages are available.
The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited.
SLLIMM nano products show the best compromise between conduction and switching energy with an outstanding robustness and EMI behavior, making the product ideal to enhance the efficiency of compressor, pumps, fans and low power motors working up to 20 kHz in hard-switching circuitries.



SLLIMM nano series : Nomenclature



Package
N = NDIP-26L
Q = N2DIP-26L

Technology Series
C = Medium Frequency (4÷ 20 kHz) –(TFS)
H = High Frequency (8 ÷ 20 kHz) –(planar)

Leads finish option
L = in Line
Z = Zig-Zag
S= without stand-off

IGBT based

ST	G	IP	x	3	y	60	T-H	xx

SLLIMM™
(Intelligent Power Module)

Max Continuous Current (DC) @ 25˚C

Special features
A = basic embedded features
T = NTC on board
-H = STD Input Low Side Driving

Breakdown Voltage / 10

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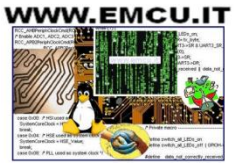

AVNET Memec

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SLLIMM nano series: Package Technology

General Features

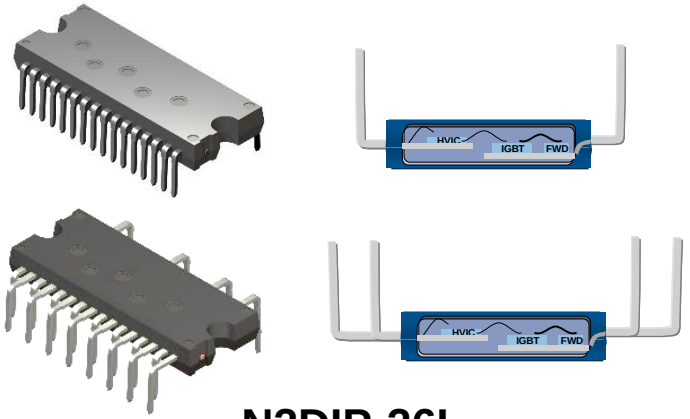
- DIP Molded Package (26 leads)
- Copper frame for signal stage
- **Mounted slots**
- **Allowed a better and easy screw on heatsink**
- **Improved Viso**
- With and **without stand-off**
- 2 leads options:
  - **In line leads**
  - Zig-Zag leads (pin to pin with 1st series)

In bold the improvement of 2nd series versus the first one

SLLIMM Nano

NDIP-26L

SLLIMM Nano 2nd series

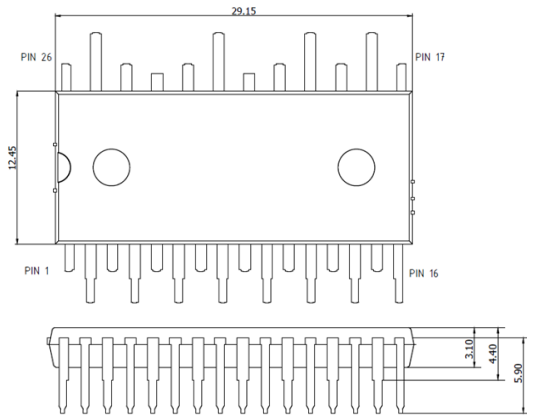


N2DIP-26L

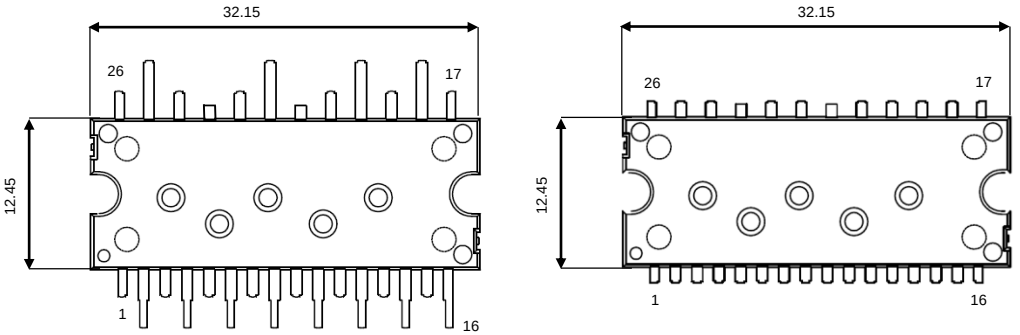
SLLIMM nano series: Package Technology

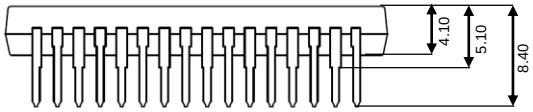
Zig-Zag versions
pin to pin compatible

Nano NDIP-26L

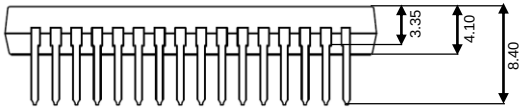


Nano 2nd series N2DIP-26L





Stand-off



No Stand-off

All measures are in mm

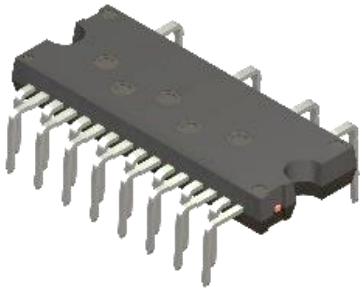
SLLIMM nano series: Product Features

Full Molded isolated package
Low power application

Smart shutdown
Effective failure protection

Comparator
Faults protection: overcurrent and short-circuit events

Op-amps
Advanced current sensing

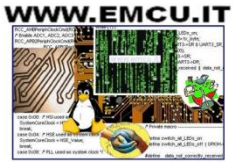


Deadtime and Interlocking function
Cross conduction prevention

Integrated Bootstrap diode
Reduced BOM and simplified layout

UVLO
Malfunctioning and fault prevention

NTC
Bult-in temperature sensing



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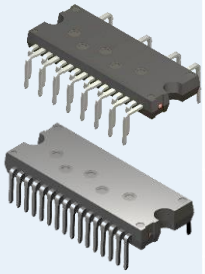
SLLIMM nano: Synoptic table

Package	Part number	Ic @ 25°C	Vcesat	Voltage	Viso	Samples (Mass Prod)
 NDIP-26L	STGIPN3H60A(T)	3A	2.15V	600V	1000V	DONE
	STGIPN3H60 (-H,E)	3A	2.15V	600V	1000V	DONE
	STGIPN3H60T-H	3A	2.15V	600V	1000V	DONE
 N2DIP-26L	STGIPQ3H60T-HZ(S)	3A	2.15V	600V	1500V	Done(wk30)
	STGIPQ3H60T-HL(S)	3A	2.15V	600V	1500V	Done(wk30)
	STGIPQ5C60T-HZ(S)	5A	1.65V	600V	1500V	Done(wk30)
	STGIPQ5C60T-HZ(S)	5A	1.65V	600V	1500V	Done(wk30)

T = NTC on board
-H = STD Input Low Side Driving
-E = ESD protection on board

Leads finish option

Z =zig zag leads
L = in line
S= without stand-off option

SLLIMM 2nd series main features

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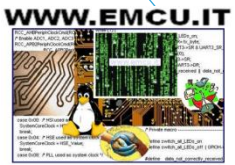
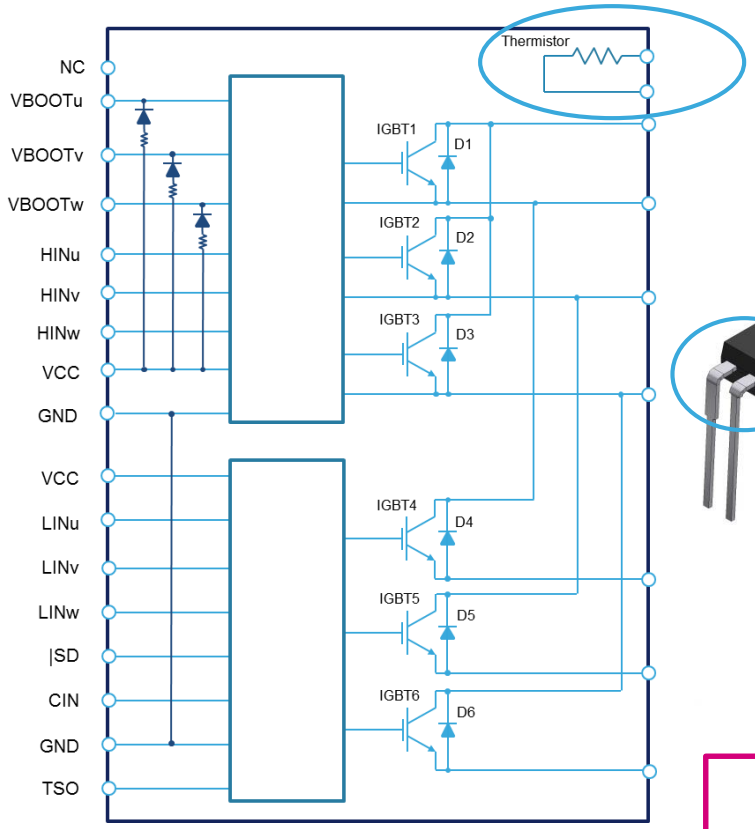
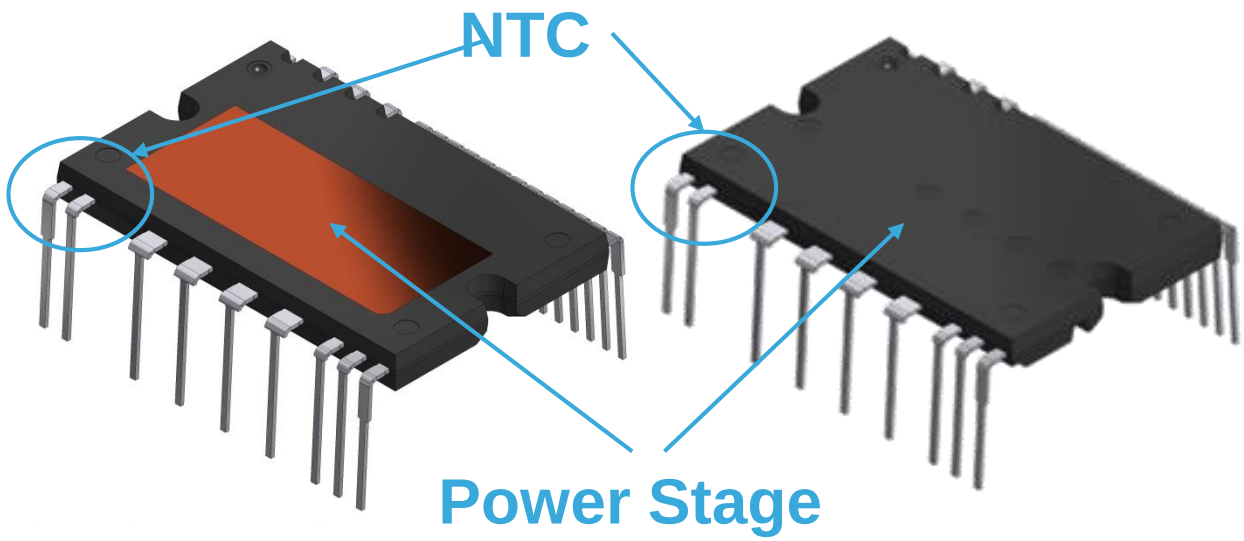


Main Features Summary

- NTC Thermistor
- Thermal sensor output
- Bootstrap Section
- Shutdown, Smart SD
- Internal Comparator
- UVLO Protection

SLLIMM™ Gen 2: NTC Thermistor

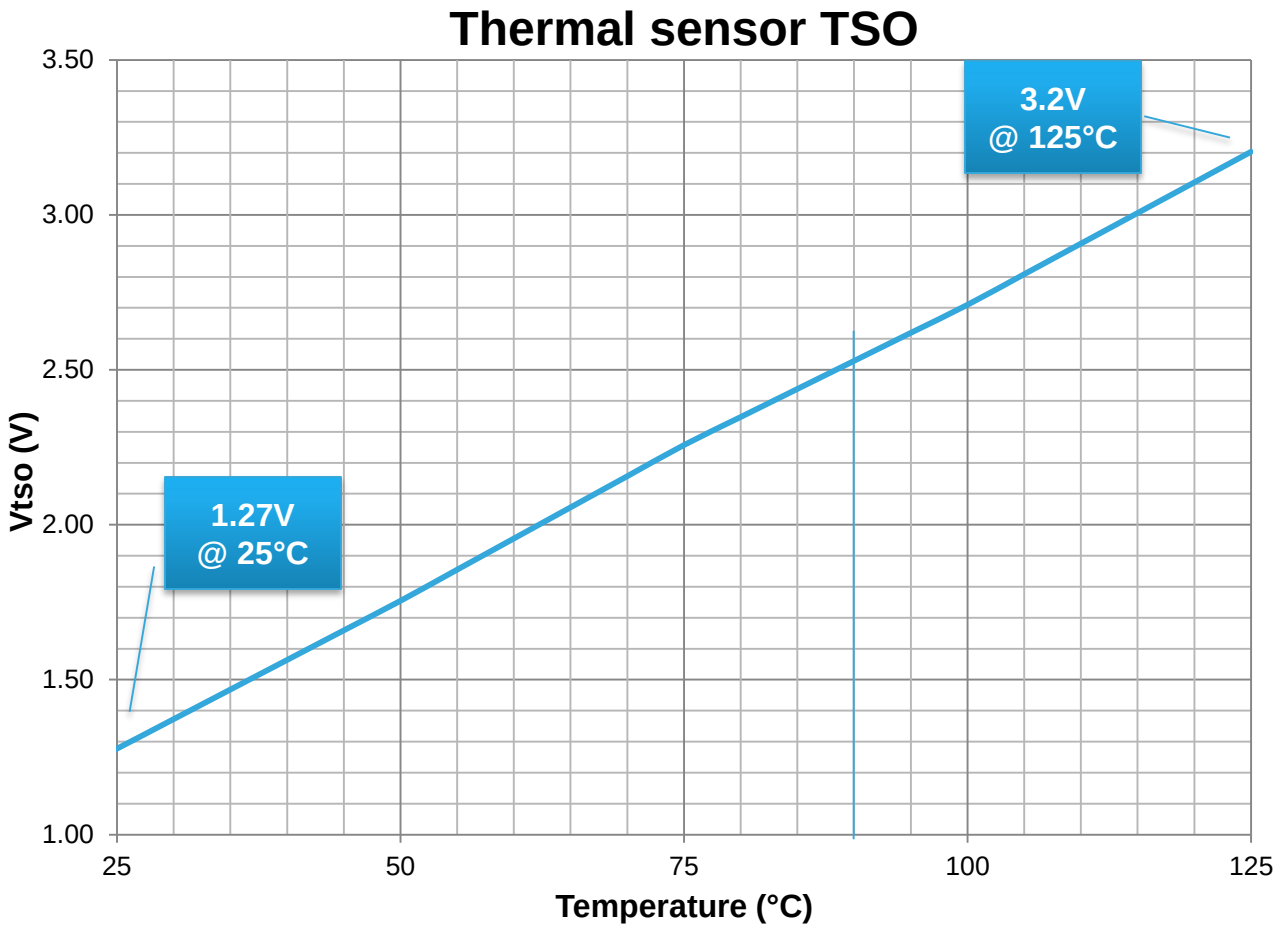




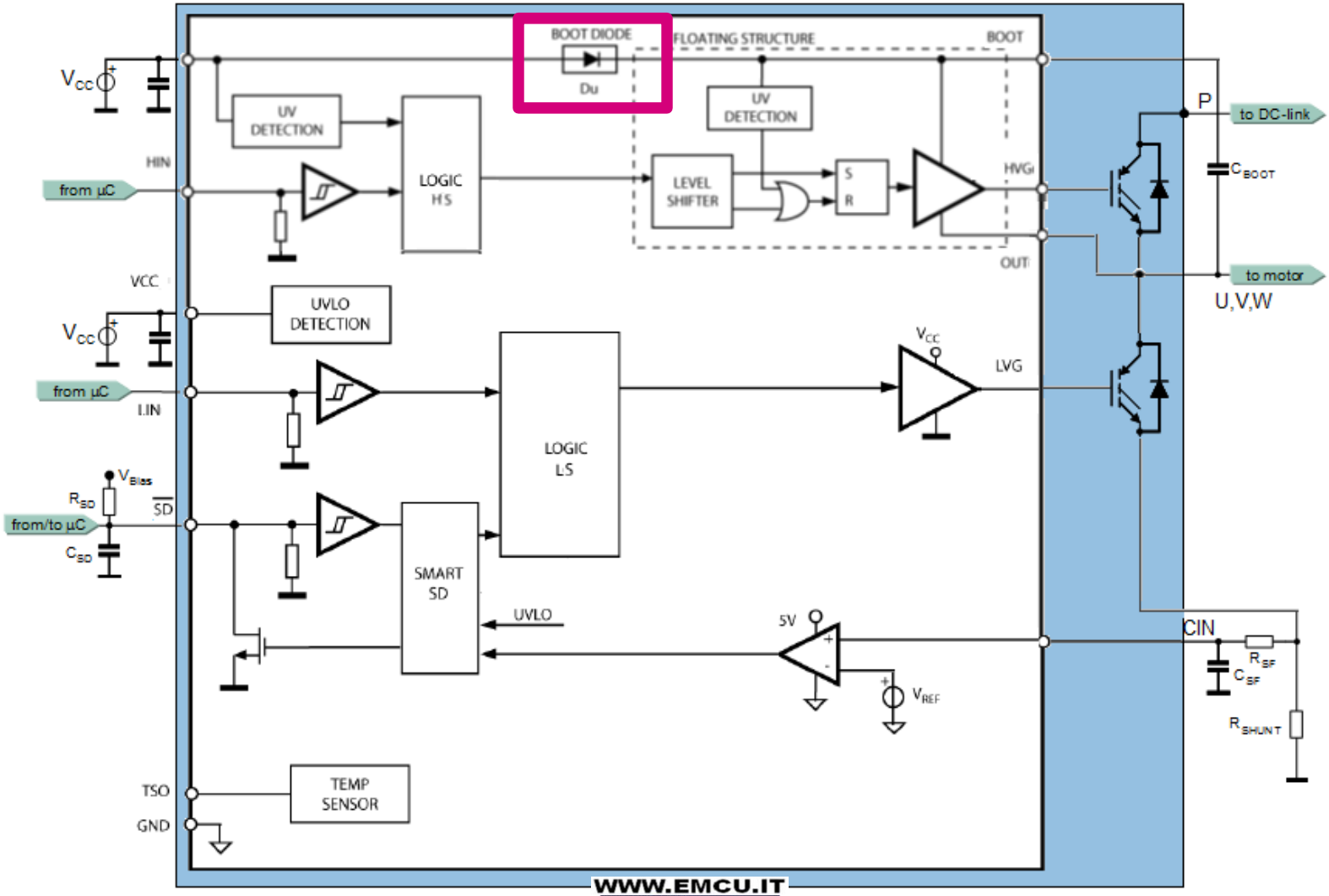
NTC is placed very close the power stage
for a more accurate temperature monitoring

Thermal Sensor Output

SLLIMM 2nd series



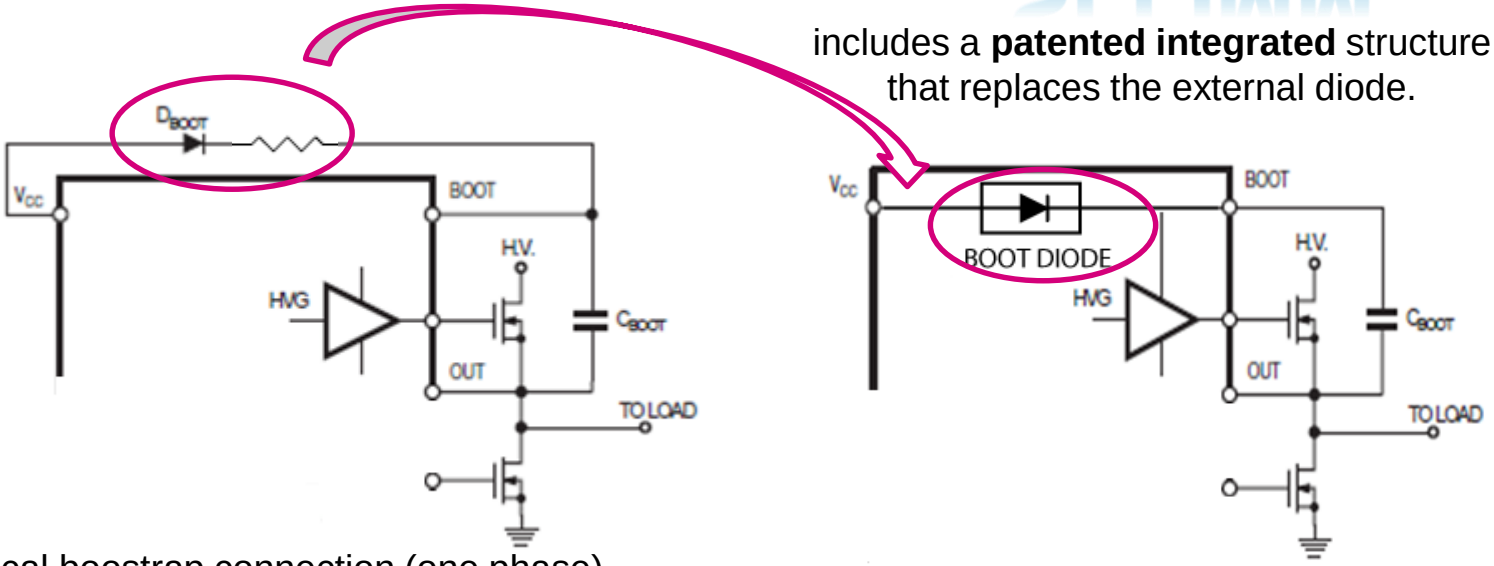
Bootstrap Block Diagram



Bootstrap Section

The easiest way to supply the high voltage section of the IPM is to realize a floating bootstrap power supply. This function is normally accomplished by a high voltage fast recovery diode plus a small series resistor.

SLLIMM includes a **patented integrated** structure that replaces the external diode.

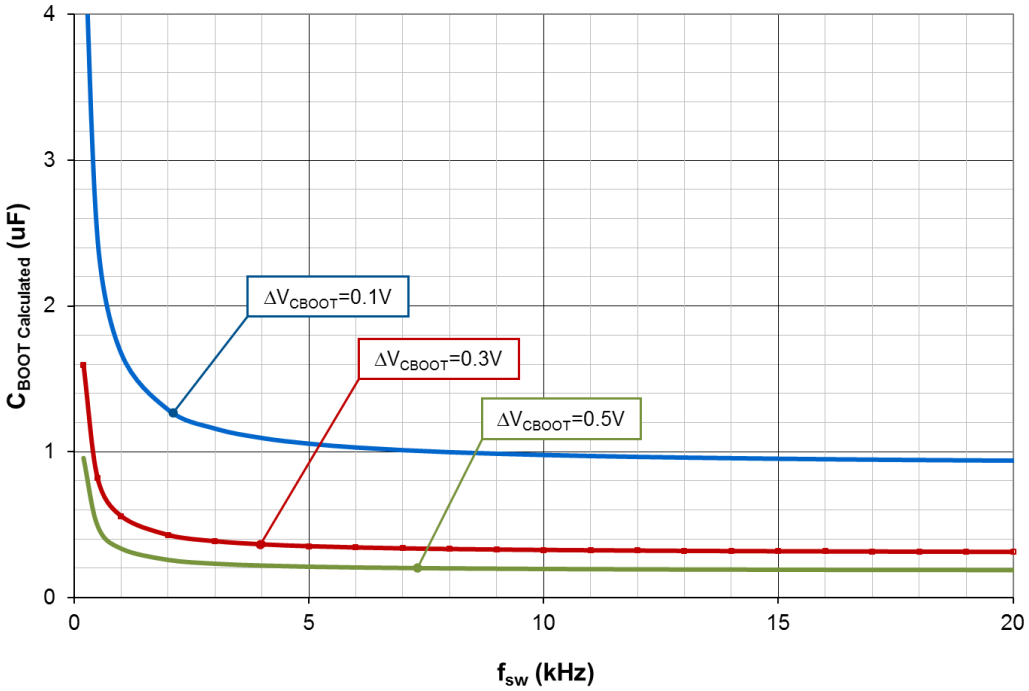


Typical boostrap connection (one phase)

- **Less passive components on the PCB board: easy layout**
- **Higher integration level means less assembly step → HIGHER RELIABILITY**

Suggested value for bootstrap capacitor

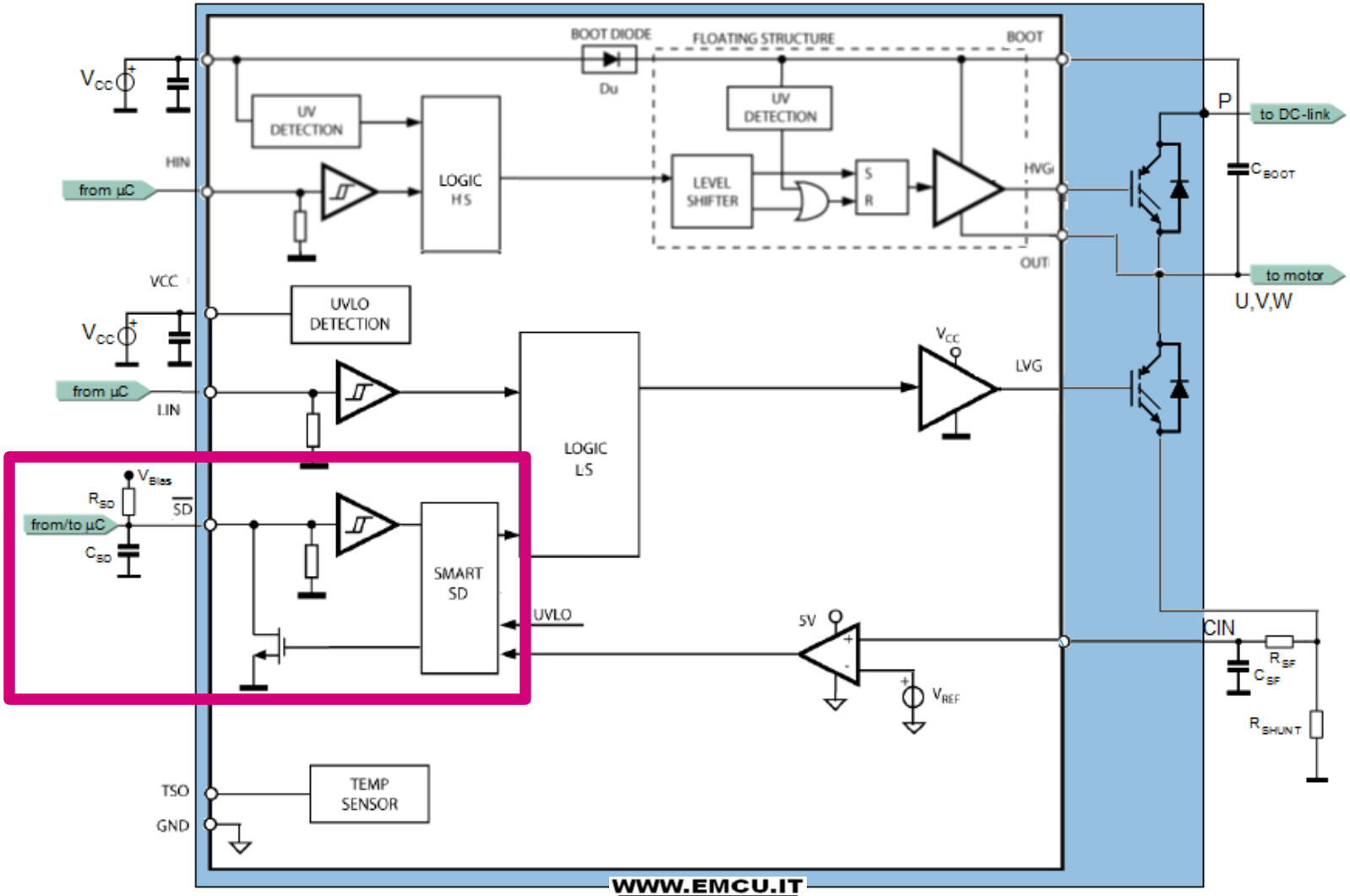
In order to help customer during the design phase, ***ST*** will provide the *suggested* bootstrap capacitors values for a given conditions.



- Continuous sinusoidal modulation
- Duty cycle δ = 50%
- V_{CC} = 16.5V
- Can be used as a worst case for all the SLLIMM IPM

Considering the limit cases during the PWM control and further leakages and dispersions in the board layout, the capacitance value to use in the bootstrap circuit must be selected two or three times higher than the CBOOT calculated in the above graph.

Shutdown Block Diagram



Shutdown Function (SD)

/SD-OD is an **input-output pin**.
It can be used by the microcontroller to rapidly shutdown the SLLIMM (see below truth table) or can be used by the SLLIMM to inform the microcontroller that a fault condition occurred.

/SD function truth table

Condition	Inputs			Outputs	
	$\overline{SD}$	LINx	HINx	LVGx	HVGx
Shutdown enable half-bridge tri-state	L	X	X	L	L
0 "logic state" half-bridge tri-state	H	L	L	L	L
1"logic state" low side direct driving	H	H	L	H	L
1"logic state" high side direct driving	H	L	H	L	H

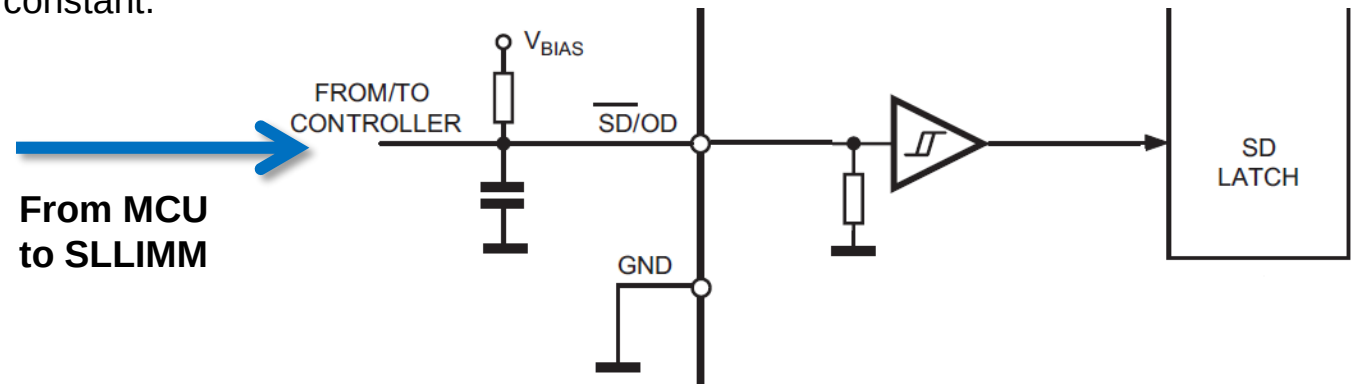
Note: X: don't care

Whatever are the input signals, if the SD function is activated (active low) the output signals are always OFF

Shutdown Function (SD)

Shutdown signal from MCU

Just connect the /SD pin to the MCU with a simple pull-up resistors. Add an RC block to fix the re-enable time constant.



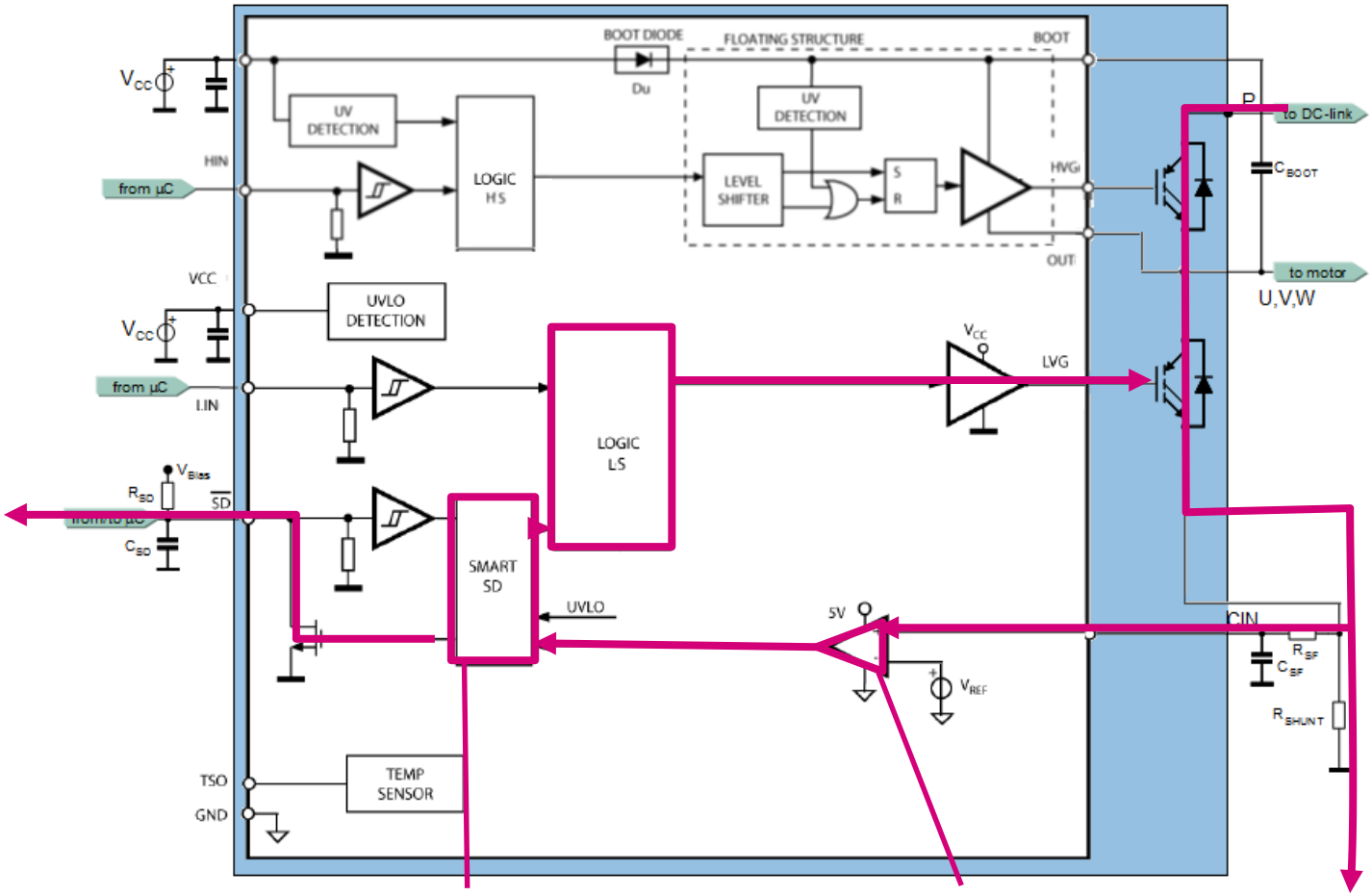
To properly size the RC block please consider that you must ensure that the proper voltage level is maintained to enable/disable the SLLIMM. Please refers to the following table:

Symbol	Parameter	Min	Typ	Max
VIL	Low logic level voltage			0.8V
VIH	High logic level voltage	2.25V		

To enable SLLIMM by MCU -> VSD > VIH(min)
To disable SLLIMM by MCU -> VSD < VIL(max)

Shutdown Function (SD)

Shutdown signal from SLLIMM



Smart SD uses a preferred internal pat minimize the delay time

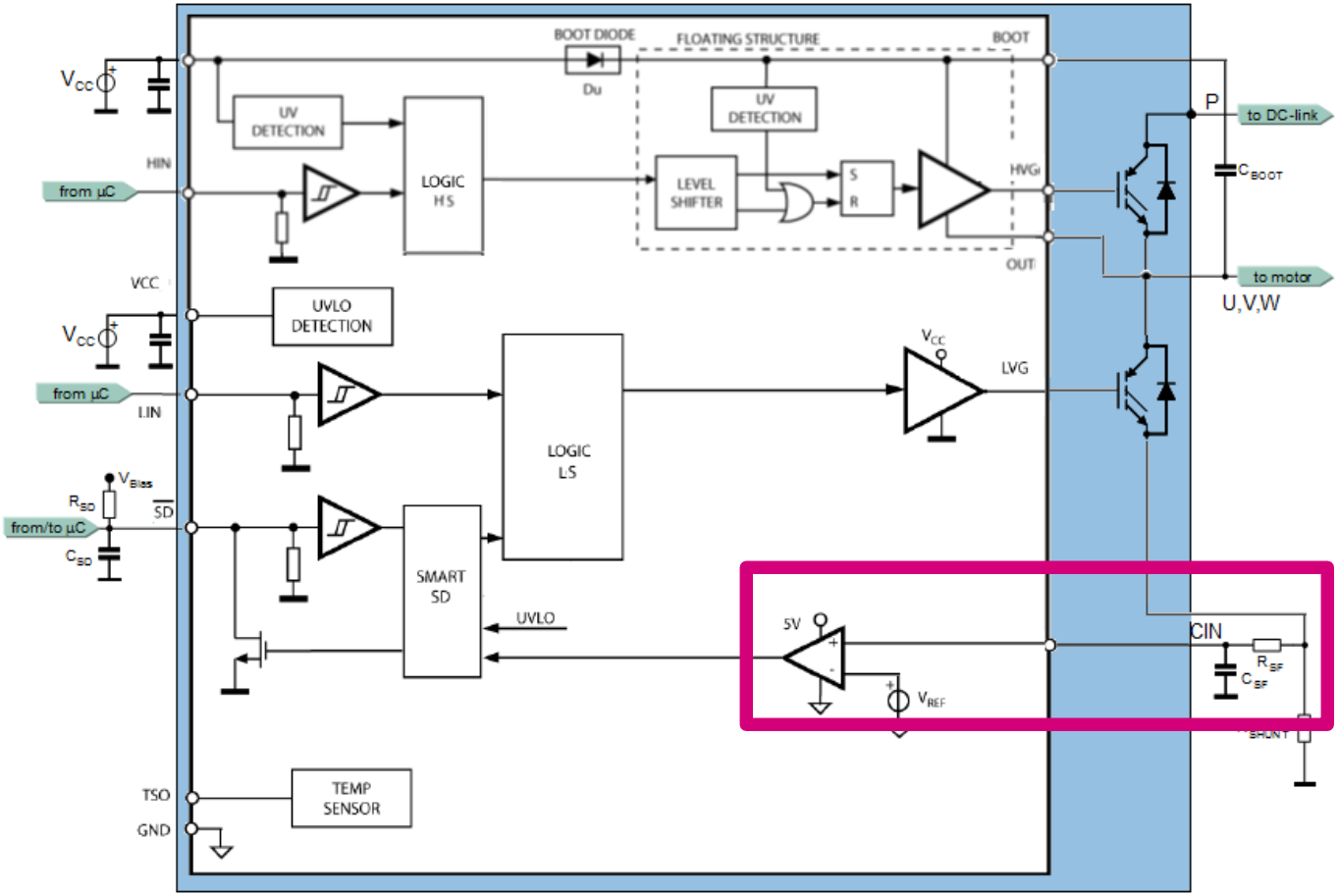
Overcurrent

Smart SD

- Shutdown internally the IGBTs in 290ns
- Inform the MCU (act as FAULT signal)

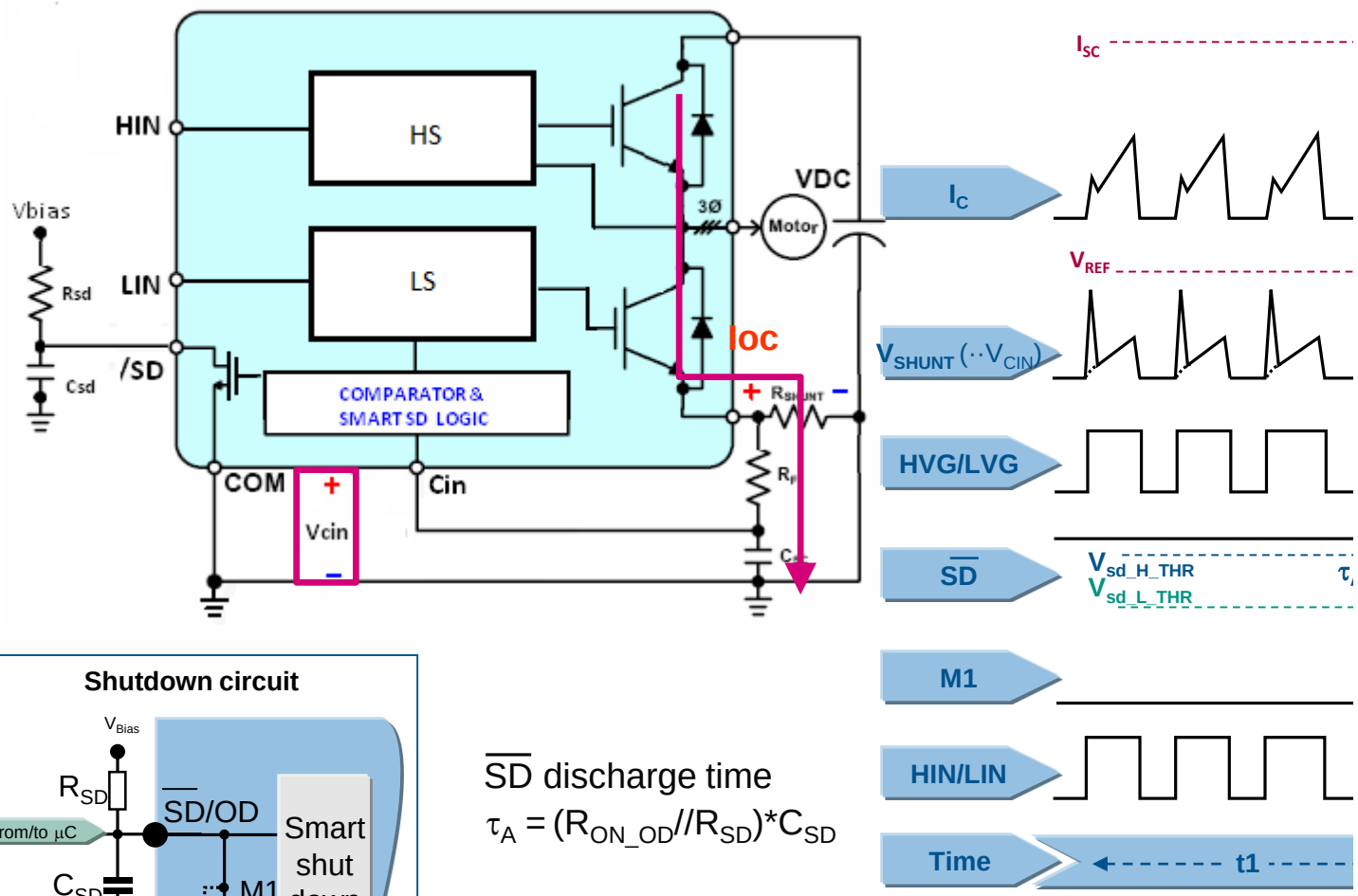
The internal comparator can be used to realize OCP

Comparator Block Diagram



Comparator and Smart Shutdown (SSD)

Over-current event

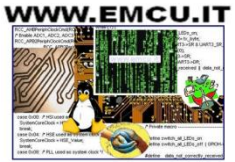


$\overline{SD}$ discharge time

$\tau_A = (R_{ON\_OD} // R_{SD}) * C_{SD}$

$\overline{SD}$ recharge time

$\tau_B = R_{SD} * C_{SD}$



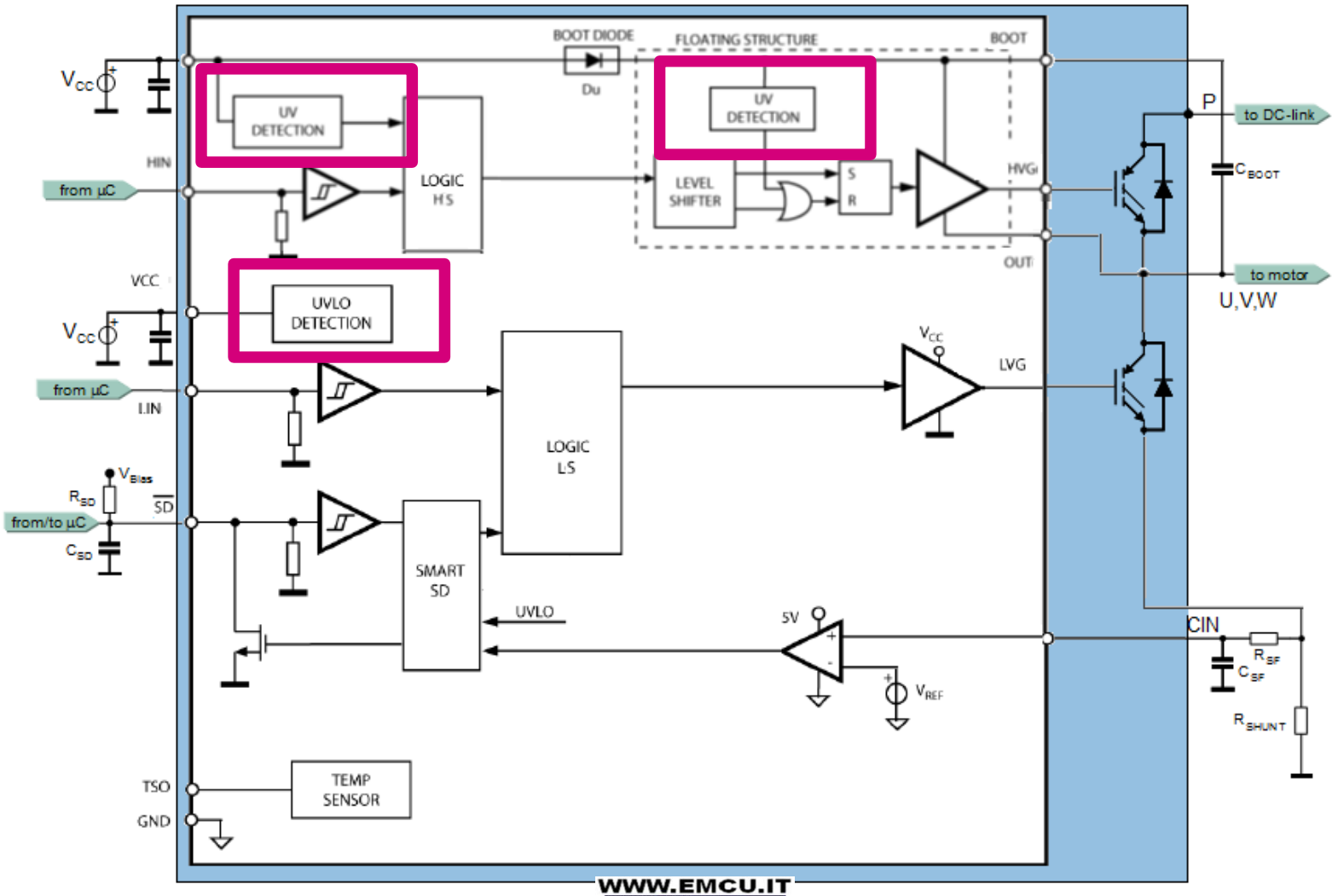
Fault signals

SLLIMM 2ND SERIES

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Over-current event	≤ 20 µs	20 µs
		≥ 20µs	OC time
UVLO	Under-voltage lock out event	≤ 50 µs	50µs
		≥ 50µs until the VCC exceed the VCC UV turn ON threshold	UVLO time

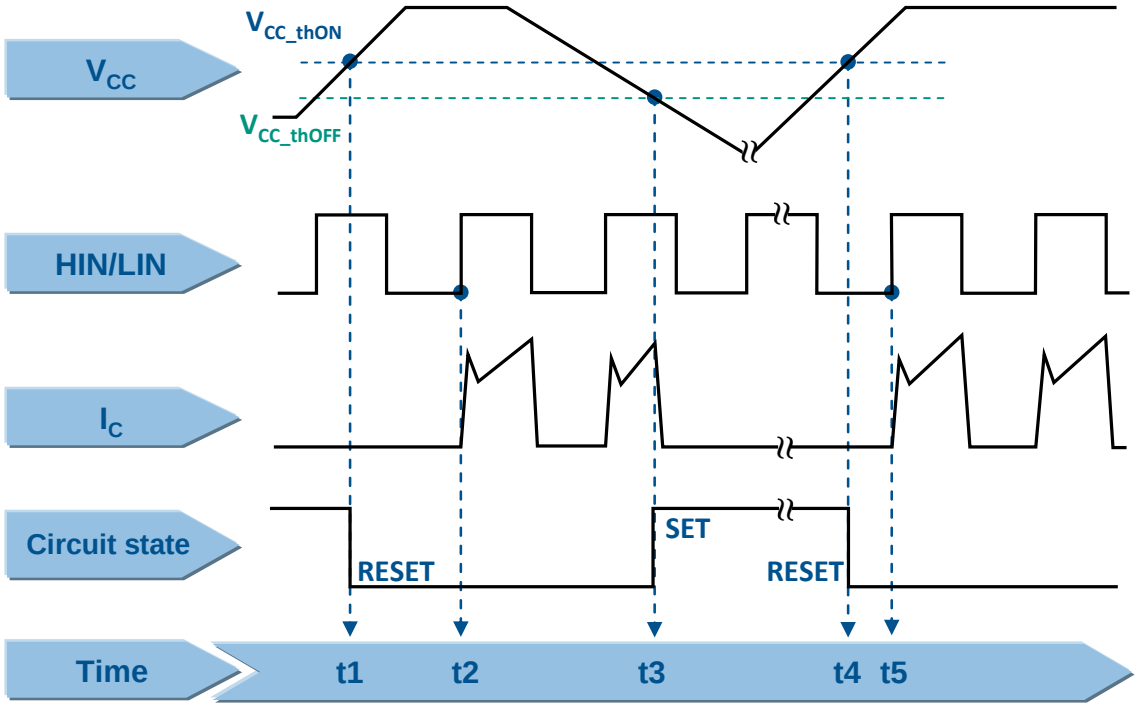
Fault timings						
t_{OC}	Overcurrent fault time	Full Temperature range	14	20	26	µs
t_{UVLO}	UVLO fault time	Full Temperature range	35	50	65	µs

UVLO Block Diagram



Undervoltage Lockout Function (UVLO)

UVLO: If Vcc or Vboot voltages go below the UVLO_thOFF, the driver is shut down to avoid any high-power-dissipation condition for the IGBT or improper functioning of SLLIMM.



- t1: VCC>VCC_thON the SLLIMM starts
- t2: HIN/LIN is on and the IGBT is turned on
- t3: VCC<VCC_thOFF the UVLO event is detected. The IGBT is turned off
- t4: VCC>VCC_thON the SLLIMM re-starts
- t5: HIN/LIN is on and the IGBT is turned on again

ST STGIF5CH60 vs. Main Competitor ver.1, Main Competitor ver.2

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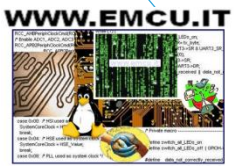
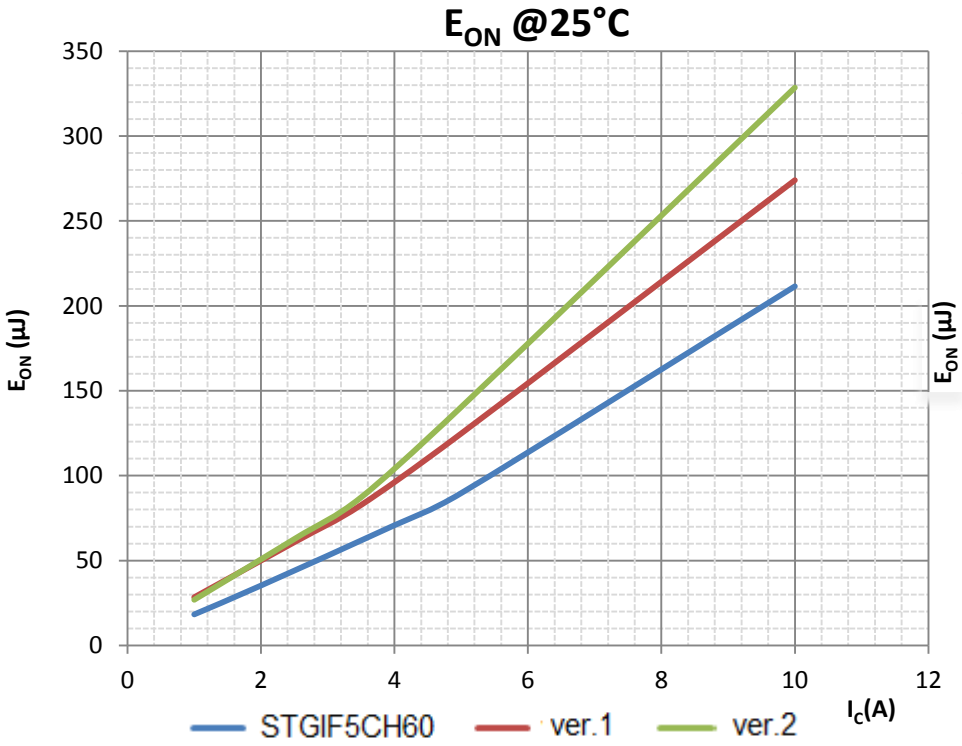
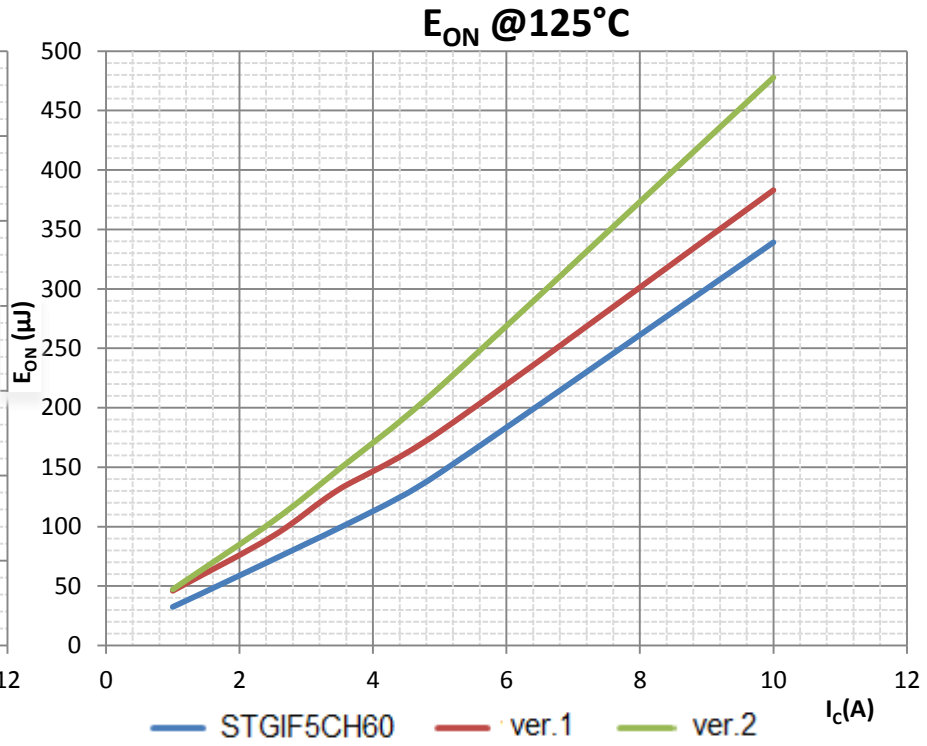


Synoptic Table

Device	STGIF5CH60TS-E T - NTC on board S - integrated temperature sensor E - (short leads), L (long leads)	Main Competitor ver.1	Main Competitor ver.2
Voltage (V)	600	600	600
Current @ T_C = 25°C (A)	8	5	5
$R_{th(j-c)}$ max single IGBT (°C/W)	5.0	4,7	5
Package type	SDIP2F-26L FULL MOLDED	DBC	DBC
Number of pin	26 (NTC on board optional) 25	25	25
Package size (mm) X, Y, Z	38.0x24.0x3.5	38.0x24.0x3.5	38.0x24.0x3.5
Integrated bootstrap diode	Yes	Yes	Yes
SD/FAULT function	Yes	Yes	Yes
Comparator for fault protection	Yes (1 pin)	Yes (1 pin)	Yes (1 pin)
Smart shutdown function	**Yes**	**No**	**No**
Protection	Under voltage protection (UV) Short circuit protection (SC) Over temperature protection (OT) (optional)	Under voltage protection (UV) Short circuit protection (SC) Over temperature protection (OT) (optional)	Under voltage protection (UV) Short circuit protection (SC) Over temperature protection (OT) (optional)
Fault event monitoring	UV - SC - OT (optional) **different timing feedback per event**	UV – SC **no differentiations per event**	UV – SC **no differentiations per event**
Temperature monitoring	Temperature sensor **NTC sensor on board (optional)**	Temperature sensor (optional)	Temperature sensor (optional)
Undervoltage lockout	Yes	Yes	Yes
Open Emitter configuration	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)
Emitter forward	(short lead type) STGIF5CH60xy-E	short lead type	short lead type

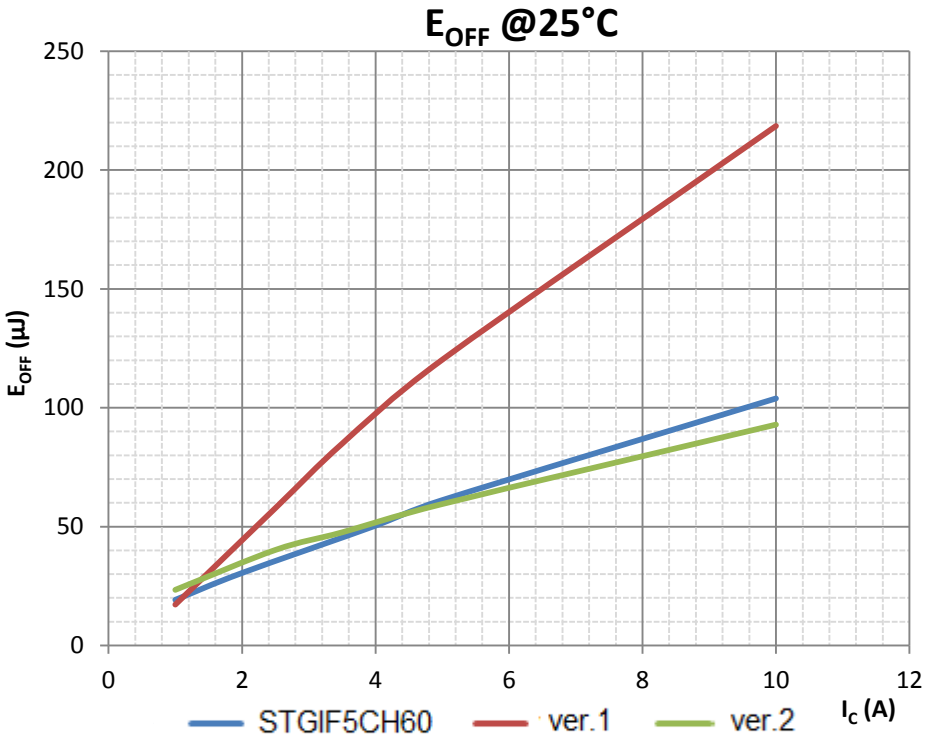
Dynamic Comparison: IGBT E_{ON}

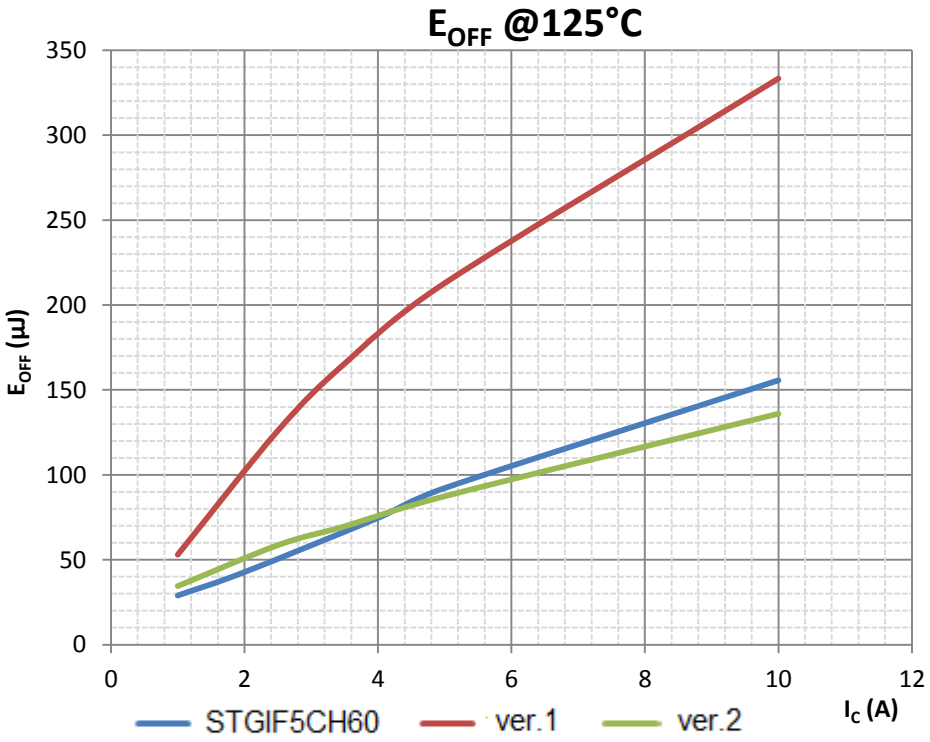




STGIF5CH60 shows better dynamic performance, during the ON phase, in all the range of current and in both junction temperatures.

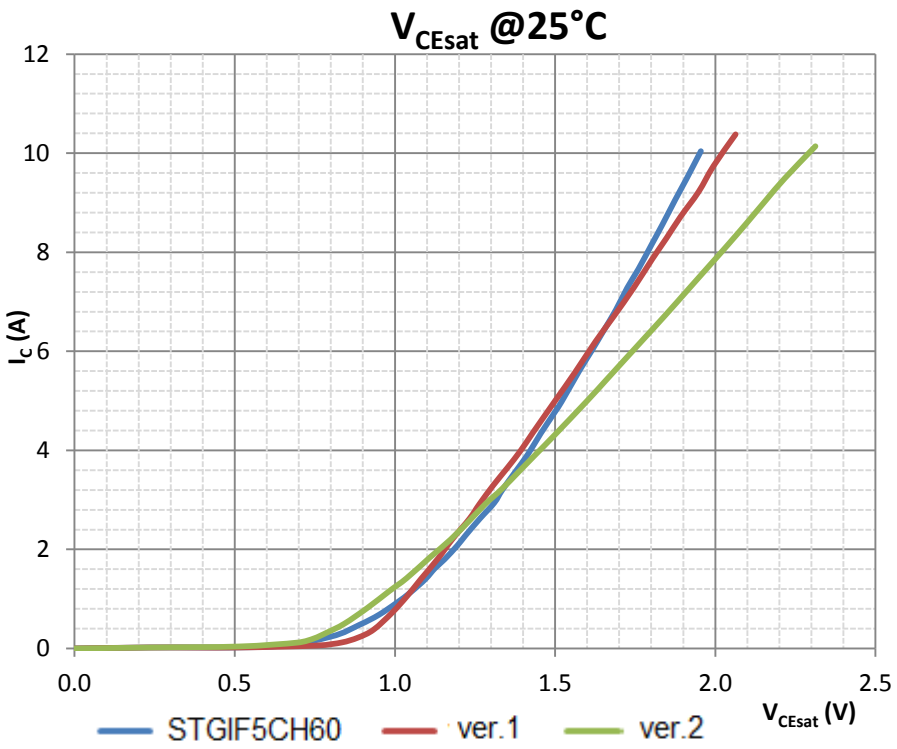
Dynamic Comparison: IGBT E_{OFF}

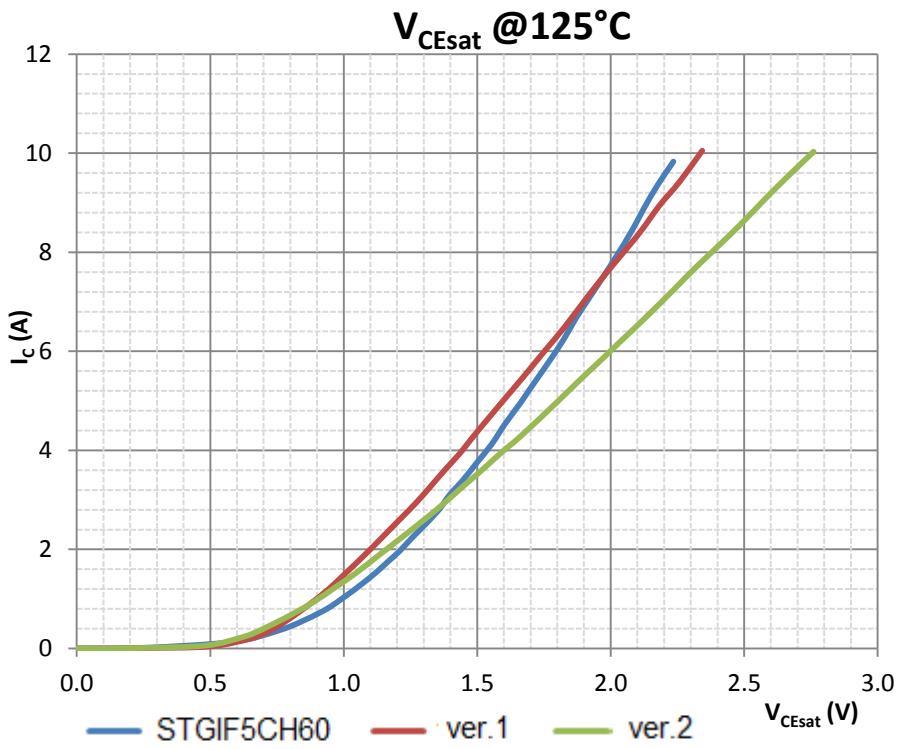




STGIF5CH60 shows a much better dynamic performance, during the ON phase, in all the range of current and in both junction temperatures compared to Main Competitor ver.1. Comparable behavior with Main Competitor ver.2.

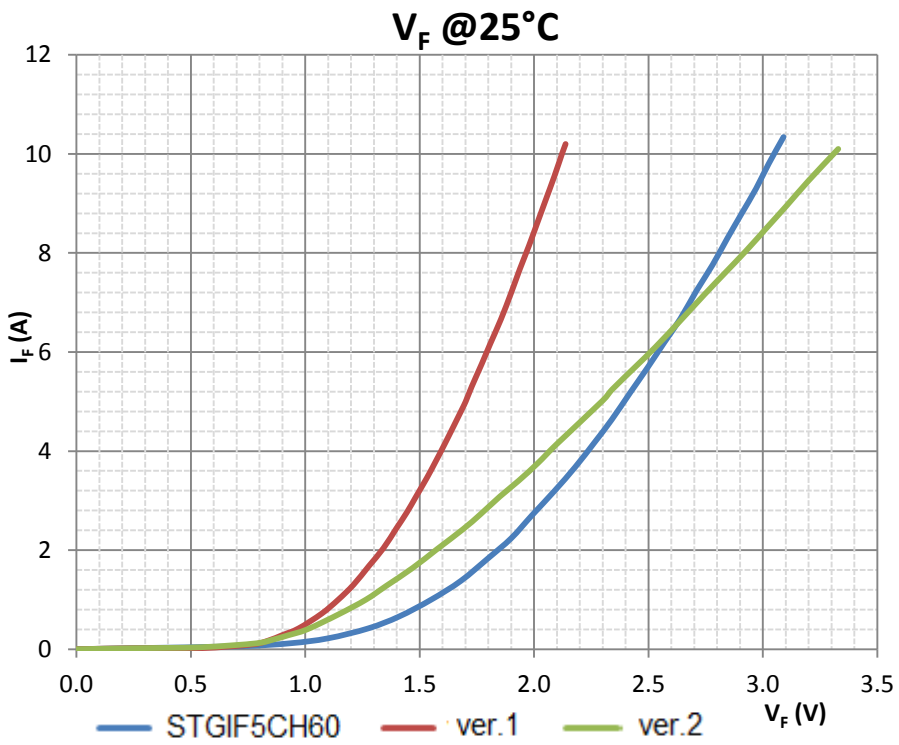
Static Comparison: IGBT $V_{CE\ sat}$

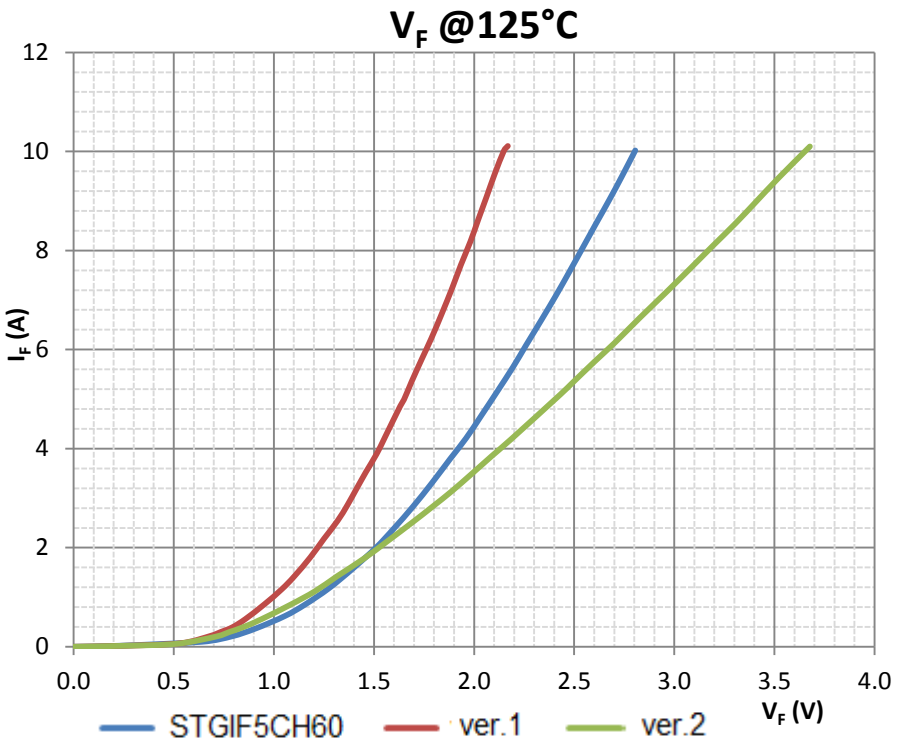




STGIF5CH60 vs. Main Competitor ver.1: similar behavior @25°C, slightly worse @125°C (up to 3.5 A).
STGIF5CH60 vs. Main Competitor ver.2: slightly worse behavior in both conditions of junction temperature (up to 3.5 A).

Static Comparison: FW diode V_F



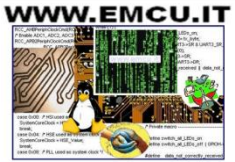


STGIF5CH60 vs. Main Competitor ver.1: has a worse behavior in term of forward voltage of antiparallel diode in both conditions of junction temperature.
STGIF5CH60 vs. Main Competitor ver.2: worse behavior @25°C and similar or better @125°C.

Simulation Parameters

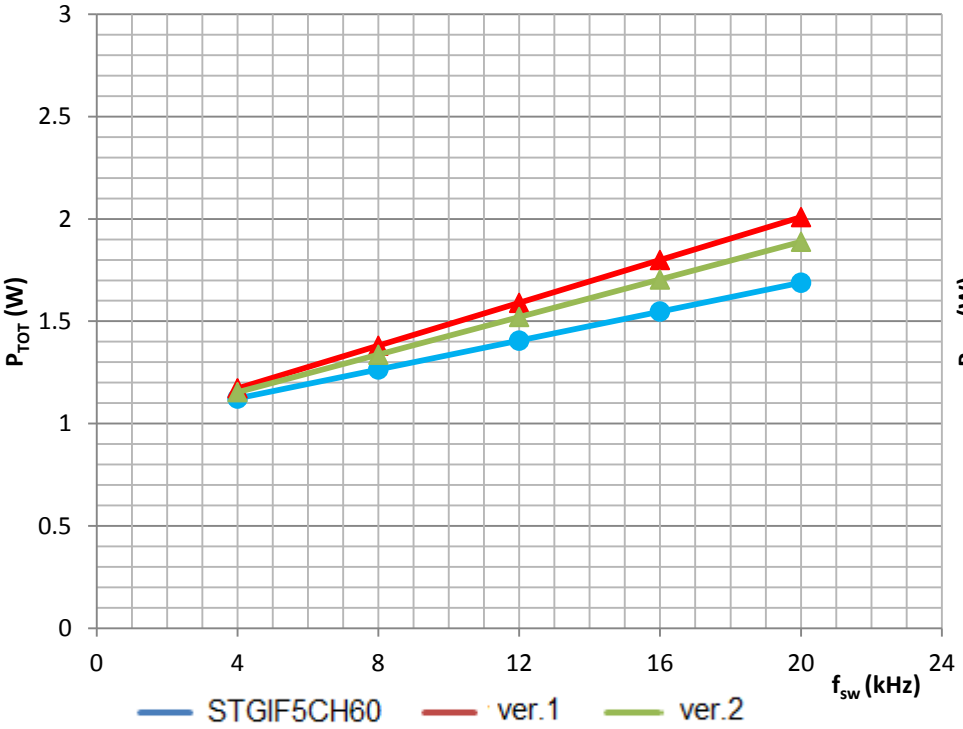
- V_{bus}= 300V
- ma= 0.8
- PF= 0.6
- f_{sine}= 60Hz
- f_{sw}= up to 20kHz
- I_{peak}= 3.5 A
- V_{CEsat}, V_F= typical values measured @ 25˚C & 125˚C
- E_{ON}, E_{OFF}= typical values measured @ 25˚C & 125˚C
- Gate driving conditions= internal, due to IPM configuration

Total power loss were evaluated

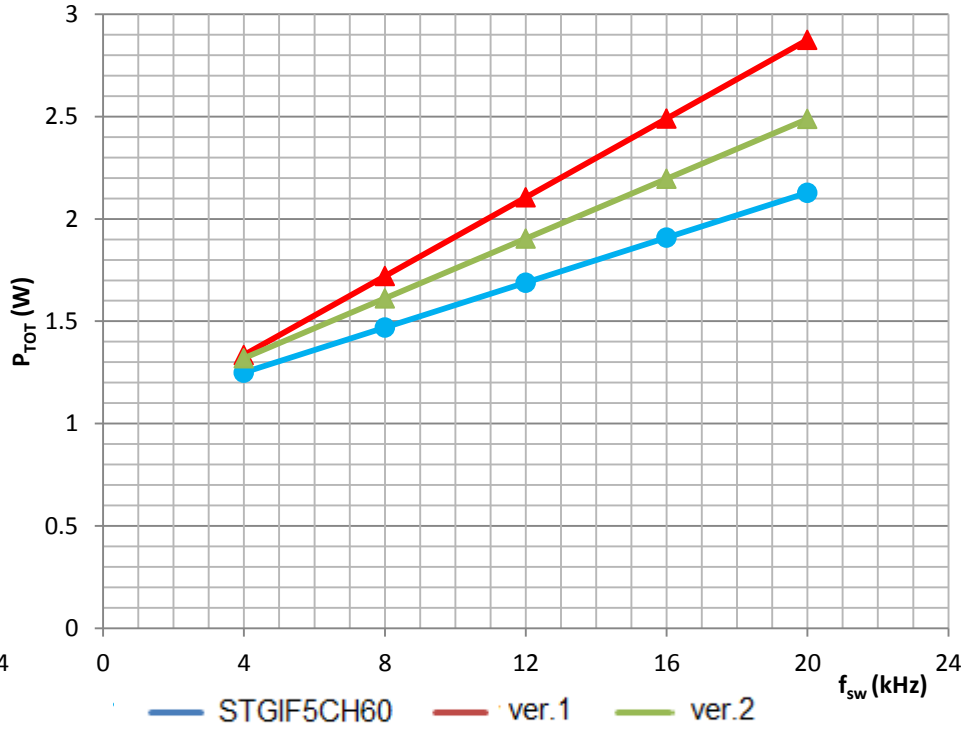


IGBT Total Power Loss @3.5A

Ipeak= 3.5 A, Tj= 25 °C



Ipeak= 3.5 A, Tj= 125 °C



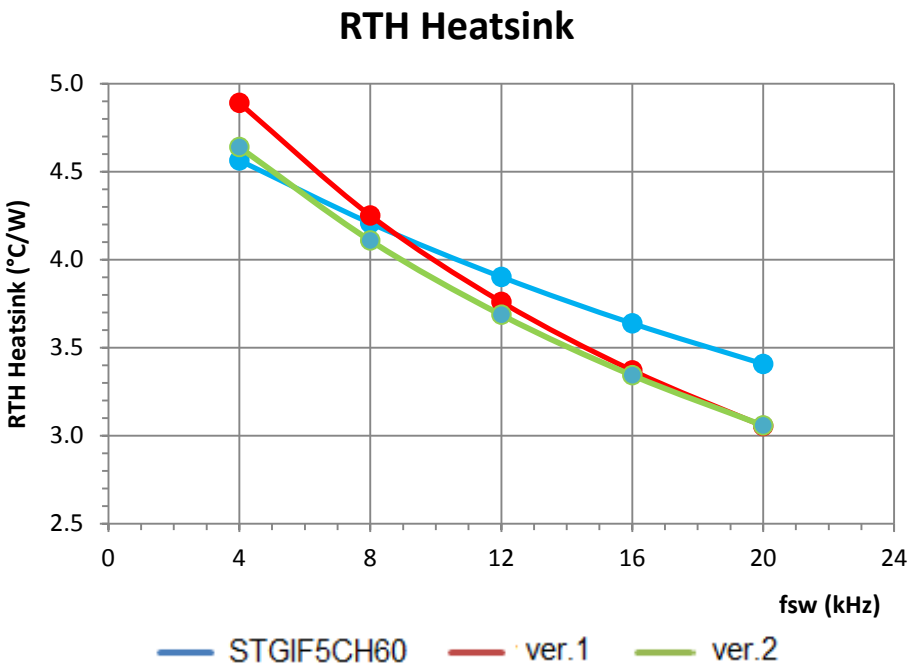
Single IGBT of STGIF5CH60 has a better efficiency in both junction temperature conditions and in all the range of frequency under analysis, than competitors.

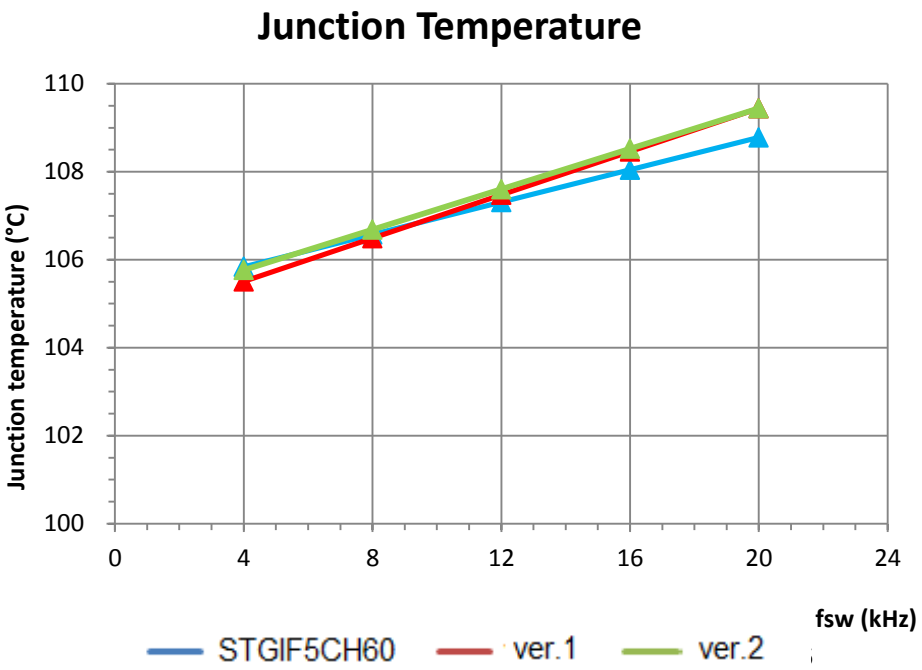
Thermal simulation

The thermal behavior of the devices under comparison was analyzed considering the following test conditions:

- **T_{case} fixed @100˚C:** assuming the same case temperature (T_C=100˚C), ambient temperature (Ta=50˚C) and current (Ipeak=3.5A) the thermal resistance of the required heatsink and the junction temperature were calculated.

Test 1: T_{case} fixed @100˚C





In order to keep the same case temperature (T_C=100°C), STGIF5CH60 requires a smaller heatsink than Main Competitor ver.2, in almost all the range of switching frequencies. Compared to Main Competitor ver.1 it requires a smallest heatsink starting from about 8kHz. This allows smaller size and lower costs solutions (thanks to the lower power dissipation).
No particular differences in terms of junction temperatures.

Layout guidelines for EMC improving

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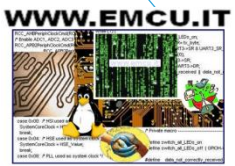
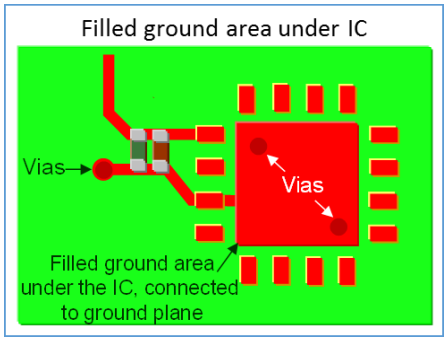


Ground

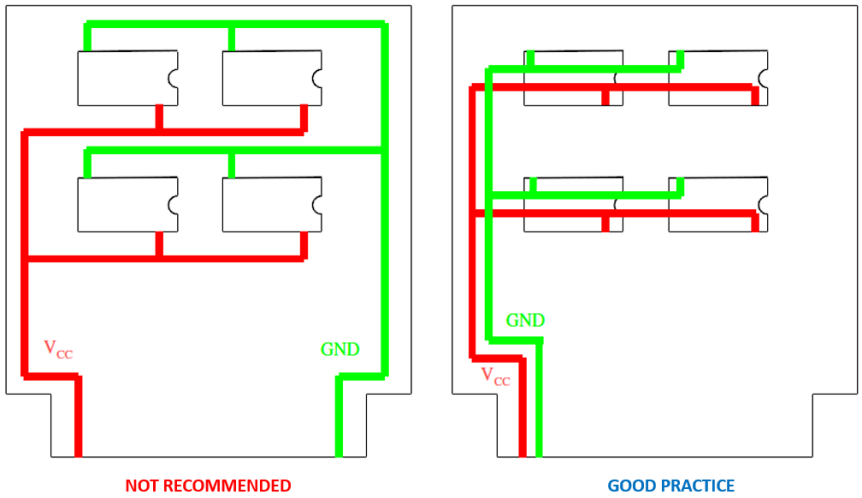
- separate signal ground tracks from power ground tracks and connect with at a single star connection directly on the shunt resistors
- wide ground traces reduce parasitic inductance
- fill unused board spaces with copper areas connected to the ground plane, especially underneath all the high frequency IC



- when more than one power supply is required, separate the power and ground tracks
- when a multilayer PCB is used, implement a complete ground layer or place ground traces in parallel with power traces to keep the supply clean

Power 1/3

- route parallel to ground on the same or adjacent layers to minimize loop area wide ground traces reduce parasitic inductance

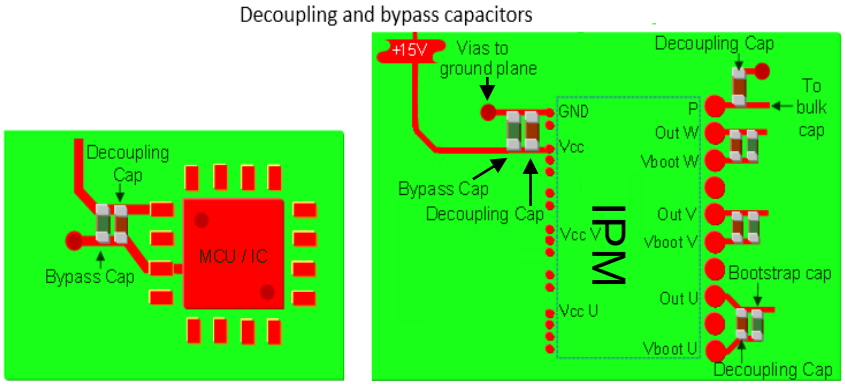


- PCB planes or wide traces reduce parasitic inductance

- bypass capacitors (aluminum or tantalum) placed as close as possible to each IC and IPM reduce the transient circuit demand on the power supply

Power 2/3

- decoupling capacitors (with low ESR) placed as close as possible in parallel with the bypass capacitor reduce high frequency switching noise on the power supply lines



- decoupling capacitors (with low ESR) placed as close as possible in parallel with the bypass capacitor reduce high frequency switching noise on the power supply lines

- a 21 V Zener diode connected to each power supply pin prevents surge destruction

Power 3/3

- a decoupling capacitor (with low ESR) in parallel with each bootstrap capacitor filters high frequency disturbances
- a 21V Zener diode in parallel with each bootstrap capacitor prevents surge destruction
- a decoupling capacitor (with low ESR) in parallel with the electrolytic bulk capacitor filters surge voltage; both capacitors should be placed as close as possible to the power device (the decoupling capacitor has priority over the bulk capacitor)
- use low inductance shunt resistors for phase leg current sensing
- minimize the wiring length between the shunt resistor and power ground to avoid malfunctions
- connect signal ground and power ground at only one point (near the terminal of the shunt resistor) to avoid any malfunction due to power ground fluctuation

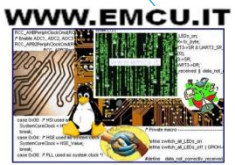
Signal

- increase the distance between adjacent tracks and separate them to minimize capacitance coupling interference
- place sensitive and high frequency away from high noise power tracks
- on double-layers boards, place signal and power tracks on the same side and ground on the other
- do not use wire jumpers, minimize layer transitions for critical signal traces and keep the same number of vias on each signal track where necessary

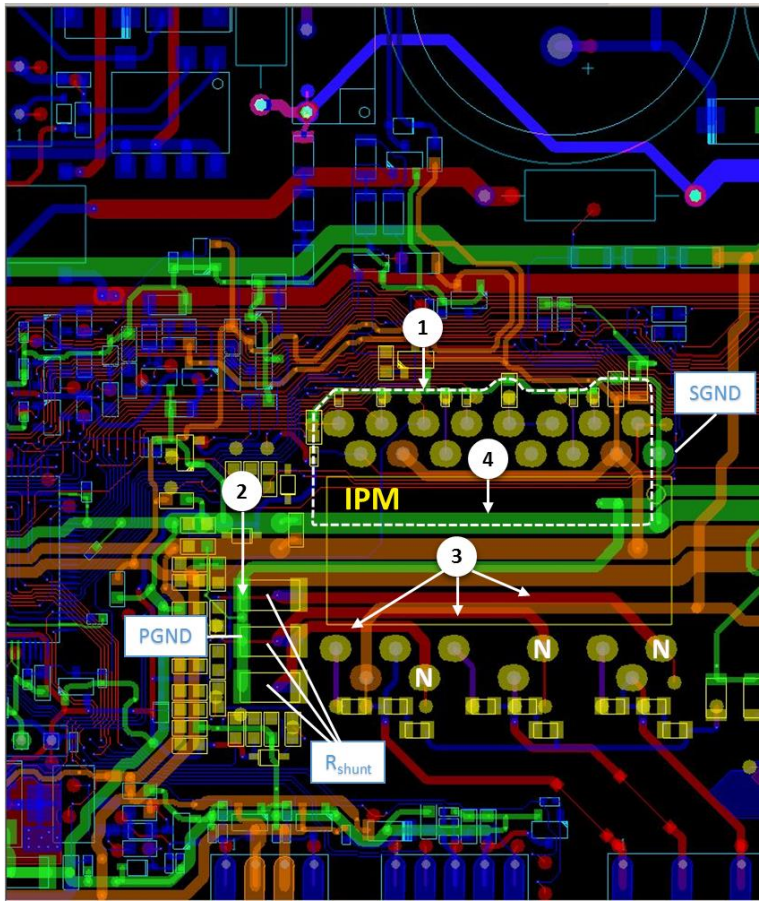
- group components according to their functionality (analog, digital, power, low-speed and high-speed sections)
- place a filter at subsystem boundaries to promote signal flow between different sections
- minimize the number of vias, especially in the high frequency signal tracks, as they introduce parasitic impedance; distribute them around the PCB, avoiding concentrations in small areas
- prefer star connections to stub connections, especially on critical signal tracks, as the latter produces reflections
- keep a constant signal track width during the entire routing as variations change its impedance and produce reflections
- unused pins cannot be unconnected and must be pulled-up or pulled-down
- respect current flow in layout design in EMI input filters

Practice case studies

life.augmented



Expample 1



1. ground tracks form a closed loop (white dashed line) which may increase EMC problems by introducing noise into the ground (due to high voltage switching tracks) and affect driver or application performance

2. the signal ground (SGND) of the IPM is connected away from the power ground (PGND); all signal grounds must be connected in a star configuration to the power ground

3. the shunt resistors are too far from the N-pins of the IPM and connected asymmetrically (the net lengths are too dissimilar)

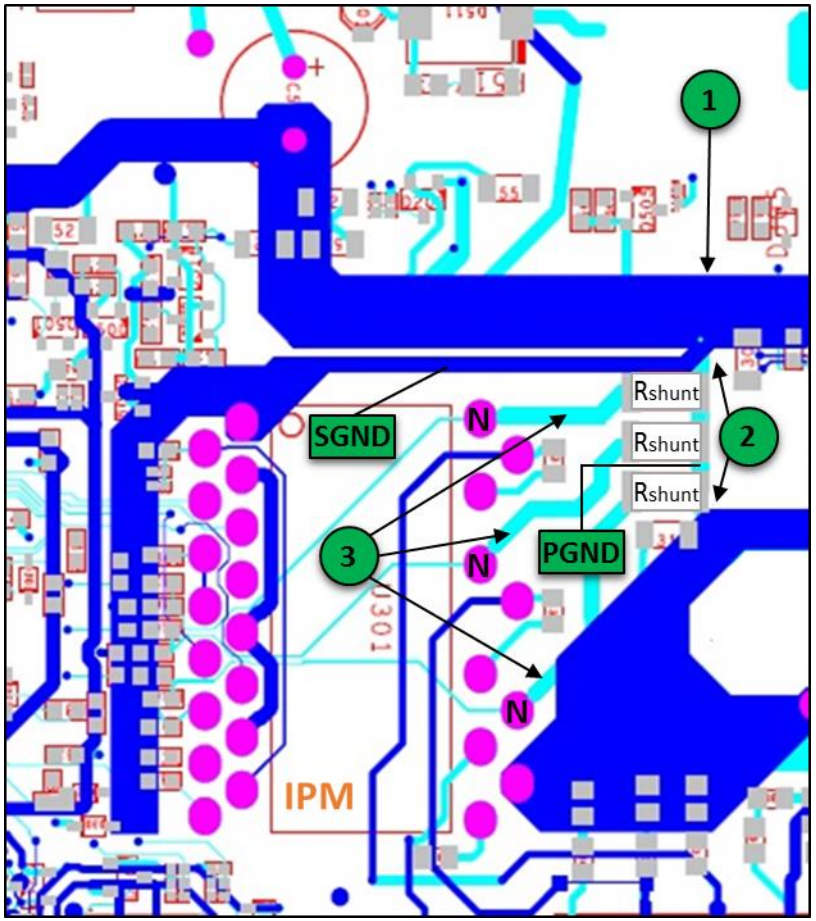
4. power ground tracks are too narrow; this may increase parasitic inductance

Expample 1, improving

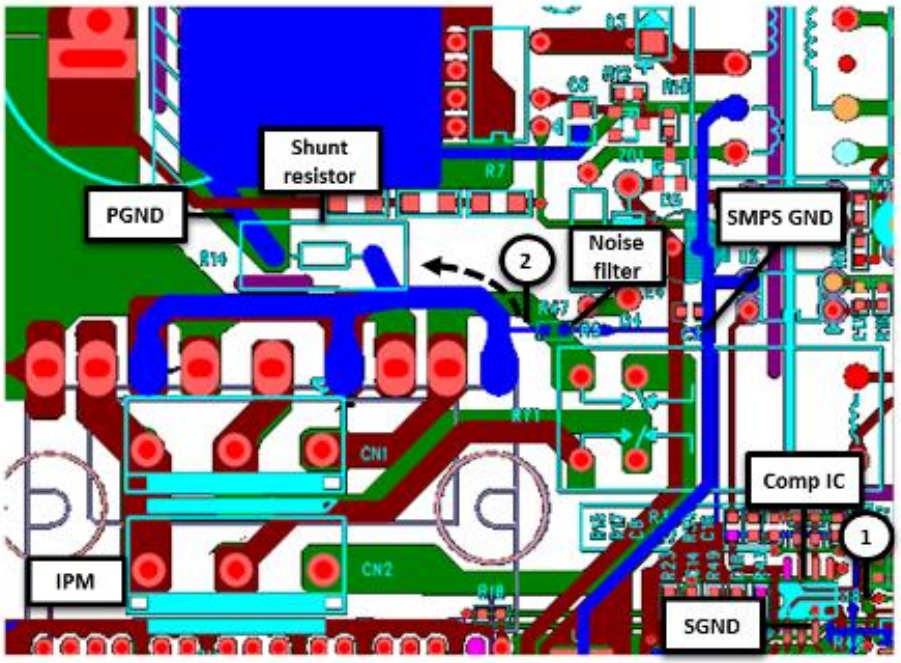
1. the ground path has been reshaped to remove any loops and increase the width/length ratio of the tracks

2. the shunt resistor ground has been changed to a star point configuration for both signal and power grounds

3. the shunt resistors have been relocated to guarantee shorter and symmetric connections with the N pins of the IPM



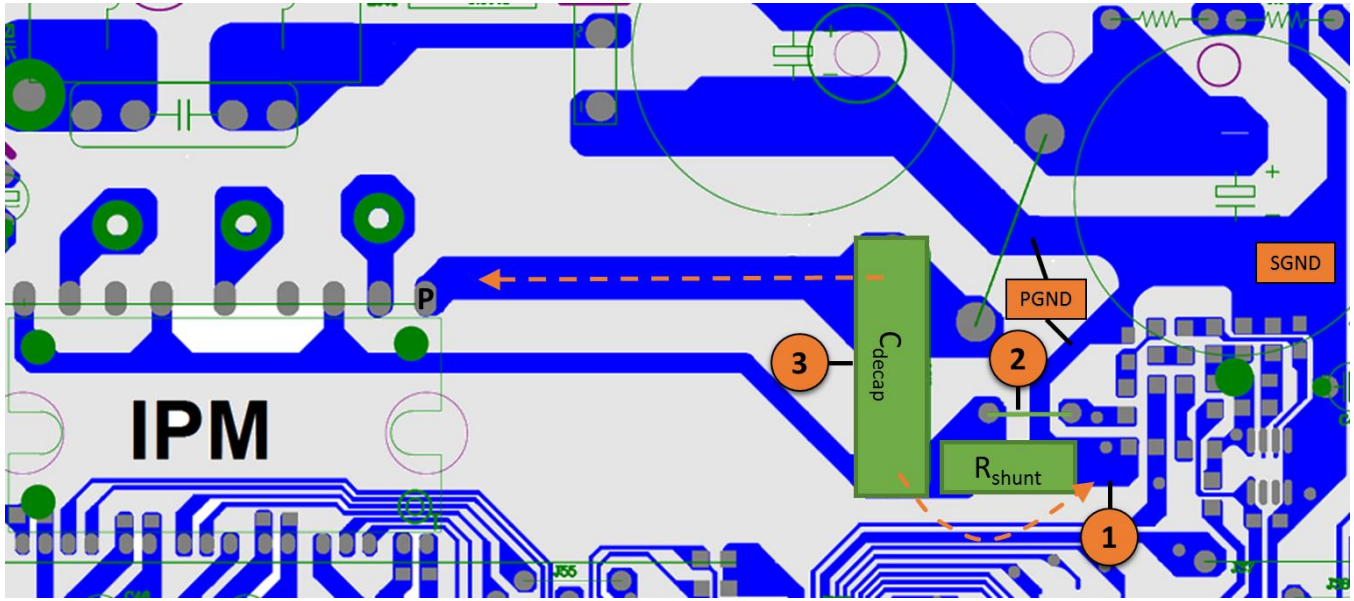
Expample 2



1. the comparator ground for OCP (SGND) is too far from shunt resistor R14 (PGND) and it crosses the SMPS power supply ground; finally, the comparator IC should be closer to the shunt resistor and away from noisy tracks

2. the current sensing track should be connected directly to shunt resistor R14 and the filtering capacitor must be placed as close as possible to the comparator pin to reduce the level of noise that could trigger false overcurrent protection

Expample 3



1. separate the signal ground tracks from the power ground tracks and connect them at a single point by using the shunt resistors in a star configuration; widen the power ground track

2. jumpers on current sensing tracks should be avoided; the RC filter ground must be connected to the IC comparator ground

3. the decoupling capacitor on the bus voltage should be connected between the P pin of the IPM (as close as possible) and the power ground (on the shunt resistor)