UM0791
User manual

Demonstration firmware for the DMX-512 communication protocol receiver based on the STM32F103Zx

Introduction

This document describes how to use the demonstration firmware for the DMX-512 communication protocol receiver. The USART (universal synchronous asynchronous receiver transmitter) module of the STM32F103Zx (ARM 32-bit Cortex™-M3) microcontroller unit receives the data from the DMX-512 controller via an RS-485 transceiver. This receiver is compatible with the latest DMX-512 protocol, and can also be used with any DMX-512 controller having a “NULL” start code.

This document provides:

- an overview of the complete solution.
- a description and flowcharts of the STM32 demonstration firmware.
- schematics and layouts.

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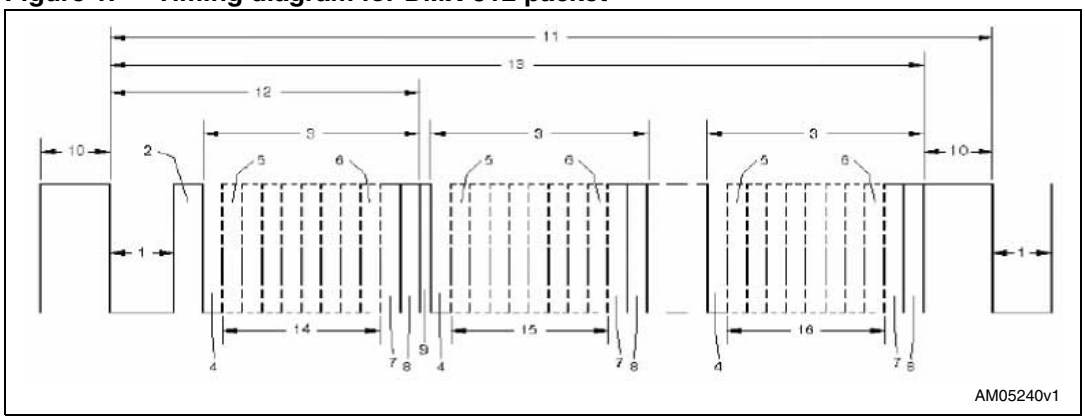
1 DMX-512 receiver format

1.1 Packet format

The DMX-512 slots are transmitted sequentially in an asynchronous serial format, beginning with slot 0 and ending with the last implemented slot, up to slot 512 (a maximum total of 513 slots). Before the first data slot is transmitted, a reset sequence is transmitted, consisting of a BREAK, a MARK AFTER BREAK and a START code. Valid DMX-512 data slot values under a NULL START code range from 0 to 255 decimal.

Figure 1. Timing diagram for DMX-512 packet



The following points refer to the numbers shown in *Figure 1*.

1. SPACE for BREAK
2. MARK AFTER BREAK
3. Slot time
4. START time
5. LEAST SIGNIFICANT data bit
6. MOST SIGNIFICANT data bit
7. STOP bit
8. STOP bit
9. MARK TIME BETWEEN SLOTS
10. MARK BEFORE BREAK
11. BREAK to BREAK time
12. RESET sequence
13. DMX-512 packet
14. START CODE (slot 0, data)
15. SLOT 1, data
16. SLOT n, data (max 512)

1.2 Timing values for DMX-512-A receiver

The receiver only accepts the data if all the timing values comply with those given in *Table 1*.

Table 1. Timing values of DMX-512 packet received

Description	Min	Typical	Max	Unit
Bit rate	245	250	255	Kbps
Bit time	3.92	4	4.08	µs
Minimum update time for 513 slots	-	22.7	-	ms
Maximum refresh rate for 513 slots	-	44	-	µs
"SPACE" for BRAEK	88	176	-	µs
"MARK" after BREAK (MAB)	8	-	<1.00	µs s
"MARK" time between slots	0	-	<1.00	s
"MARK" before BREAK (MBB)	0	-	<1.00	s
BREAK to BREAK time	1196	-	1.25	µs s
DMX-512 packet	1196	-	1.25	µs s

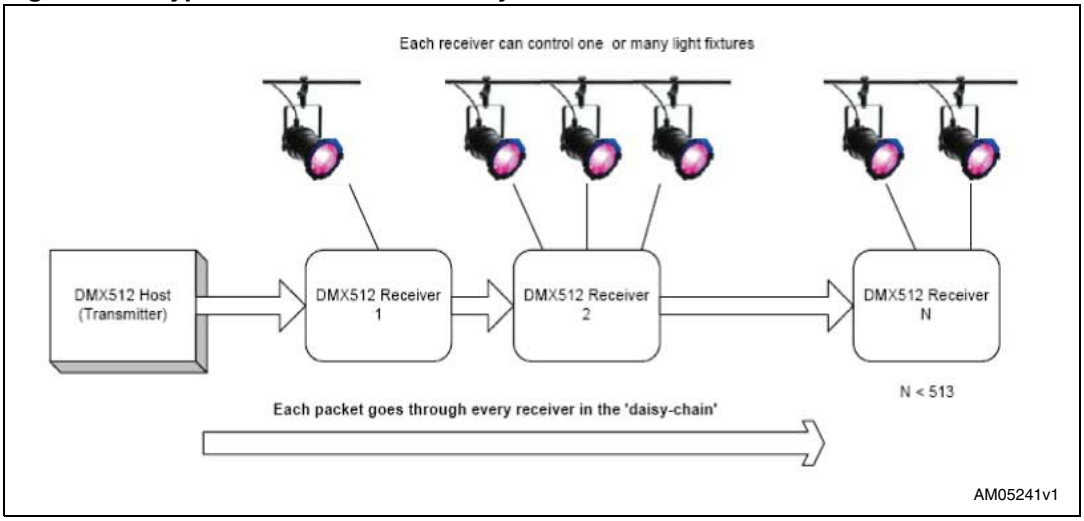
2 DMX-512 receiver

2.1 System overview

Figure 2 represents a typical DMX-512 system.

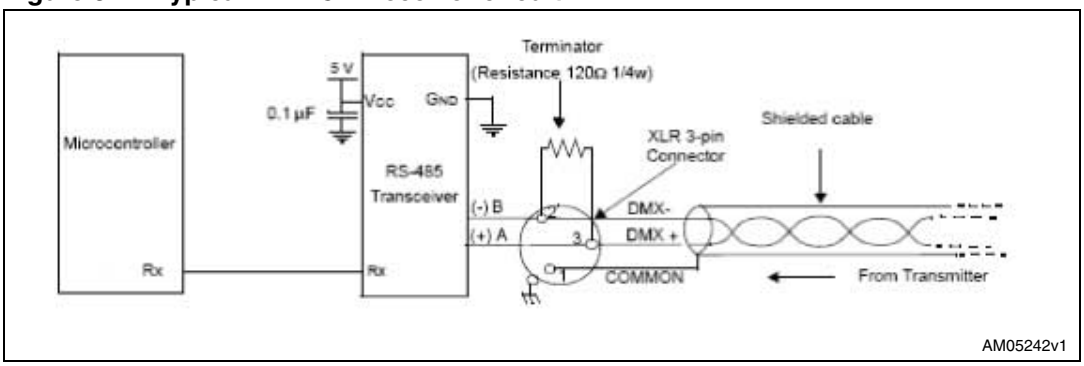
1. The multiple receivers are connected to the DMX host in a daisy-chain manner and every packet goes through every receiver in its entirety.
2. Each receiver receives the differential signal through an RS-485 transceiver and gives it to the controller on the receiving side.
3. Each receiver is programmed with a specific slot address so that it knows which slot it has to extract from each packet.

Figure 2. Typical DMX-512 receiver system



4. There should be only one terminating resistance with a set of receivers and that terminating resistance should be connected with the receiver farthest from the transmitter/controller.

Figure 3. Typical DMX-512 receiver circuit

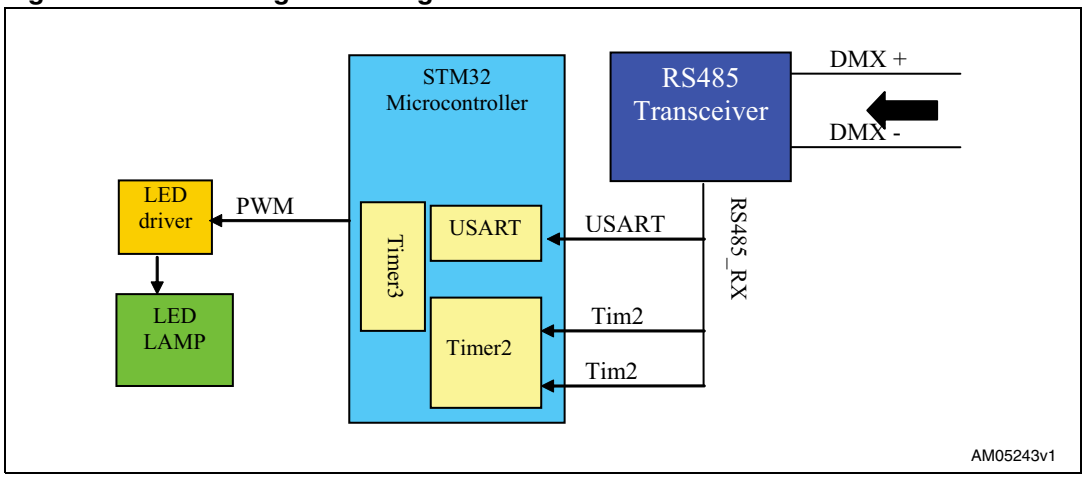


2.2 DMX-512 receiver block diagram

Figure 4 shows the block diagram of the single DMX-512 receiver. The signals are first received by the RS-485 transceiver. The STM32F103Zx microcontroller receives the packet through the USART_RX pin according to the address programmed.

The receiver then extracts a particular slot from the packet and modifies the duty cycle of the PWM output as per the data received.

Figure 4. Block diagram of single DMX-512 receiver

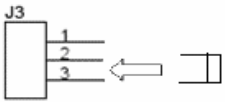


2.3 RS-485 transceiver

Figure 5 on page 9 depicts the front view of the RS-485 transceiver board.

The jumpers on the RS-485 transceiver board should be set as shown below to receive the DMX differential signal from the transmitter and transmit the signal to the microcontroller.

- Jumper J3 on pin 2 and pin 3



- Jumper J4 on pin 2 and pin 3

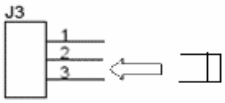


Figure 5. Front view of RS-485 transceiver board

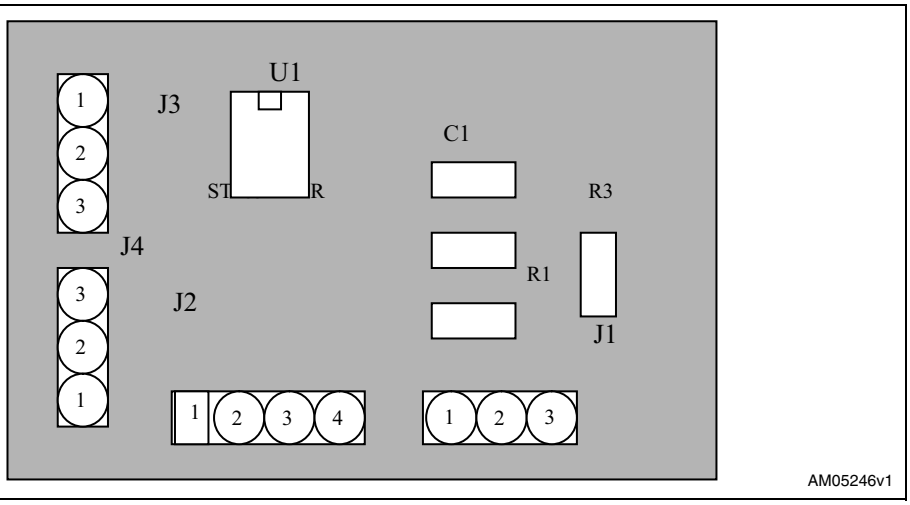
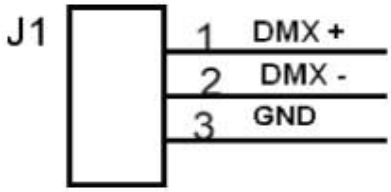


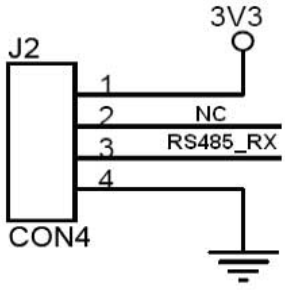
Figure 6 and *Figure 7* show the connections of J1 and J2 on the RS-485 transceiver board.

Figure 6. J1 pin diagram



DMX+ and DMX- are the differential signals from the DMX-512 transmitter. NC means *not connected*.

Figure 7. J2 pin diagram

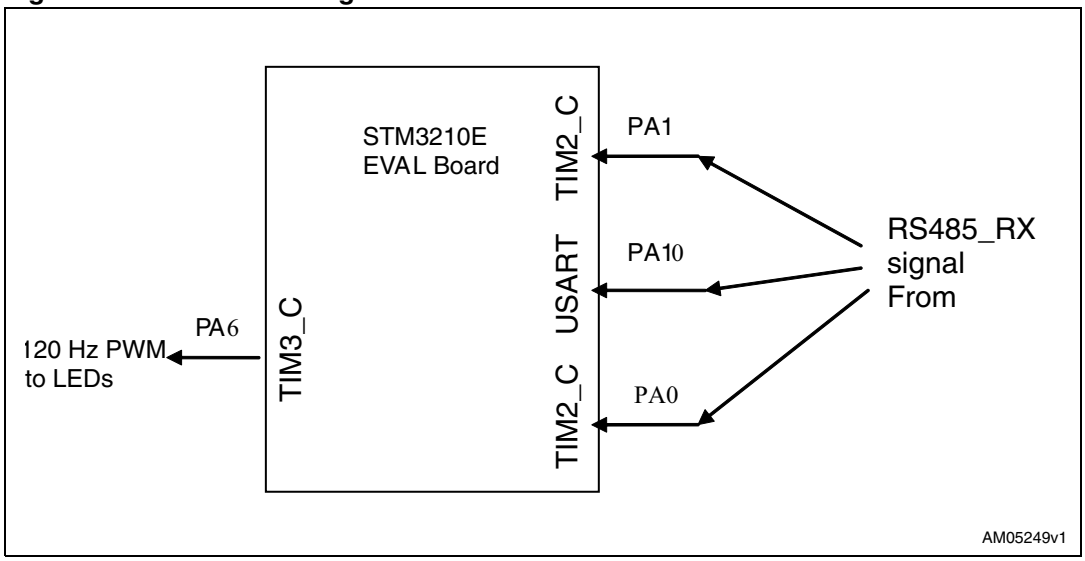


RS485_RX is the signal given to the STM32F103Zx. NC means *not connected*.

2.4 MCU block diagram

Figure 8 shows the connections to the STM3210E-EVAL board.

Figure 8. MCU block diagram



The RS485_RX signal is transmitted to three GPIO pins, PA0, PA1 and PA10. The PWM output is generated on pin PA6.

- PA0 is configured as channel1 of timer2. The falling edge input capture is configured on this channel.
- PA1 is configured as channel2 of timer2. The rising edge input capture is configured on this channel.
- PA10 is configured as the Rx pin of USART1.
- A PWM of 120 Hz is produced on channel1 of timer3. The duty cycle of the PWM varies according to the data received.

3 Demonstration firmware

This chapter describes the software developed for the DMX-512 receiver. The differential signals are first received by the RS-485 transceiver. After the retransmission of the signals from the RS-485 transceiver, the valid “RESET sequence” (“BREAK” and “MARK after BREAK”) and the DMX-512 packet time are detected to process the received data. A particular data slot is selected from the packet received according to the address programmed, and the duty cycle of the PWM is varied, such that “255” signifies a 100% duty cycle and “0” signifies a 0% duty cycle. The software is described as it appears in each of the files, starting with the DMX initialization file followed by the main file and then the interrupt file. The software is developed using IAR EWARM5.3. The project uses the STM32 firmware library version 3.0.0.

The demonstration firmware consists of four main parts.

- A *dmx_init.c* file for configuring all the peripherals used in this application.
- A main routine, including PWM control, based on the data received.
- A Timer2 interrupt routine.
- A USART1 interrupt routine.

3.1 *dmx_init.c* file description

The *dmx_init* file is used for configuring various peripherals used in the application. Each function is described hereafter.

3.1.1 Timer2_Initialise

This function configures channel 1 in rising edge polarity and channel 2 in falling edge polarity of TIMER2 in input capture mode.

3.1.2 USART1_Intialise

This function configures USART1 in receiver mode with a baud rate of 250 kbps.

3.1.3 Timer3_PWM

The TIM3 clock runs at 120 Hz. TIM3 is set-up to work in PWM1 mode.

3.1.4 PWM_Update

This function updates the duty cycle of the PWM according to the data received.

3.2 *main.c* file description

The *main.c* file contains all the data required to initialize the peripherals used for this application. After receiving a valid packet according to the DMX-512 2008 standard, a particular data slot is retrieved according to the address programmed, and the duty cycle of the PWM is updated, shown by a change in the intensity of the LEDs.

The following sections describe each of the functions defined in the *main.c* file.

3.2.1 RCC_Configuration

This function enables the high-speed external crystal, including the PLL. It also configures various system clocks.

3.2.2 NVIC_Configuration

This function sets up the interrupts used in the STM32F103Zx.

3.2.3 GPIO_Configuration

This function sets up various IO ports used for the application.

3.3 Timer2 interrupt routine

In the timer2 interrupt subroutine, the “RESET Sequence” and DMX-512 packet time are detected and checked to see whether they are within the limits of the DMX-512 2008 standard. If the “RESET Sequence” is not valid, the timer2 interrupt routine waits for a valid “RESET Sequence”. If the DMX-512 packet time is *above* the limits, the entire packet is discarded.

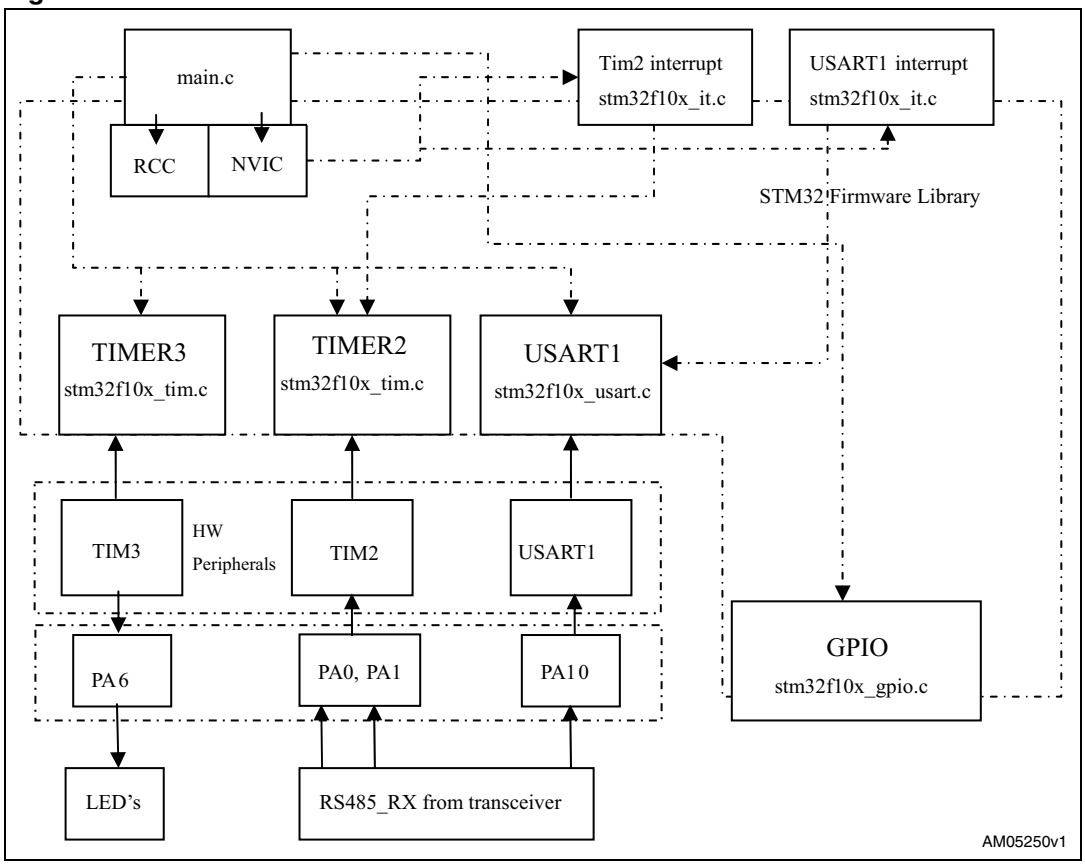
3.4 USART1 interrupt routine

This routine handles frame errors and data storage. Initially, when a frame error is detected it is treated like the “RESET Sequence”. Once the “RESET Sequence” has been validated (confirmed in the timer2 interrupt routine), this routine starts receiving data slots and stores them in a buffer when the USART receive interrupt is enabled. If a frame error occurs in between data slots, no additional data is stored.

4 Firmware architecture overview

Figure 9 illustrates the architecture of the demonstration firmware.

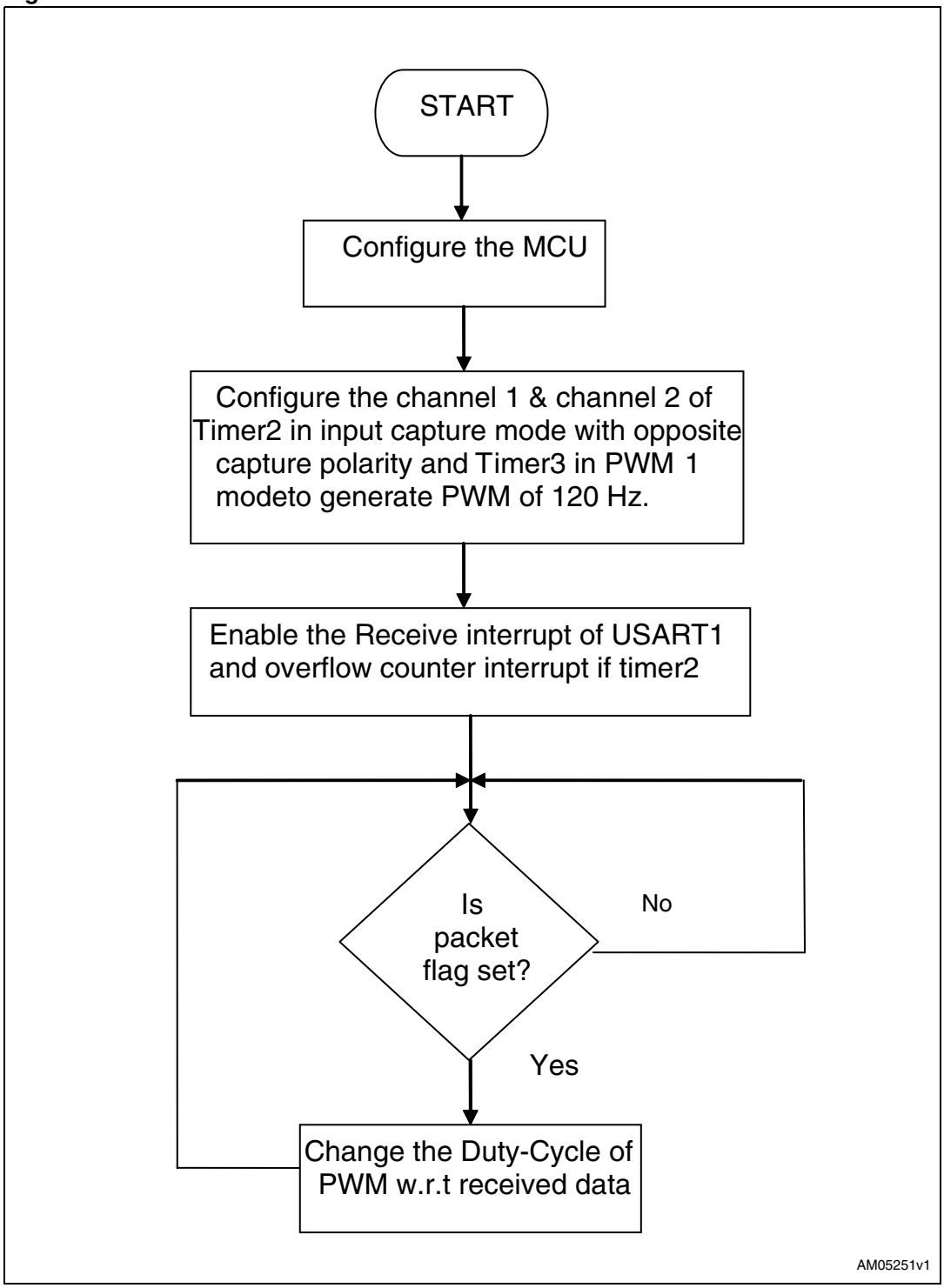
Figure 9. Demonstration firmware architecture overview



5 Firmware flowcharts

5.1 Main routine

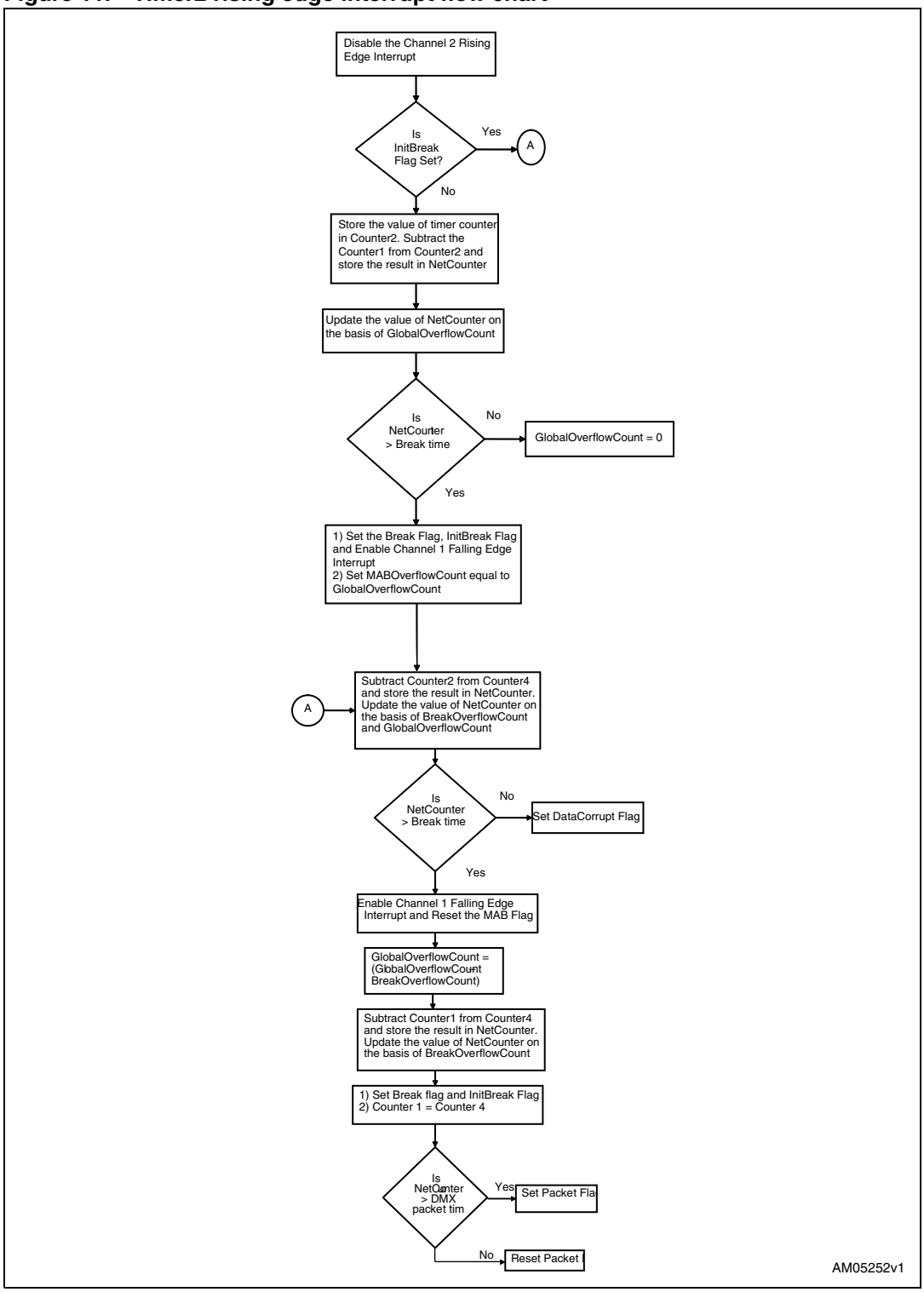
Figure 10. Main routine flow chart



5.2 Timer2 interrupt routine

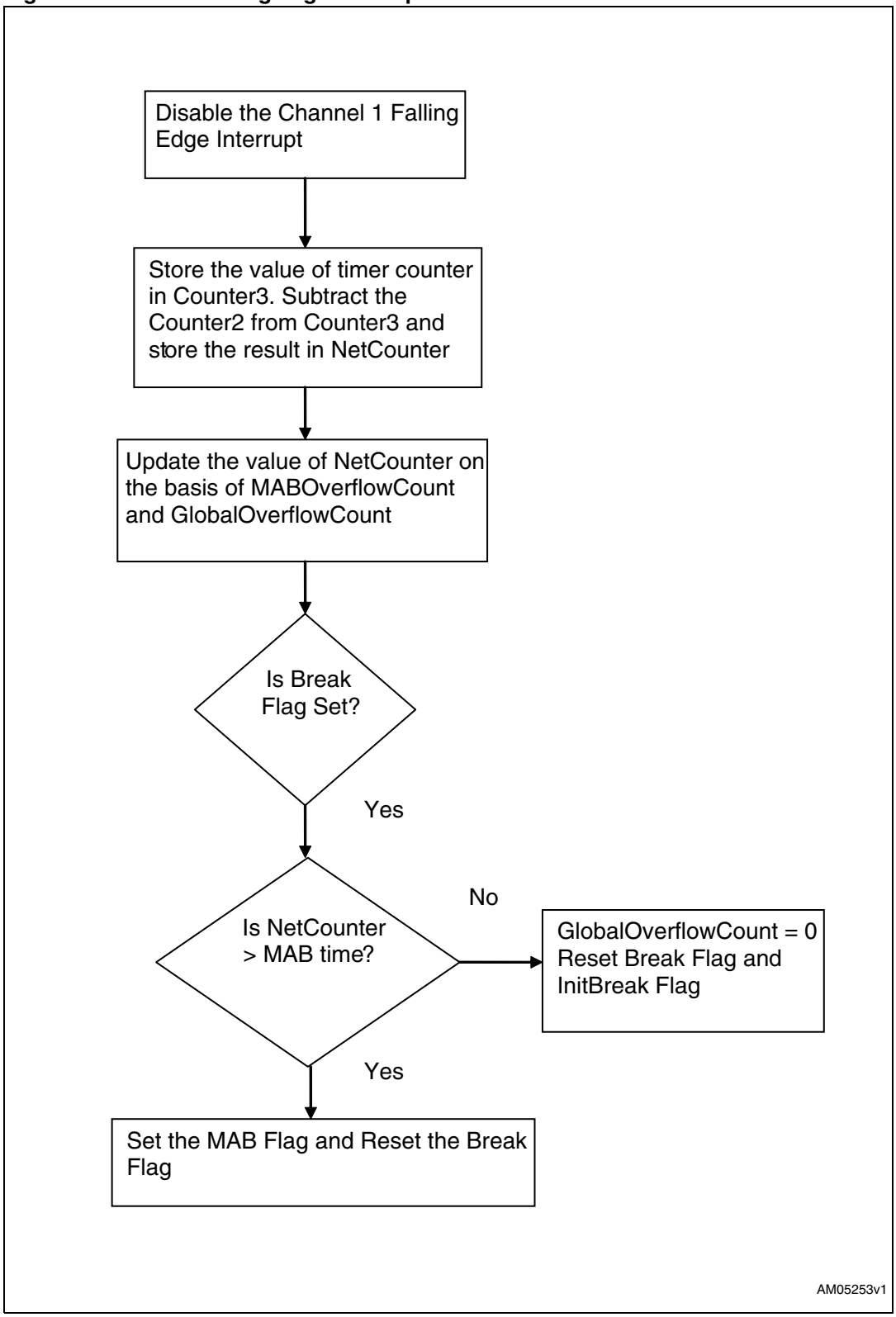
5.2.1 Channel 2 rising edge interrupt routine

Figure 11. Timer2 rising edge interrupt flow chart



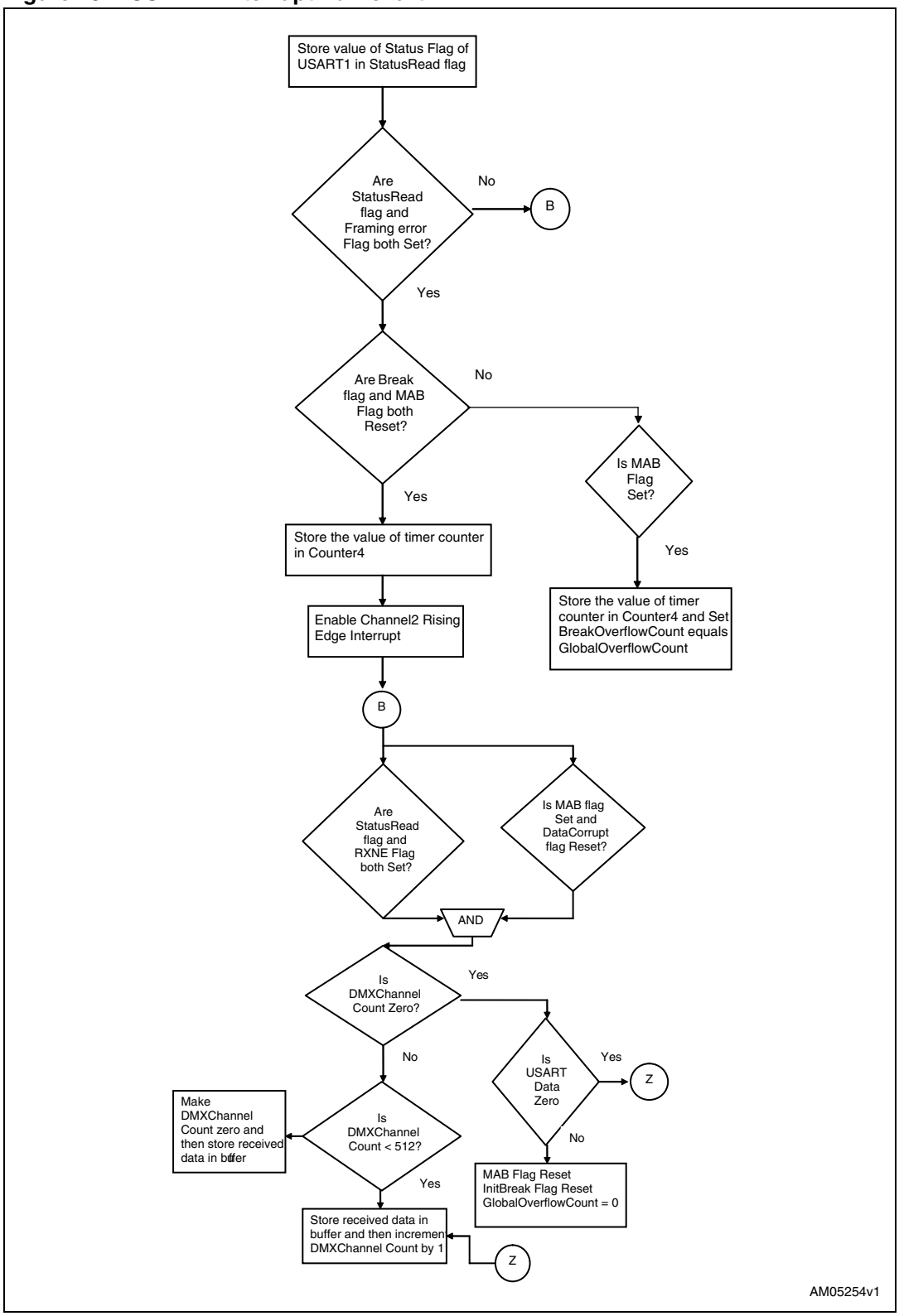
5.2.2 Channel 1 falling edge interrupt routine

Figure 12. Timer2 falling edge interrupt flow chart



5.3 USART1 interrupt routine

Figure 13. USART1 interrupt flow chart



6 Key features/specifications

The developed solution:

- receives data according to the DMX-512 2008 standard.
- is used with any DMX-512 transmitter irrespective of the number of bytes transmitted by the transmitter.

7 Schematic and layout

Figure 14. Schematic of RS-485 transceiver board

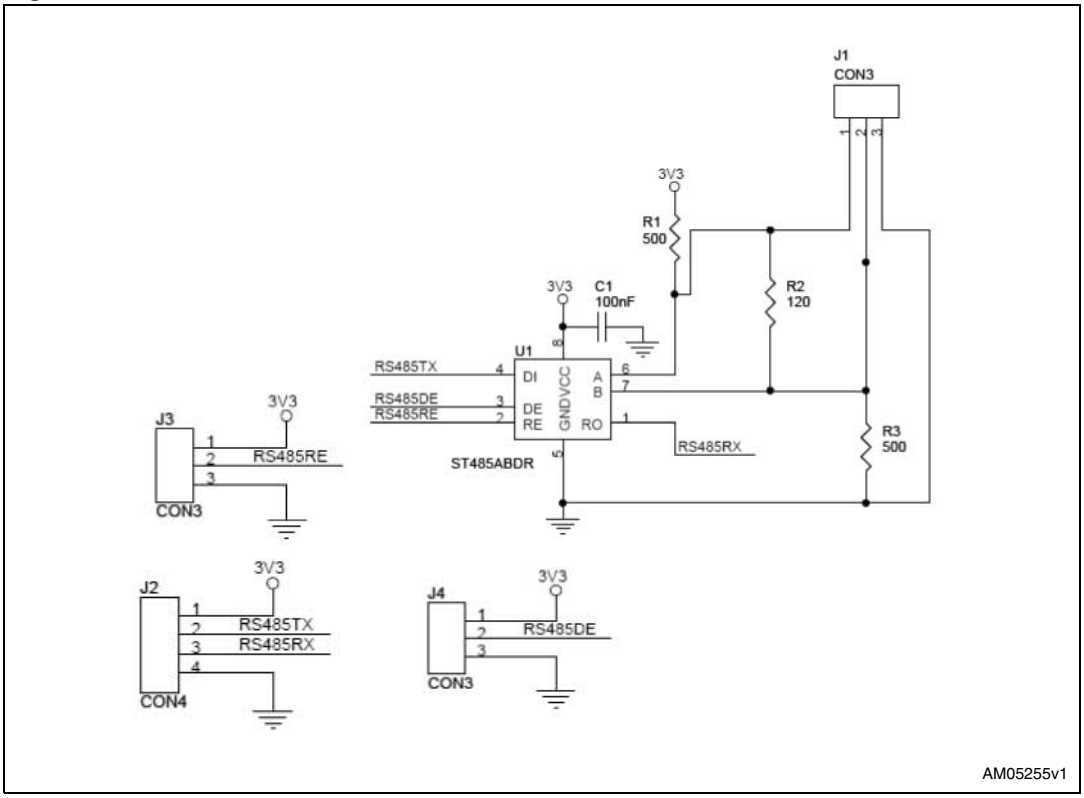
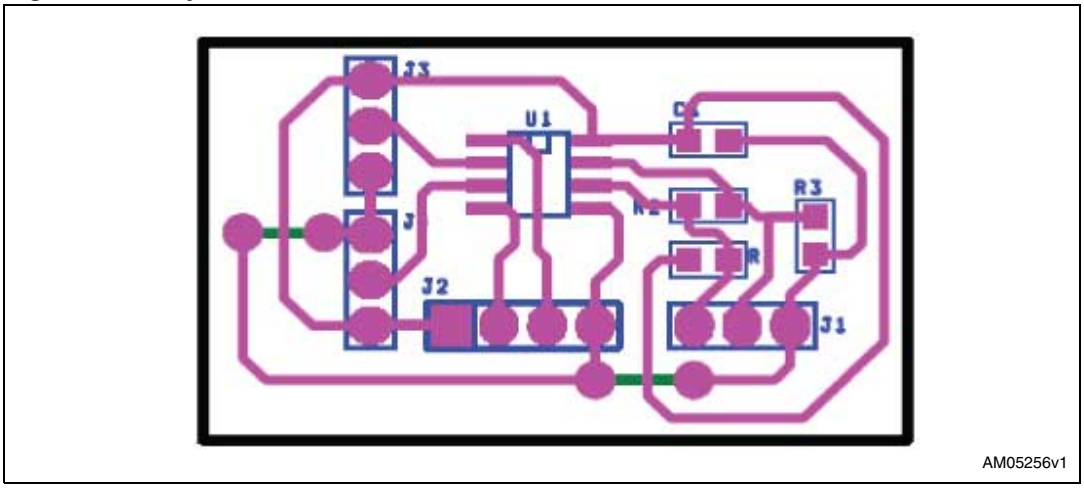


Figure 15. Layout of RS-485 transceiver board



8 Revision history

Table 2. Document revision history

Date	Revision	Changes
02-Feb-2010	1	Initial release.
17-Mar-2010	2	Changed document title from “DMX-512 communications protocol algorithm for receiver, based on the STM3210E-EVAL” to “Demonstration firmware for the DMX-512 communication protocol receiver based on the STM32F103Zx”. Replaced some references to the STM32 device with STM32F103Zx throughout the document. Corrected board part number in *Section 2.4: MCU block diagram* and *Figure 8 on page 10*. Minor text changes throughout the document.

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