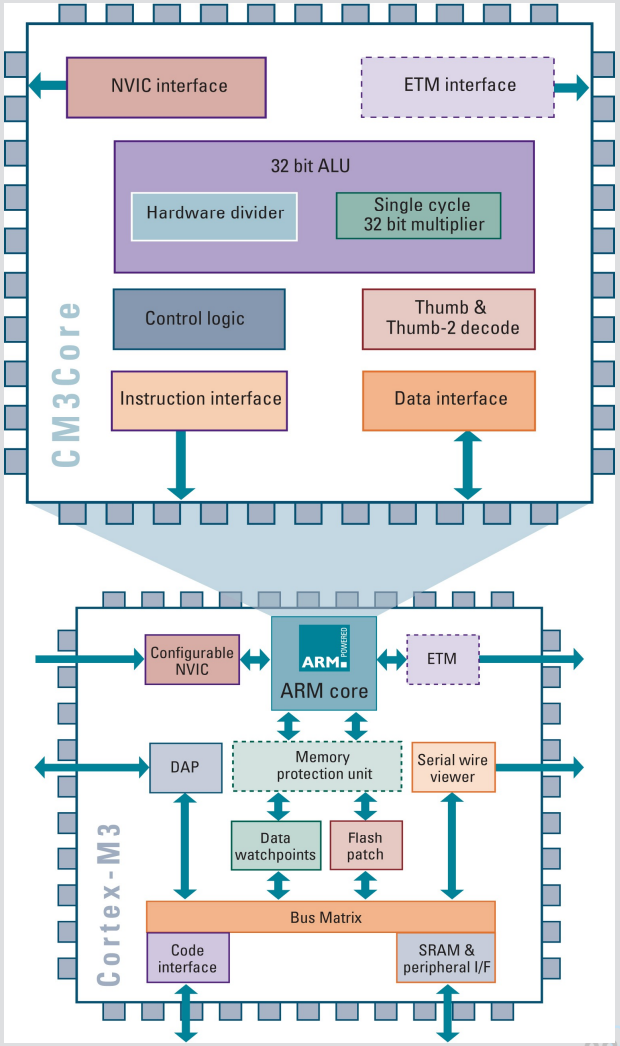
STM32x tec.pres.

STM32 ARM® Cortex™-M3 Based Product Introduction

STM32x Cortex M3

- **Hierarchical processor integrating core and advanced system peripherals**
- **Cortex-M3 core**
  - **Harvard architecture**
  - **3-stage pipeline w. branch speculation**
  - **Thumb®-2 and traditional Thumb**
  - **ALU w. H/W divide and single cycle multiply**
- **Cortex-M3 *Processor***
  - **Cortex-M3 core**
  - **Configurable interrupt controller**
  - **Bus matrix**
  - **Advanced debug components**



STM32x Cortex M3

- **ARM v7M Architecture**
- **Thumb-2 Instruction Set Architecture**
  - Mix of 16 and 32 bit instructions for very high code density
- **Harvard architecture**
  - Separate I & D buses allow parallel instruction fetching & data storage
- **Integrated Nested Vectored Interrupt Controller (NVIC) for low latency interrupt processing**
- **Vector Table is addresses, not instructions**
- **Designed to be fully programmed in C**
  - **Even reset, interrupts and exceptions**
- **Integrated Bus Matrix**
  - **Bus Arbiter**
  - **Bit Banding – Atomic Bit Manipulation (single instruction Read/Write)**
  - **Write Buffer**
  - **Memory Interface (I&D) Plus System Interface & Private Peripheral Bus**
- **Integrated System Timer (SysTick) for Real Time OS or other scheduled tasks**
- **Outstanding efficiency of 1.2 DMIPS/MHz**

STM32x Cortex M3

- 3-Stage Pipeline
  - Fetch, Decode & Execute
- Single Cycle Multiply

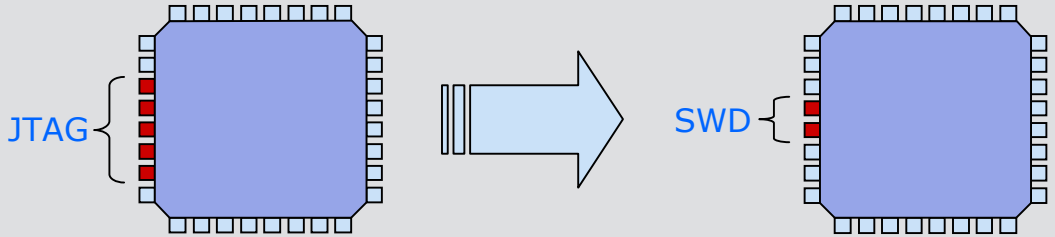
Source	Destination	Cycles
16b x 16b	32b	1
32b x 16b	32b	1
32b x 32b	32b	1
32b x 32b	64b	3-7*

*UMULL, SMULL,UMLAL, and SMLAL are interruptible and can also complete early depending on source values

- Hardware Division
  - UDIV & SDIV (Unsigned or Signed divide)
  - Instruction takes between 2 & 12 cycles depending on dividend and devisor
  - Closer the dividend and division the faster the instruction completes
  - Instruction is interruptible (abandoned/restarted)

STM32x Cortex M3

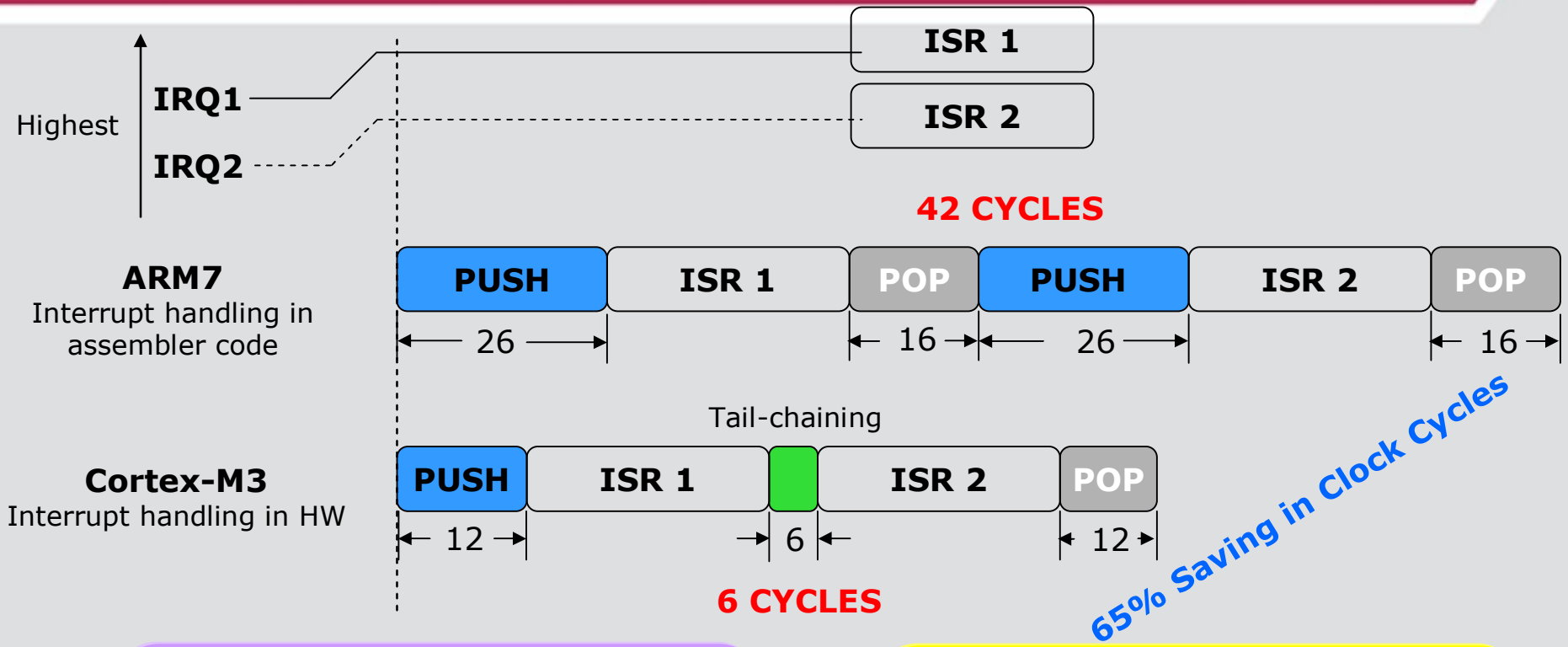
- Serial Wire Debugging **for optimized device pin-out**



More pins available for the application

- Embedded break/watch capabilities **for** easy flashed application debugging
  - ♦ **8 hardware breakpoints**
  - ♦ **2 hardware watchpoints** (test access to variable, memory in R&W)
- Serial Wire Viewer **for targeted low bandwidth** data trace
  - ♦ **Using serial wire interface or dedicated bus CKout+D[3..0] for better bandwidth**
  - ♦ **Triggered by embedded break and watch points**
- ETM capability for better real time debugging
  - ♦ **Instruction trace only**
  - ♦ **External signal triggering capability**
  - ♦ **Can be used in parallel with data watchpoint**

STM32x Cortex M3 - Interrupt



ARM7

- 26 cycles from IRQ1 to ISR1 entered
  - Up to 42 cycles if LSM
- 42 cycles from ISR1 exit to ISR2 entry
- 16 cycles to return from ISR2

Cortex-M3

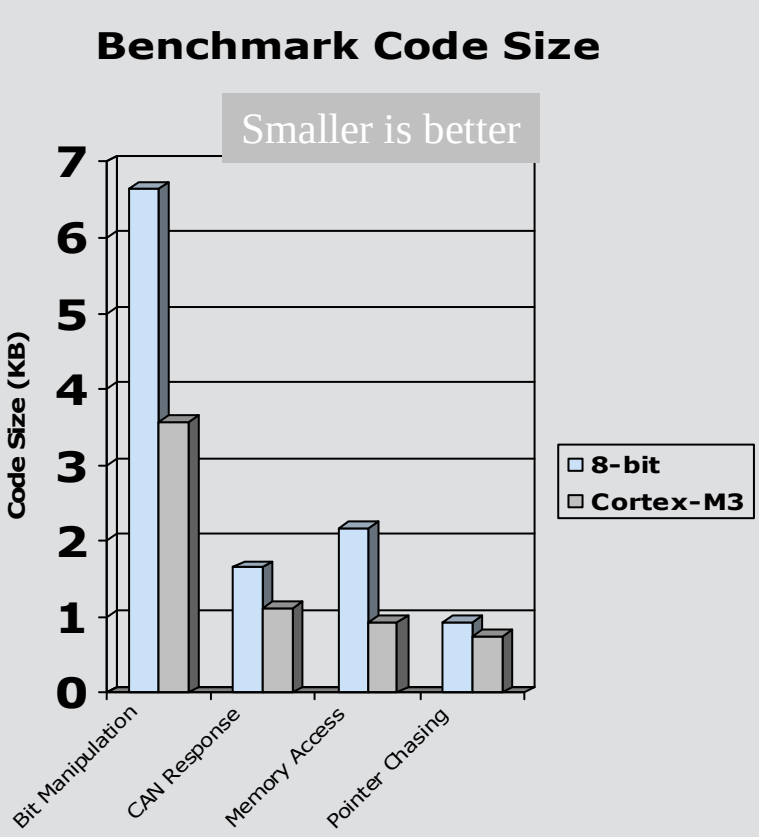
- 12 cycles from IRQ1 to ISR1 entered
  - 12 cycles if LSM
- 6 cycles from ISR1 exit to ISR2 entry
- 12 cycles to return from ISR2

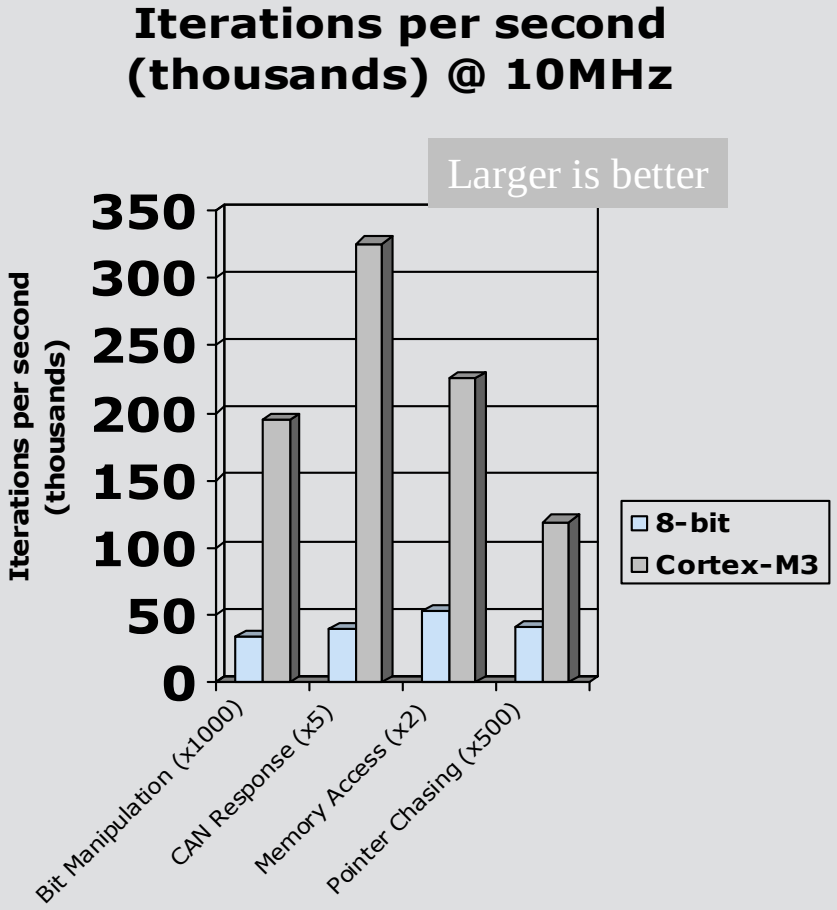
STM32x Cortex M3 – Power Management

- **Like to 8bit Microcontroller Cortex use power mode management**
  - **SLEEP NOW**
    - ♦ **"Wait for Interrupt"** instructions to enter low power mode
      - → No more dedicated control register settings sequence
    - ♦ **"Wait for Event"** instructions to enter low power mode
      - → No need of Interrupt to wake-up from sleep
      - → Rapid resume from sleep
  - **SLEEP on EXIT**
    - ♦ Sleep request done in interrupt routine
    - ♦ Low power mode entered on interrupt return
      - → **Very fast wakeup time** without context saving (6 cycles)
  - **DEEP SLEEP**
    - ♦ **Long duration sleep**
      - → From product side: PLL can be stopped or shuts down the power to digital parts of the system
      - → Enables low power consumption
- **Optimized RUN mode CORE power consumption 3 time less than ARM7^{TDMI}**

STM32x Cortex M3

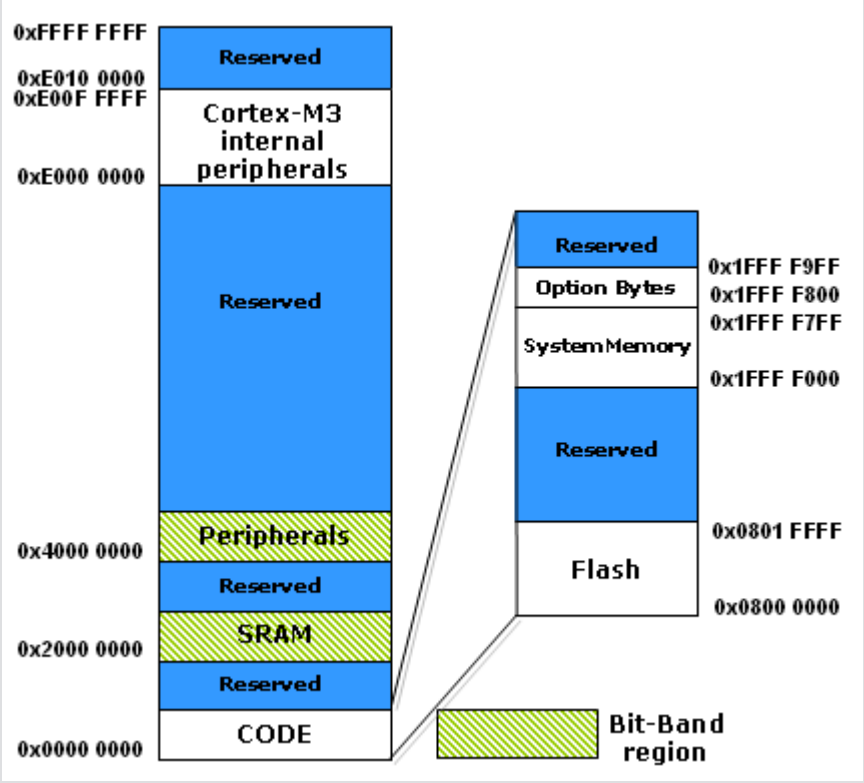
CODE SIZE AND TIME EXECUTION COMPARISON BETWEEN 8-BIT PRODUCT AND CORTEX-M3





STM32x Cortex M3 - MEMORY

Boot Loader Auto Detect Speed and is available for:
USART1: STM32F101/2/3
USART1/2 – CAN- USB: STM32F105/7
DFU is an application available for all STM32 and must be enclosed inside appll.



Boot modes

Depending on the Boot configuration, Embedded Flash Memory, System Memory or Embedded SRAM Memory is aliased at @0x00

BOOT Mode Selection Pins		Boot Mode	Aliasing
BOOT1	BOOT0		
x	0	User Flash	User Flash is selected as boot space
0	1	SystemMemory	SystemMemory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

SystemMemory: contains the Bootloader used to re-program the FLASH through USART.

Boot from SRAM :

In the application initialization code you have to Relocate the Vector Table in SRAM using the NVIC *Exception Table and Offset* register

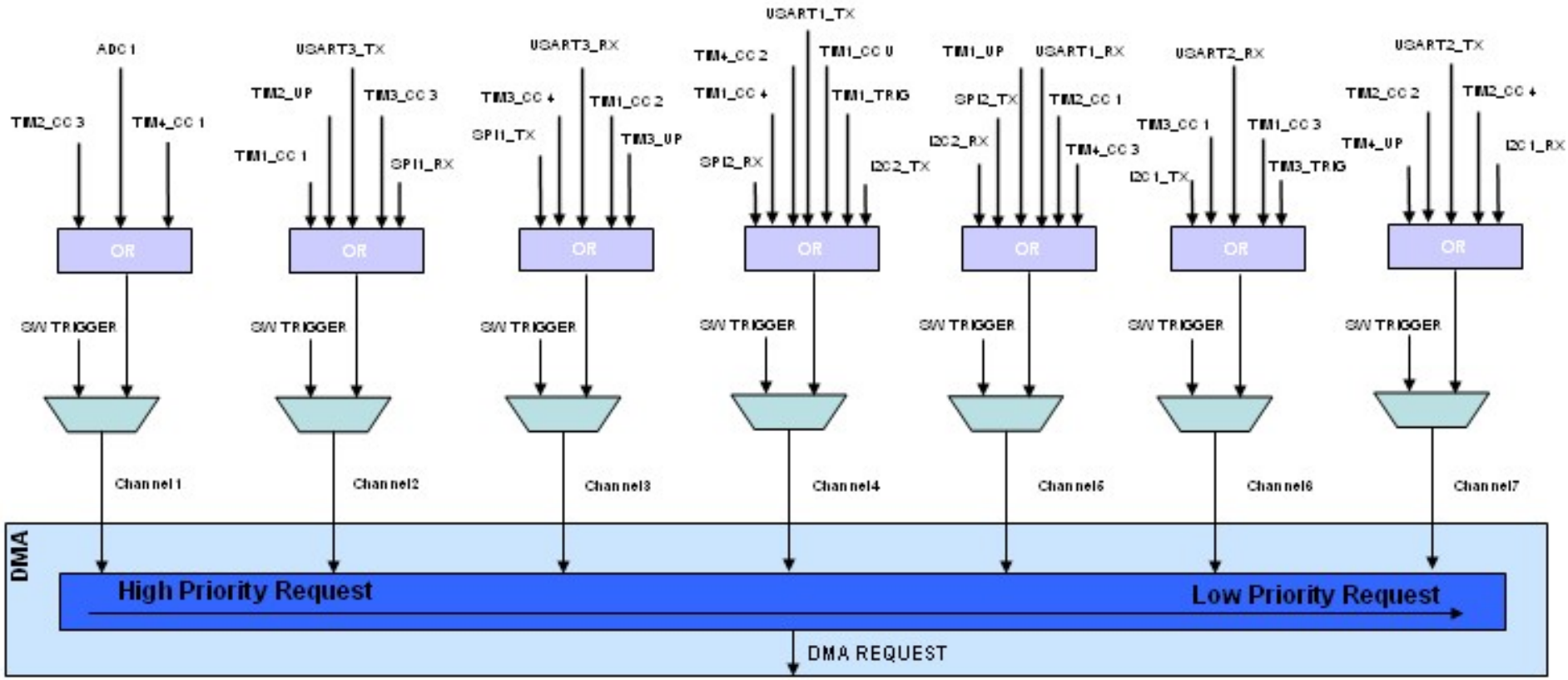
- ***Addressable memory space of 4 GBytes***

STM32x Cortex M3 - DMA

- 7 independently configurable channels: hardware requests or software trigger on each channel
- Software programmable priorities: Very high, High, Medium or Low. (Hardware priority in case of equality)
- Programmable and Independent source and destination transfer data size: Byte, Halfword or Word
- 3 event flags for each channel: DMA Half Transfer, DMA Transfer complete and DMA Transfer Error
- Memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers
- Faulty channel is automatically hardware disabled in case of bus access error
- Programmable number of data to be transferred: up to 65536
- Support for circular buffer management

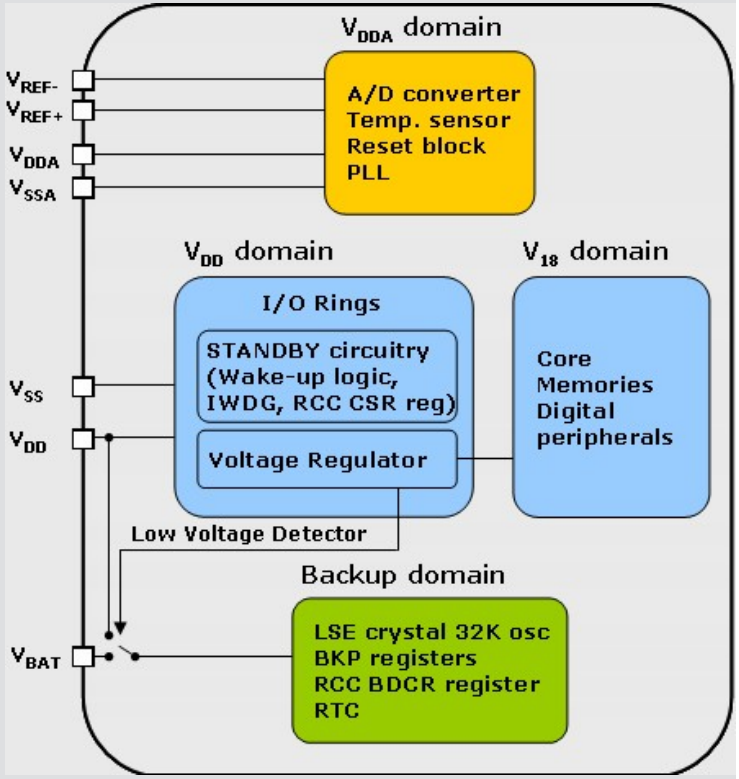
STM32x Cortex M3 – DMA/cont.

The DMA controller provides access to 7 channels



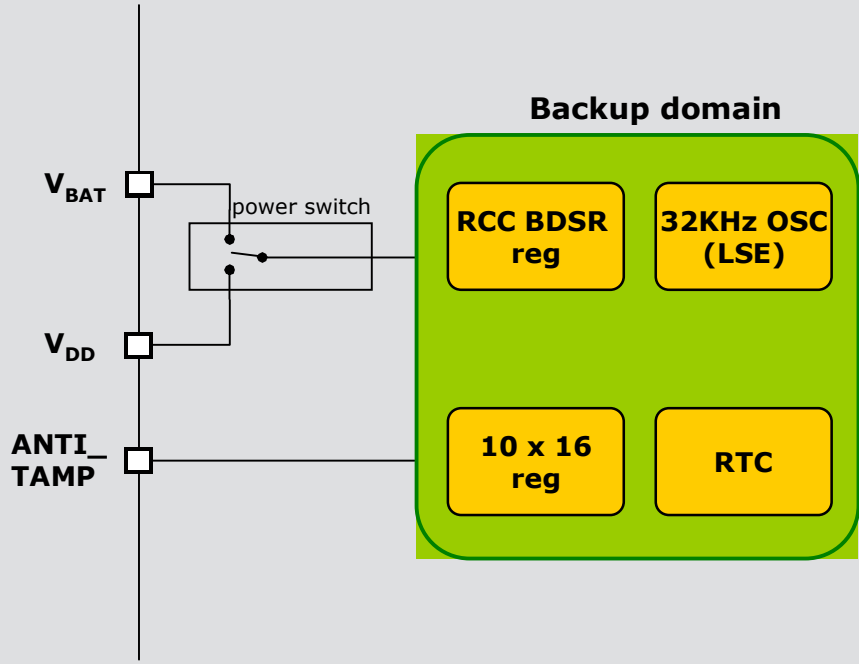
STM32x Cortex M3 - Power Supply

- Power Supply Schemes
  - **V_{DD}** = 2.0 to 3.6 V: External Power Supply for I/Os and the internal regulator.
  - **V_{DDA}** = 2.0 to 3.6 V: External Analog Power supplies for ADC, Reset blocks, RCs and PLL.
    ➔ ADC working only if $V_{DDA} \geq 2.4$ V
  - **V_{BAT}** = 2.0 to 3.6 V: For Backup domain when **V_{DD}** is not present.
  - Power pins connection:
    - V_{DD} and V_{DDA} must be connected to the same power source
    - V_{SS}, V_{SSA} and V_{REF-} must be tight to ground
    - $0V < V_{REF+} \leq V_{DDA}$
    - V_{REF+} and V_{REF-} available only in LQFP100 package, in other packages they are internally connected respectively to V_{DDA} and V_{SSA}



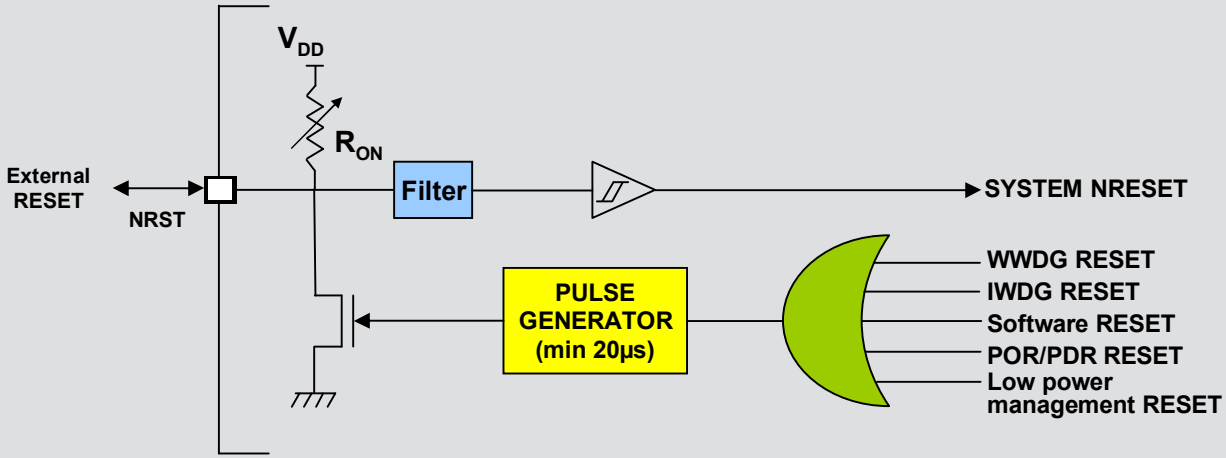
STM32x Cortex M3 - Backup Domain

- **Backup Domain contains**
  - RTC (Counter, Prescaler and Alarm mechanism)
  - Separate 32KHz Osc (LSE) for RTC
  - Up to 64 x 16-bits user backup registers
  - RCC BDSR register: RTC source clock selection and enable + LSE config
  - ➔ Reset only by Backup domain RESET
- **V_{BAT} independent voltage supply**
  - Automatic switch-over to V_{BAT} when V_{DD} goes lower than PDR level
  - No current sunk on V_{BAT} when V_{DD} present
- **Tamper detection: resets all user backup registers**
  - Configurable level: low/high
  - Configurable interrupt generation



STM32x Cortex M3 - RESET Sources

- System RESET
  - Resets all registers except some RCC registers and BKP domain
  - Sources
    - Low level on the NRST pin (External Reset)
    - WWDG end of count condition
    - IWDG end of count condition
    - A software reset (through NVIC)
    - Low power management Reset



- Power RESET
  - Resets all registers except BKP domain
  - Sources
    - Power On/Power down Reset (POR/PDR)
    - When exiting STANDBY mode

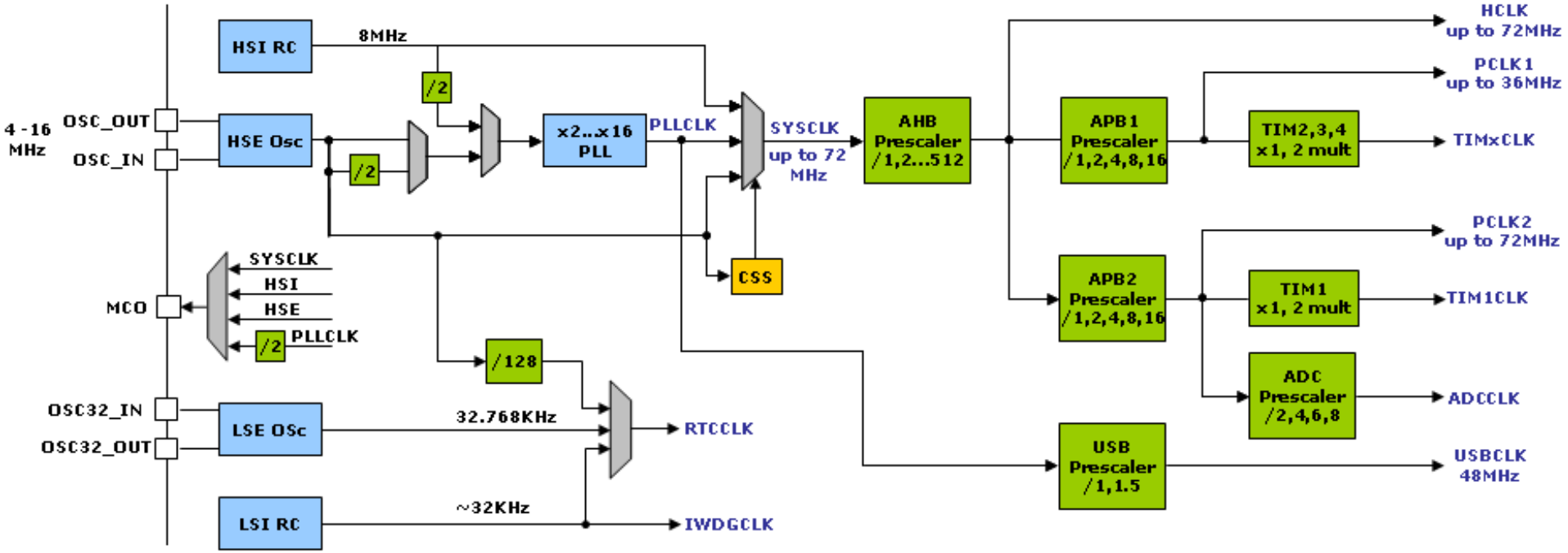
- Backup domain RESET
  - Resets all BKP domain
  - Sources
    - Setting BDRST bit in RCC BDCR register
    - VDD or VBAT power on, if both supplies have previously been powered off.

STM32x Cortex M3 - On Chip Oscillators

- **Multiple clock sources for full flexibility in RUN/Low Power modes**
  - **HSE** (High Speed External oscillator): 4MHz to 16MHz main osc which can be multiplied by the PLL to provide a wide range of frequencies
  - **HSI** (High Speed Internal RC): factory trimmed internal RC oscillator 8MHz +/- 1% over 0-70°C temp range
    - Feeds System clock after reset or exit from STOP mode for fast startup (startup time : 2us max)
    - Backup clock in case HSE osc is failing
  - **LSI** (Low Speed Internal RC): 32KHz internal RC for IWDG and optionally for the RTC used for Auto Wake-Up (AWU) from STOP/STANDBY mode
  - **LSE** (Low Speed External oscillator): 32.768kHz osc provides a precise time base with very low power consumption (max 1µA). Optionally drives the RTC for Auto Wake-Up (AWU) from STOP/STANDBY mode.
  - **CSS** Clock Security System

STM32x Cortex M3 - Clock Scheme

- System Clock (SYSCLK) sources
  - ✓ HSI
  - ✓ HSE
  - ✓ PLL
- RTC Clock (RTCCLK) sources
  - ✓ LSE
  - ✓ LSI
  - ✓ HSE clock divided by 128
- USB Clock (USBCLK) provided from the internal PLL
- Clock-out capability on the MCO pin (PA.08) / max 50MHz
- Configurable dividers provides AHB, APB1/2, ADC and TIM clocks
- Clock Security System (CSS) to backup clock in case of HSE clock failure (HSI feeds the system clock)
  - Enabled by SW w/ interrupt capability linked to Cortex NMI

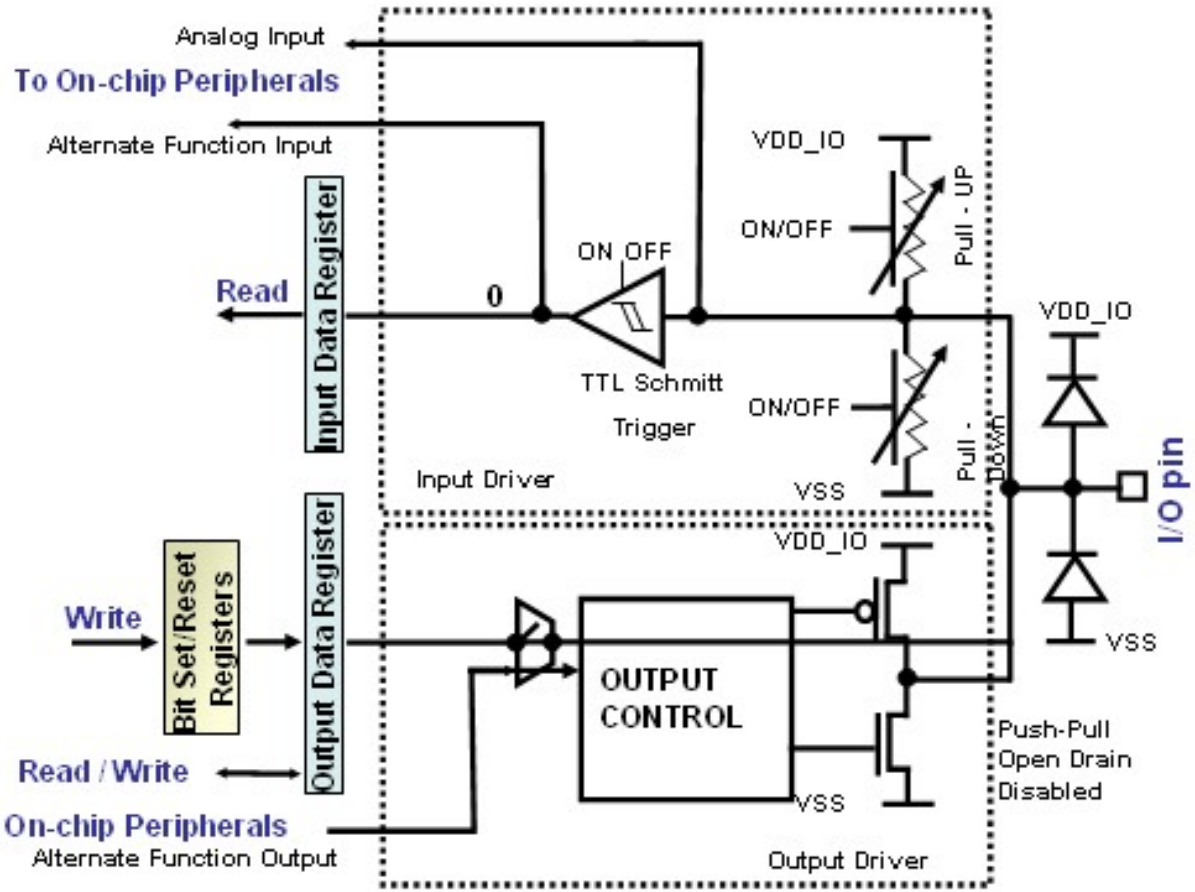


STM32x Cortex M3 - GPIO Features

- 80 multifunction bi-directional I/O ports available: 80% IO ratio
  - 80 Standard I/Os (5V tolerant, 20 mA drive)
  - 18 MHz Toggling
  - Configurable Output Speed up to 50 MHz
  - Up to 16 Analog Inputs
  - Alternate Functions pins (like USARTx, TIMx, I2Cx, SPIx, CAN, USB…)
  - All I/Os can be set-up as external interrupt (up to 16 lines at time)
  - One I/O can be used as Wake-Up from STANDBY (PA.00)
  - One I/O can be set-up as Tamper Pin (PC.13)
  - All Standard I/Os are shared in 5 ports (GPIOA..GPIOE)
  - Atomic Bit Set and Bit Reset using BSRR and BRR registers
  - Locking mechanism to avoid spurious write in the IO registers
    - When the LOCK sequence has been applied on a port bit, it is no longer possible to modify the configuration of the port bit until the next reset (no write access to the CRL and CRH registers corresponding bit).

STM32x Cortex M3 - GPIO Configuration Modes

Configuration Mode	CNF1	CNF0	MOD1	MOD0
Analog Input	0	0	00	
Input Floating **(Reset State)**	0	1		
Input Pull-Up	1	0		
Input Pull-Down	1	0		
Output Push-Pull	0	0	00: For inputs 01: 10 MHz 10: 2 MHz 11: 50 MHz	
Output Open-Drain	0	1		
AF Push-Pull	1	0		
AF Open-Drain	1	1		



STM32x Cortex M3 - ADC Features

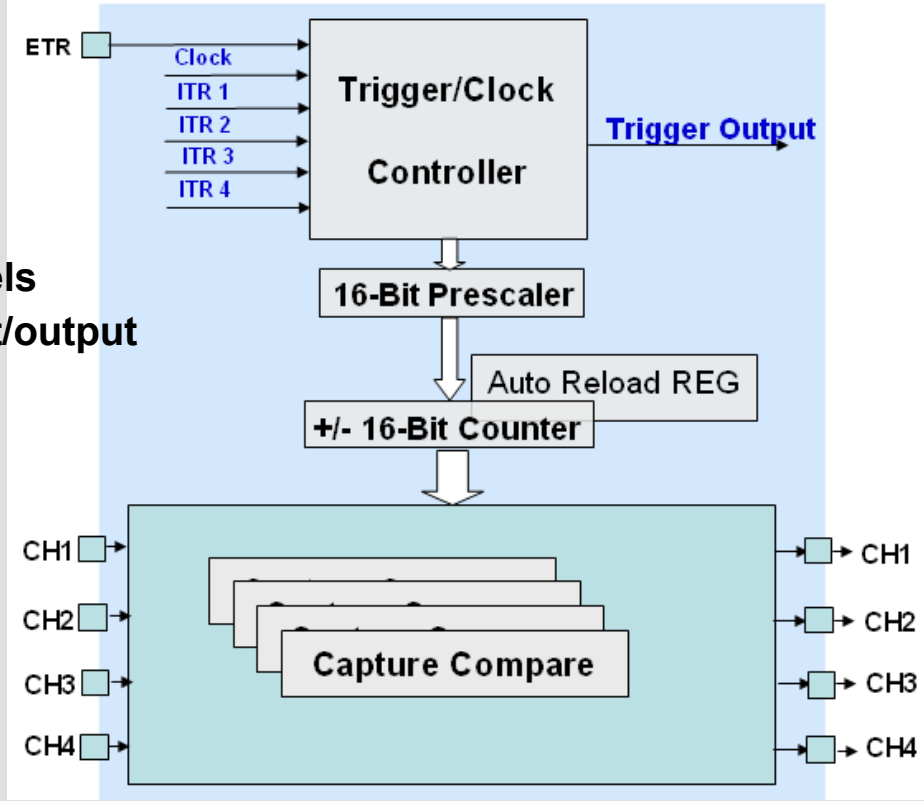
- ADC conversion rate 1 Msample (up to 2Ms) and 12-bit resolution
- ADC supply requirement: 2.4V to 3.6 V
- ADC input range: VREF- ≤ VIN ≤ VREF+
  (VREF+ and VREF- available only in 100/144 package)
- 8 conversion mode
- Up to 21 multiplexed channels:
  - 19 external channels
  - 2 internal channels: connected to Temperature sensor and internal reference voltage (Bandgap voltage)
- Channels conversion groups:
  - Up to 16 channels regular group
  - Up to 4 channels injected group
- Single and continuous conversion modes

STM32x Cortex M3 - ADC Features

- Scan mode for automatic conversion of channel 0 to channel ‘n’
- External trigger option for both regular and injected conversion
- Channel by channel programmable sampling time and conversion order
- Discontinuous mode on regular and injected groups
- Self-calibration
- Left or right Data alignment with inbuilt data coherency
- Analog Watchdog on high and low thresholds
- Interrupt generation on:
  - End of Conversion
  - End of Injected conversion
  - Analog watchdog
- DMA capability (only on ADC1)

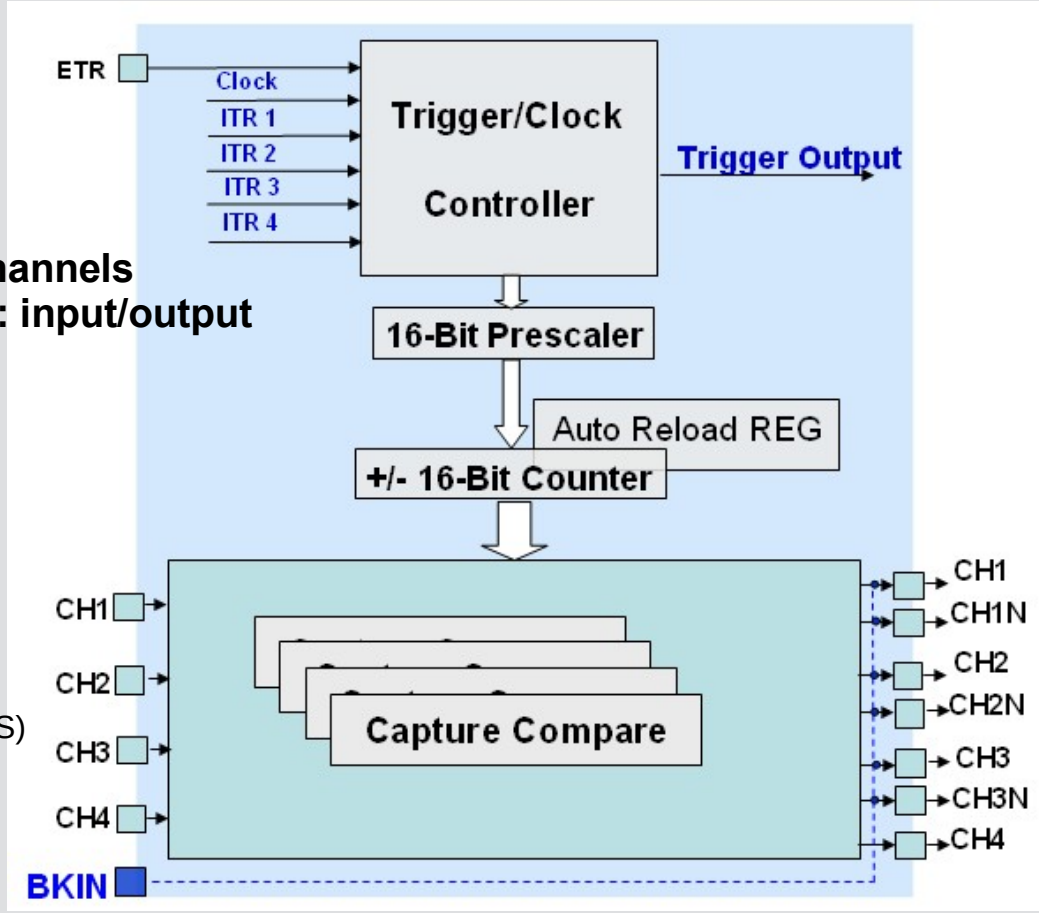
STM32x Cortex M3 - General Purpose timer

- TIM2, 3, 4 on Low Speed APB (APB1)
- Internal clock up to 36 MHz
- 16-bit Counter
  - Up, down and centered counting modes
  - Auto Reload
- 4 x 16 High resolution Capture Compare Channels
  - Programmable direction of the channel: input/output
  - Output Compare
  - PWM
  - Input Capture, PWM Input Capture
  - One Pulse Mode
- Synchronization
  - Timer Master/Slave
  - Synchronisation with external trigger
  - Triggered or gated mode
- Encoder interface
- 6 Independent IRQ/DMA Requests generation
  - At each Update Event
  - At each Capture Compare Events
  - At each Input Trigger



STM32x Cortex M3 - Advanced Control Timer (TIM1)

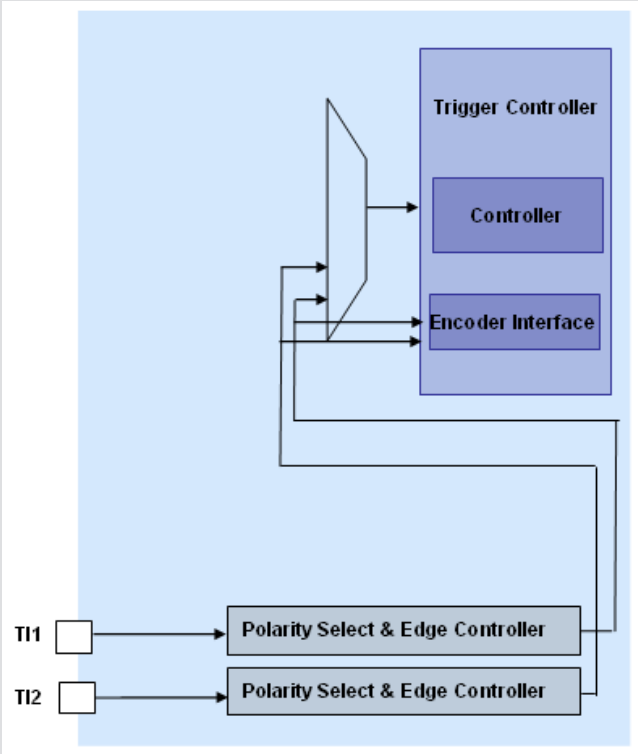
- Internal clock up to 72MHz
- 16-bit Counter
  - Auto Reload
  - Up, down and centered counting
  - modes
- 4x 16 High resolution Capture Compare channels
  - Programmable direction of the channel: input/output
  - Output Compare: Toggle, PWM
  - Input Capture
  - PWM Input Capture
- Synchronization
- Up to 8 IT/DMA Requests
- Motor Control Specific Feature
- OC Signal Management
  - 6 Complementary outputs
  - Dead-time management (0…14uS res.13,8nS)
  - Repetition Unit
- Encoder Interface
- Hall sensor Interface
- Embedded Safety features
  - Break sources: BKIN pin/ CSS, HW operate without clock
    CSS



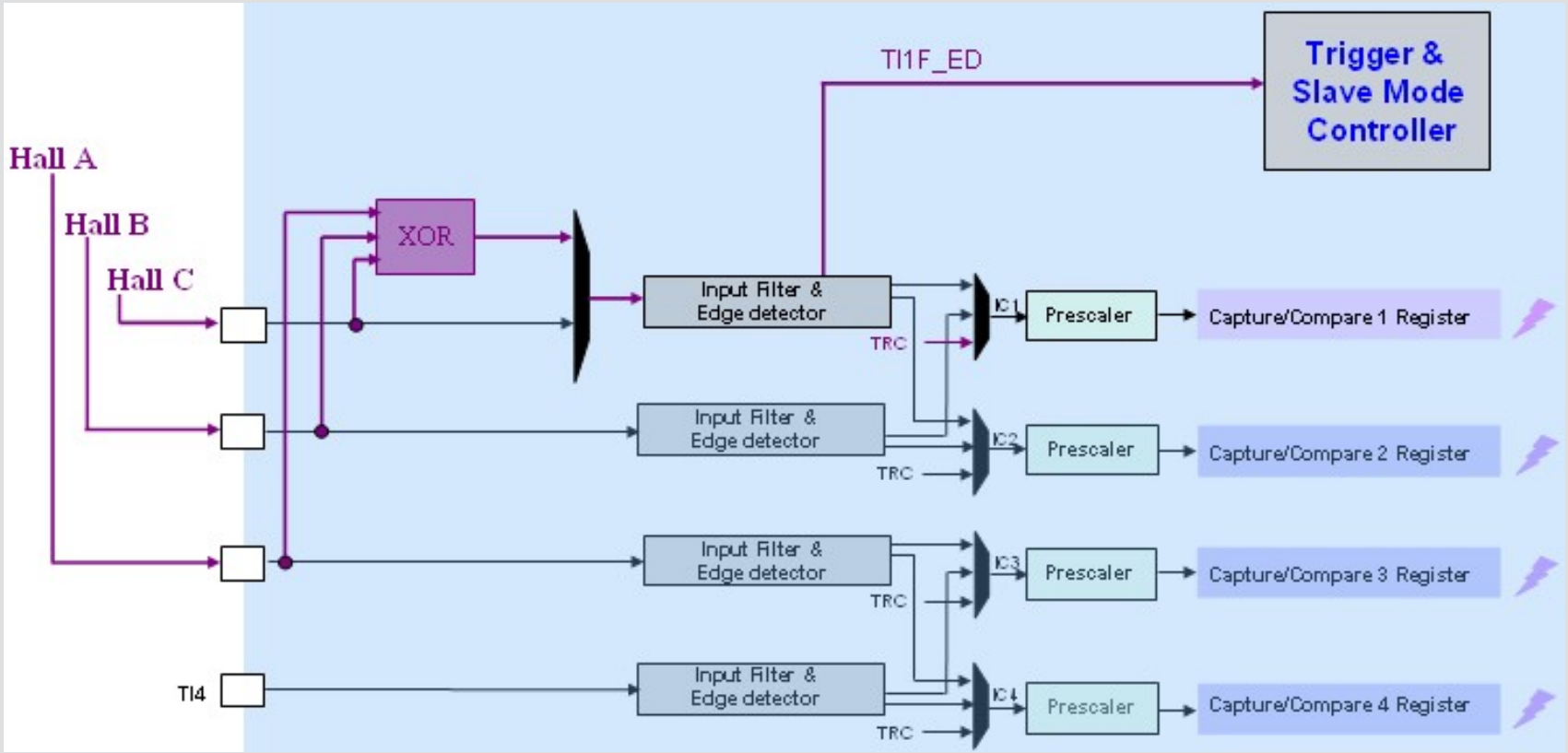
STM32x Cortex M3 - Encoder Interface

- Encoders are used to measure position and speed of motion systems (either linear or angular)
- The encoder interface mode acts as an external clock with direction selection
- The counter provides information on the current position (for instance angular position of an electric motor's rotor)
- To obtain dynamic information (speed, acceleration) on must measure the number of counts between two periodic events, generated by another timer
- Encoders and Microcontroller connection example:
  - An external incremental encoder can be connected directly to the MCU without external interface logic.

    The third encoder output which indicates the mechanical zero position, may be connected to an external interrupt and trigger a counter reset.

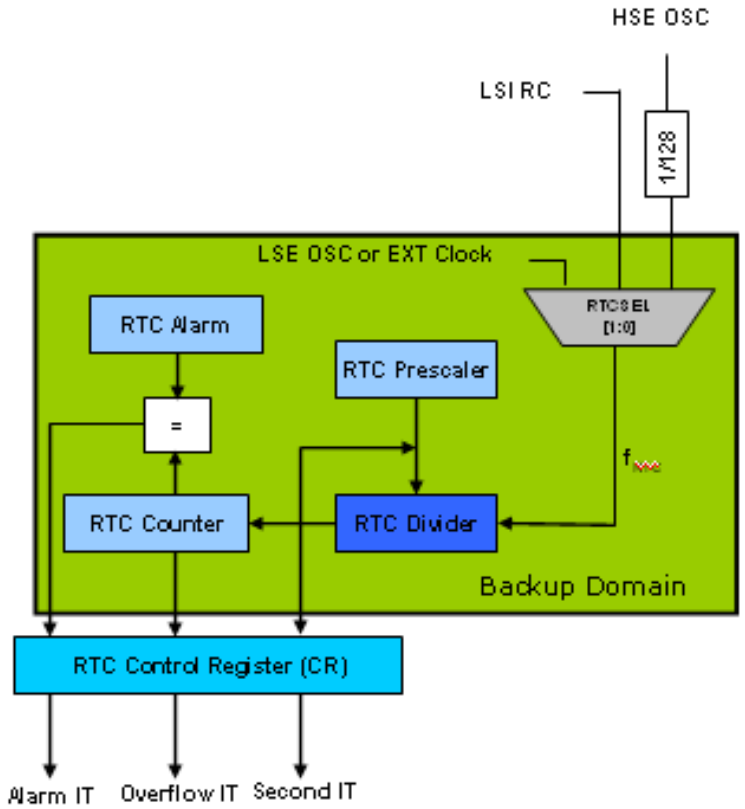


STM32x Cortex M3 - Hall sensor Interface



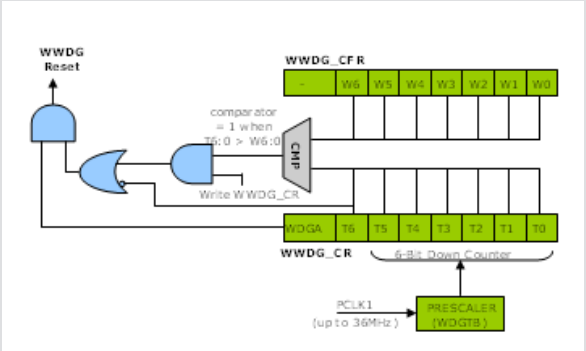
STM32x Cortex M3 - RTC Features

- Clock sources
  - 32.768 kHz dedicated oscillator (LSE)
  - Low frequency (32kHz), low power internal RC(LSI)
  - HSE divided by 128
- 3 Event/Interrupt sources
  - Second
  - Overflow
  - Alarm (also connected to EXTI Line 17 for Auto Wake-Up from STOP)
- Register protection against unwanted write operations
- RTC core & clock configuration in Backup domain
  - Independent V_{BAT} voltage supply
  - Reset only by Backup domain reset
  - RTC config kept after reset or wake-up from STANDBY
- Calibration Capability
  - RTC clock can be output on Tamper pin for calibration
  - Then the clock can be adjusted from 0 to to 121ppm by a step of 1ppm



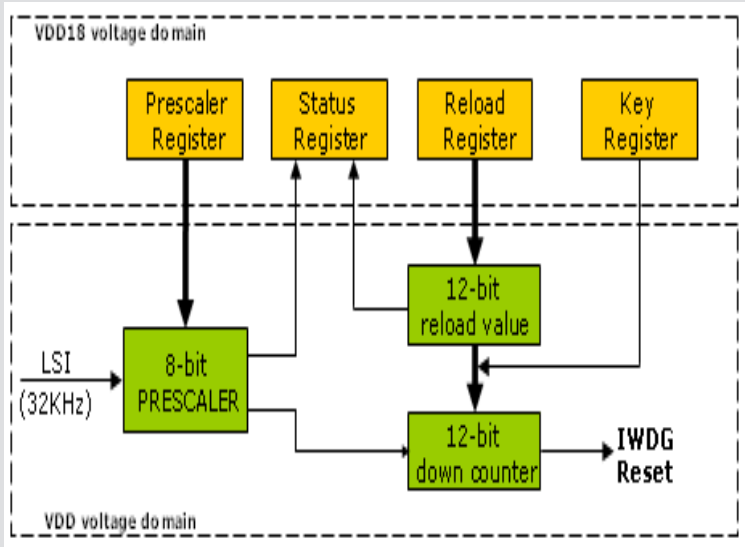
STM32x Cortex M3 - WWDG features

- Configurable time-window, can be programmed to detect abnormally late or early application behavior
- Conditional reset
  - Reset (if watchdog activated) when the down counter value becomes less than 40h (T6=0)
  - Reset (if watchdog activated) if the down counter is reloaded outside the time-window
- To prevent WWDG reset: write T[6:0] bits (with T6 equal to 1) at regular intervals while the counter value is lower than the time-window value (W[6:0])
- Early Wakeup Interrupt (EWI): occurs whenever the counter reaches 40h ➔ can be used to reload the down counter
- WWDG reset flag (in RCC_CSR) to inform when a WWDG reset occurs
- Min-max timeout value @36MHz (PCLK1): 113µs / 58.25ms



STM32x Cortex M3 - IWDG (independent WDG)

- Selectable HW/SW start through option byte
- Advanced security features:
  - IWDG clocked by its own dedicated low-speed clock (LSI) and thus stays active even if the main clock fails
  - Once enabled the IWDG can't be disabled (LSI can't be disabled too)
  - Safe Reload Sequence (key)
  - IWDG function implemented in the VDD voltage domain that is still functional in STOP and STANDBY mode (IWDG reset can wake-up from STANDBY)
- To prevent IWDG reset: write IWDG_KR with AAAAh key value at regular intervals before the counter reaches 0
- IWDG reset flag (in RCC_CSR) to inform when a IWDG reset occurs
- Min-max timeout value @32KHz (LSI): 125µs / 32.8s

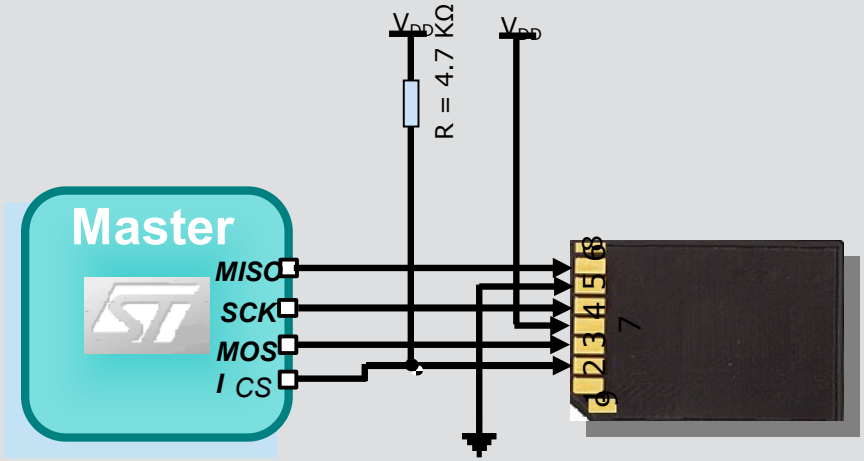


STM32x Cortex M3 - SPI Features

- **Two SPIs: SPI1 on high speed APB2 and SPI2 on low speed APB1**
- **Full duplex synchronous transfers on 3 lines**
- **Simplex synchronous transfers on 2 lines with or without a bi-directional data line**
- **Programmable data frame size :8- or 16-bit transfer frame format selection**
- **Programmable data order with MSB-first or LSB-first shifting**
- **Master or slave operation**
- **Programmable bit rate:** up to 18 MHz in Master/Slave mode
- **NSS management by hardware or software for both master and slave: Dynamic change of Master/Slave operations**

STM32x Cortex M3 - SD/MMC

- **Basic SD/MMC support (SPI protocol):**
  - **Performance: speed up to 18MHz**
  - **Error checking: hardware CRC calculation**

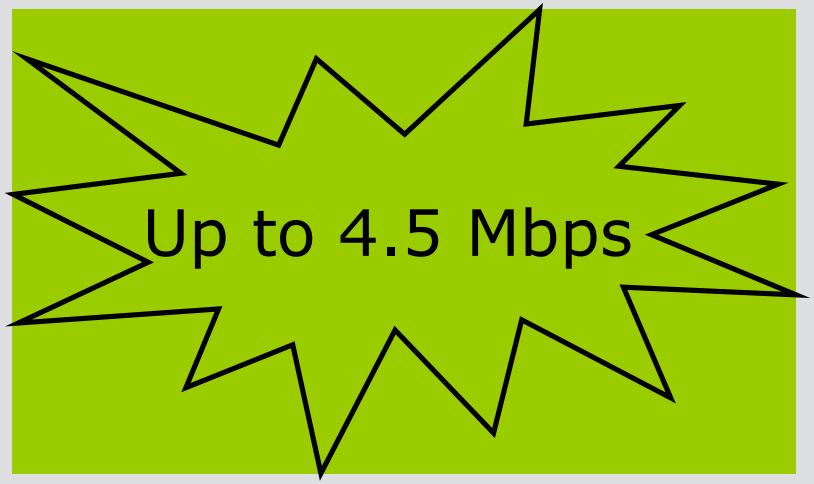


STM32x Cortex M3 - I2C Features

- Multi Master and slave capability
- Controls all I²C bus specific sequencing, protocol, arbitration and timing
- Standard and fast I²C mode (up to 400kHz)
- 7-bit and 10-bit addressing modes
- Dual Addressing Capability to acknowledge 2 slave addresses
- Status flags:
  - Transmitter/Receiver mode flag
  - End-of-Byte transmission flag
  - I2C busy flag
- Configurable PEC (Packet Error Checking) Generation or Verification:
  - PEC value can be transmitted as last byte in Tx mode
  - PEC error checking for last received byte

STM32x Cortex M3 - USART Features

- Three USART: USART1 High speed APB2 and USART2,3 on Low speed APB1
- Fully-programmable serial interface characteristics:
  - Data can be 8 or 9 bits
  - Even, odd or no-parity bit generation and detection
  - 0.5, 1, 1.5 or 2 stop bit generation
  - Programmable baud rate generator
    - Integer part (12 bits)
    - Fractional part (4 bits)
  - Support hardware flow control (CTS and RTS)
- Dedicated transmission and reception flags (TxE and RxNE) with interrupt capability
- Support for DMA
  - Receive DMA request
  - Transmit DMA request



STM32x Cortex M3 - USART Features Cont.

- 10 interrupt sources to ease software implementation
- LIN Master/Slave compatible
- Synchronous Mode: Master mode only
- IrDA SIR Encoder Decoder
- Smartcard Capability
- Single wire Half Duplex Communication
- Multi-Processor communication
  - USART can enter Mute mode
  - Mute mode: disable receive interrupts until next header detected
  - Wake up from mute mode (by idle line detection or address mark detection)

STM32x Cortex M3 - USART Features Cont.

SPI

USART supports Full duplex synchronous communication mode
Full-duplex, three-wire synchronous transfer
USART Master mode only
Programmable clock polarity (CPOL) and phase (CPHA)
Programmable Last Bit Clock generation
Transmitter Clock output (SCLK)

IrDA

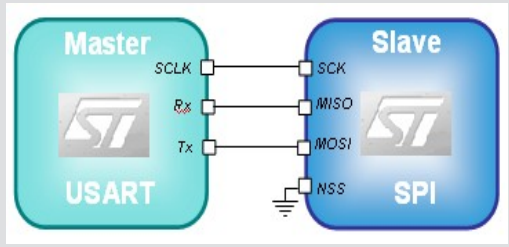
USART supports the IrDA Specifications
Half-duplex, NRZ modulation,
Max bit rate 115200 bps
3/16 bit duration for normal mode
Low power mode: 1.42MHz<USART Prescaler<2.12MHz

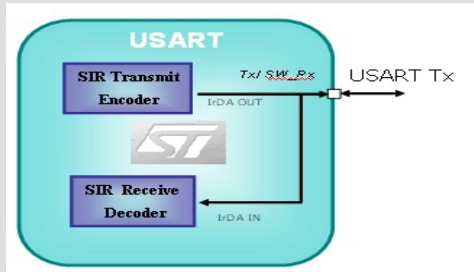
Smart Card Emulation

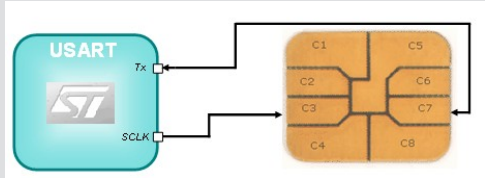
USART supports Smart Card Emulation ISO 7816-3
Half-Duplex, Clock Output (SCLK)
9Bits data, 0.5 Stop Bit in receive, 1.5 Stop Bits in transmit
Parity Error Generation with NACK transmission
Programmable Guard Time
Programmable Clock Prescaler to guarantee a wide range clock input

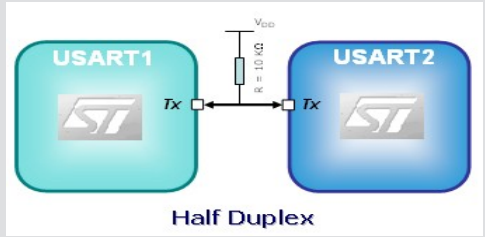
Single Wire Half Duplex mode

USART supports Half duplex synchronous communication mode
Only Tx pin is used (Rx is no longer used)
Used to follow a single wire Half duplex protocol.







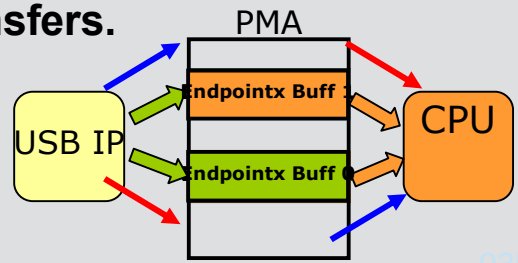


STM32x Cortex M3 - CAN

- Main features:
  - Supports CAN protocol version 2.0 A, B Active
  - Bit rates up to 1Mbit/s
  - Support the time Triggered Communication option
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
  - Time Stamp on SOF transmission
- Reception
  - Two receive FIFOs with three stages
  - 14 scalable filter banks
  - Identifier list features
  - Configurable FIFO overrun
  - Time Stamp on SOF reception

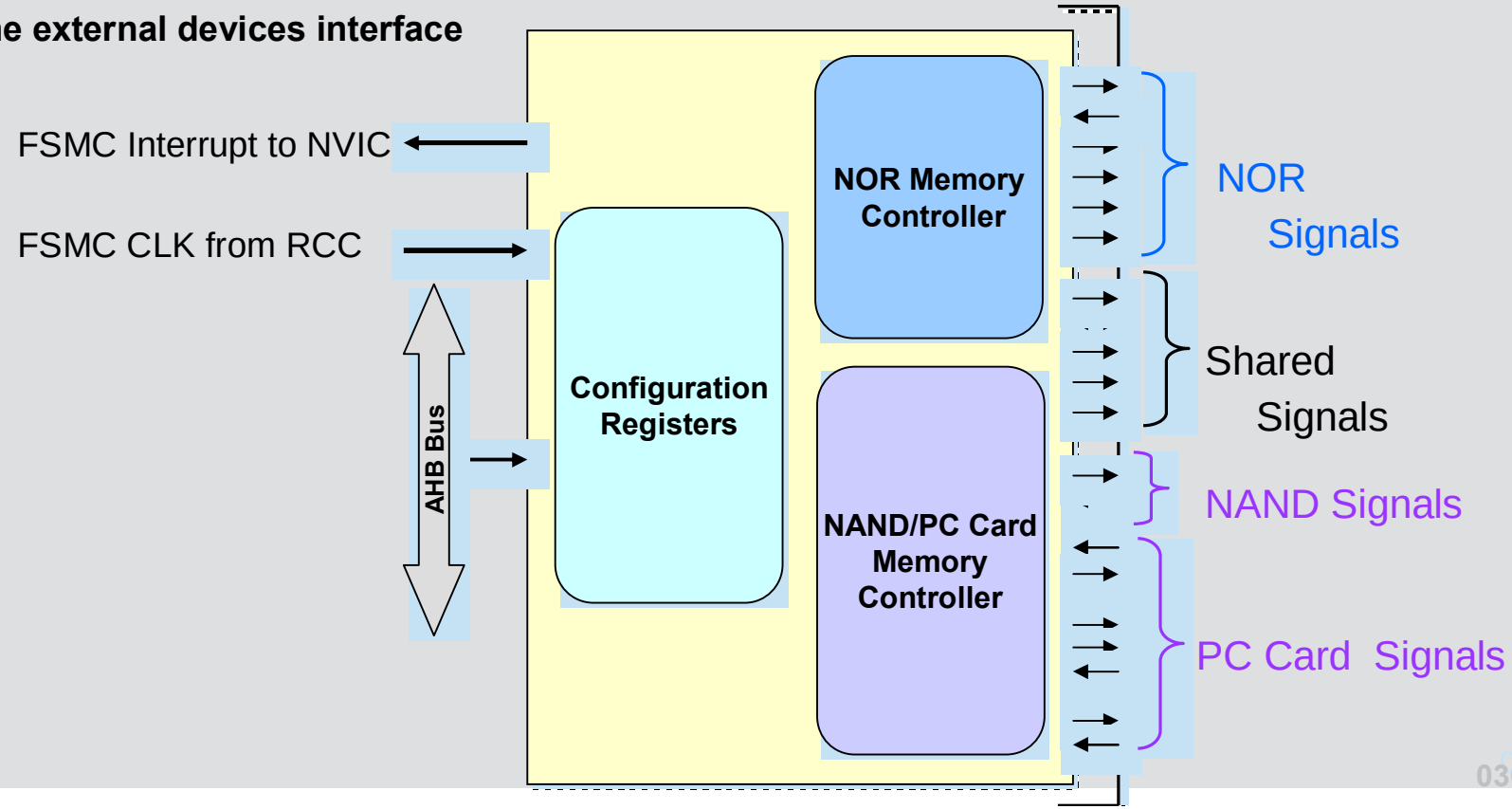
STM32x Cortex M3 - USB

- Fully Certified USB2.0 12Mbps (Full Speed) Device
- Configurable endpoints transfer mode type:
  - control, bulk, interrupt and Isochronous.
- Configurable number of endpoints:
  - up to 8 bidirectional endpoints and 16 mono-directional endpoints.
- USB suspend/resume support.
- Dedicated SRAM Area (Packet Memory Area) up to 512bytes
  - (shared with CAN).
- Dynamic buffer allocation according to the user needs.
- Special double buffer support for Isochronous and Bulk transfers.



STM32x Cortex M3 - External Memory Interface: EMI / FSMC

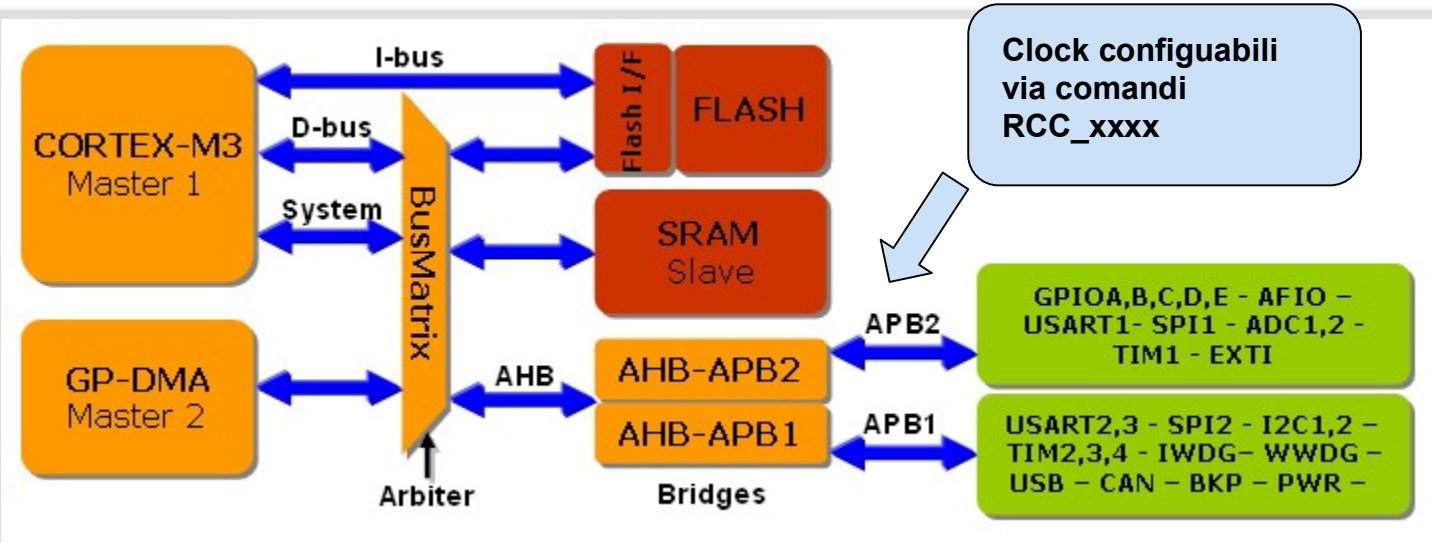
- The FSMC consists of four main blocks:
  - The AHB interface (including the IP configuration registers)
  - The NOR Flash/PSRAM controller
  - The NAND Flash/PC Card controller
  - The external devices interface



STM32x Cortex M3 - DAC

- **Two DAC converters: one output channel for each one**
- **8-bit or 12-bit monotonic output**
- **Left or right data alignement in 12-bit mode**
- **Synchronized update capability**
- **Noise-wave or Triangular-wave generation**
- **Dual DAC channel independent or simultaneous conversions**
- **DMA capability for each channel**
  - **Request generated when External Trigger occurs**
- **External triggers for conversion**
- **DAC supply requirement: 2.4V to 3.6 V**
- **Conversion range: 0 to 3.6 V**
- **DAC outputs range: 0 ≤ DAC_OUTx ≤ VREF+ (VREF+ and VREF- available only in 100 and 144 pins package,** ADC and DAC share the same VREF+)

STM32x Cortex M3 - BUS



- Multiply possibilities of bus accesses to SRAM, Flash, Peripherals, DMA
  - **BusMatrix added to Harvard architecture allows parallel access**
- Efficient DMA and Rapid data flow
  - **Direct path to SRAM through arbiter, guarantees alternating access**
  - **Harvard architecture + BusMatrix allows Flash execution in parallel with DMA transfer**
- Increase Peripherals Speed for better performance
  - **Dual Advanced Peripheral buses (APB) architecture w/ High Speed APB (APB2) up to 72MHz and Low Speed APB (APB1) up to 36MHz**

➔ **Allows to optimize use of peripherals (18MHz SPI, 4.5Mbps USART, 72MHz PWM Timer, 18MHz toggling I/Os)**

STM32x Cortex M3 – STM32F103/107

Both lines include up to:

- Up to 256KB FLASH
- Multiple com. Peripherals
  USART, SPI, I2C
- Multiple 16-bit TIMERS
- Dual DAC
- ETM
- Main Osc 3-16MHz
- Internal 8 MHz RC and 40 kHz RC
- Real Time Clock
- 2 x Watchdogs
- Reset circuitry
- Up to 12 channels DMA
- 80% GPIO ratio

STM32F107

72MHz CPU | Up to 64KB SRAM | 2x12-bit ADC (1µs) Temp sensor | USB 2.0 OTG FS | 2xCAN 2.0B | 2xI2S High Quality Audio | 1 x PWM timer | Ethernet IEEE1588

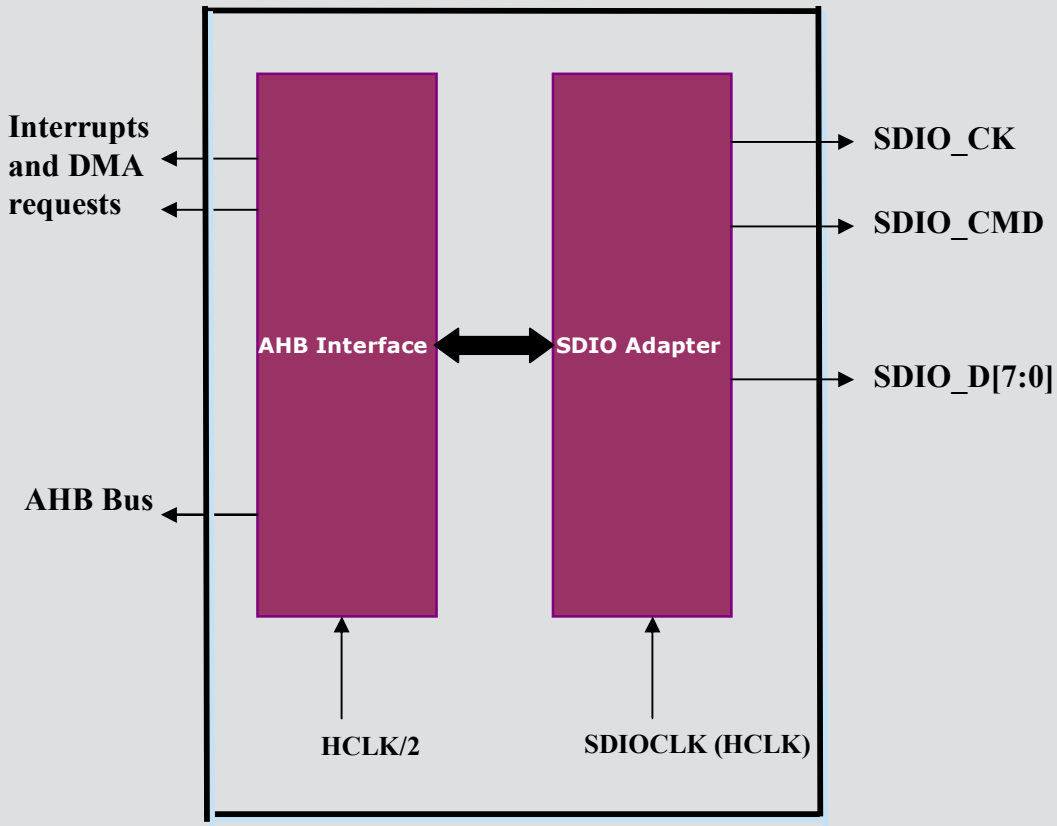
+

STM32F105

72MHz CPU | Up to 64KB SRAM | 2x12-bit ADC (1µs) Temp sensor | USB 2.0 OTG FS | 2xCAN 2.0B | 2xI2S High Quality Audio | 1 x PWM timer

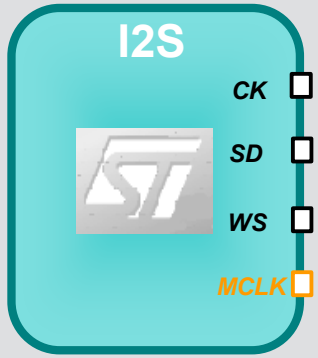
STM32x Cortex M3 - SDIO

- The SDIO consists of two parts:
  - The SDIO adapter block provides all functions specific to the **MMC/SD/SD I/O** card such as the clock generation unit, command and data transfer.
  - The AHB interface accesses the SDIO adapter registers, and generates interrupt and DMA request signals.



STM32x Cortex M3 - I2S audio protocol

- Two I2Ss: Available on SPI2 and SPI3 peripherals.
- Simplex communication (only transmitter or receiver)
- Master or slave operations.
- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8KHz to 48KHz)
- Programmable data format (16-, 24- or 32-bit data formats)
- Programmable packet frame (16-bit and 32-bit packet frames).
- Underrun flag in slave transmit mode and Overrun flag in receive mode.
- 16-bit register for transmission and reception.
- I2S protocols supported:
  - I2S Phillips standard.
  - MSB Justified standard (Left Justified).
  - LSB Justified standard (Right Justified).
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)



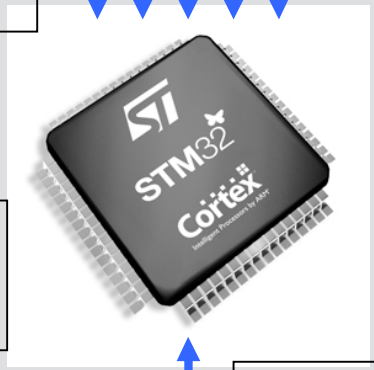
STM32x Cortex M3 – I2S, FSMC, SDIO, Serial

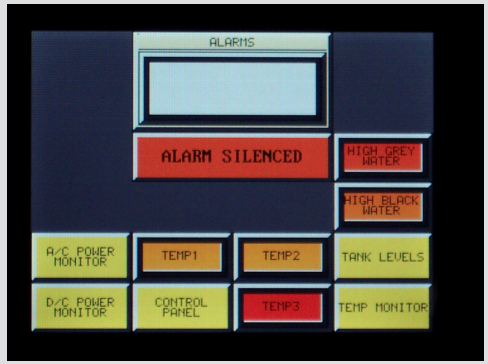
Serial coms and I/Os
5 Uarts/ 3 SPI/ 2I2C
5 timers, up to 112 I/Os
3 ADC, 21 channels

To phone line, alarm sensors and I/Os

FSMC
Parallel interface to graphic module

I2S
Interface to audio DAC for superior audio quality





Audio for the user
Voice and music

SDIO
SD card and SD modules

SD card for software upgrade

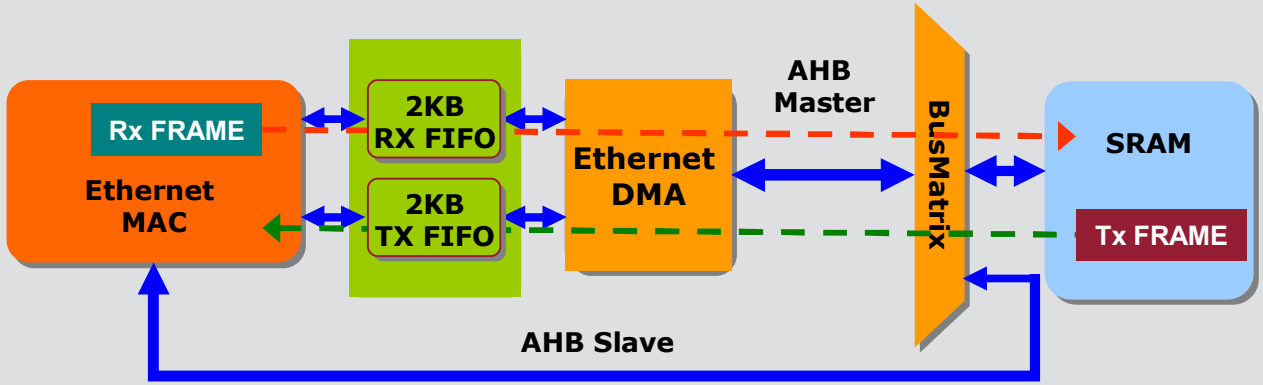
Wi-Fi to home network

STM32x Cortex M3 - Ethernet MAC 10/100

- Supports 10/100Mbits, Half/Full-duplex operations modes, with external PHY interface.
- Dedicated DMA controller with two sets of FIFOs.
- Supports Ethernet frame time stamping.
- Supports Power-down mode.
- Two interrupt vectors:
  - Ethernet normal operations.
  - Ethernet wakeup event.
- Compliant with the following standards:
  - IEEE 802.3-2002 for Ethernet MAC
  - IEEE 1588-2002 standard for precision networked clock synchronization
  - RMII specification from RMII consortium

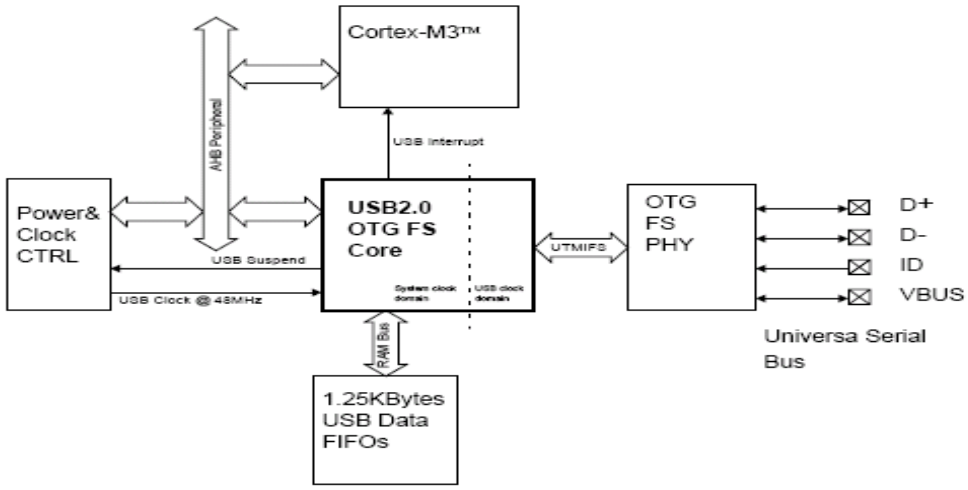
STM32x Cortex M3 - MAC FIFOs

- The MAC core has two sets of FIFOs, of 2KB each one, with a configurable threshold.
- Two modes for popping data towards the MAC, for frames transmission:
  - Threshold mode: as soon as the threshold level is reached.
  - Store-and-Forward mode: a complete frame is stored into the FIFO.
- Two modes for popping data towards the DMA, for frames reception:
  - Cut-through mode: as soon as the threshold level is reached.
  - Store-and-Forward mode: a complete frame is received into the FIFO.

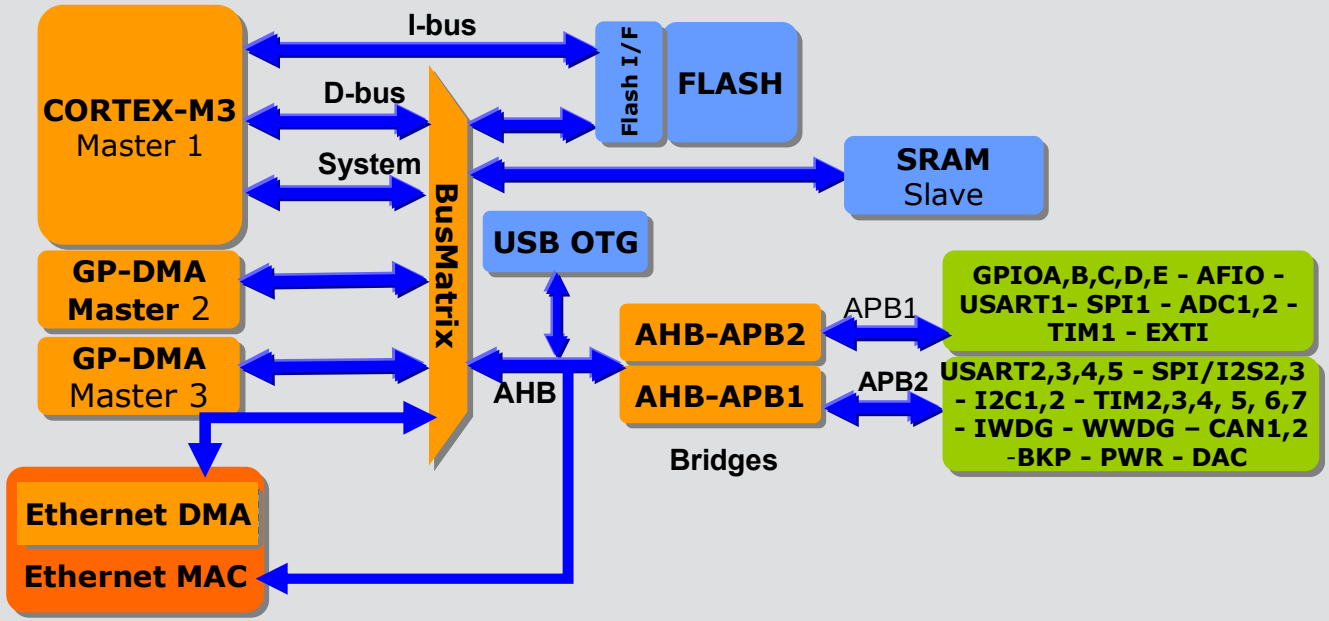


STM32x Cortex M3 - USB 2.0 On-The-Go Full Speed

- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Rev 1.3)
- Operates in Full-Speed and Low Speed (FS, 12-Mbps, LS 1.5 Mbps) mode.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
- Operate in Host, device and OTG modes.



STM32x Cortex M3 – STM32F103/107



LINK

ST-MCU
http://www.st.com/mcu/index.html

STM32
http://www.st.com/mcu/inchtml-pages-stm32.html

Documents and files for family STM32
http://www.st.com/mcu/familiesdocs-110.html

STM32 for motor control
http://www.st.com/mcu/inchtml-pages-stm32mc.html

MCU Training & Seminars
http://www.st.com/mcu/inchtml-pages-mcu_train.html

Product Brochures & Selectors
http://www.st.com/stonline/products/promlit/p_microcontrollers.htm

Extra info
http://emcu.altervista.org/