STM32® 32-bit Flash microcontroller

powered by

ARM® Cortex™-M3

Technical part

10/10/2009

Silica Cortex
Speed Way
2009

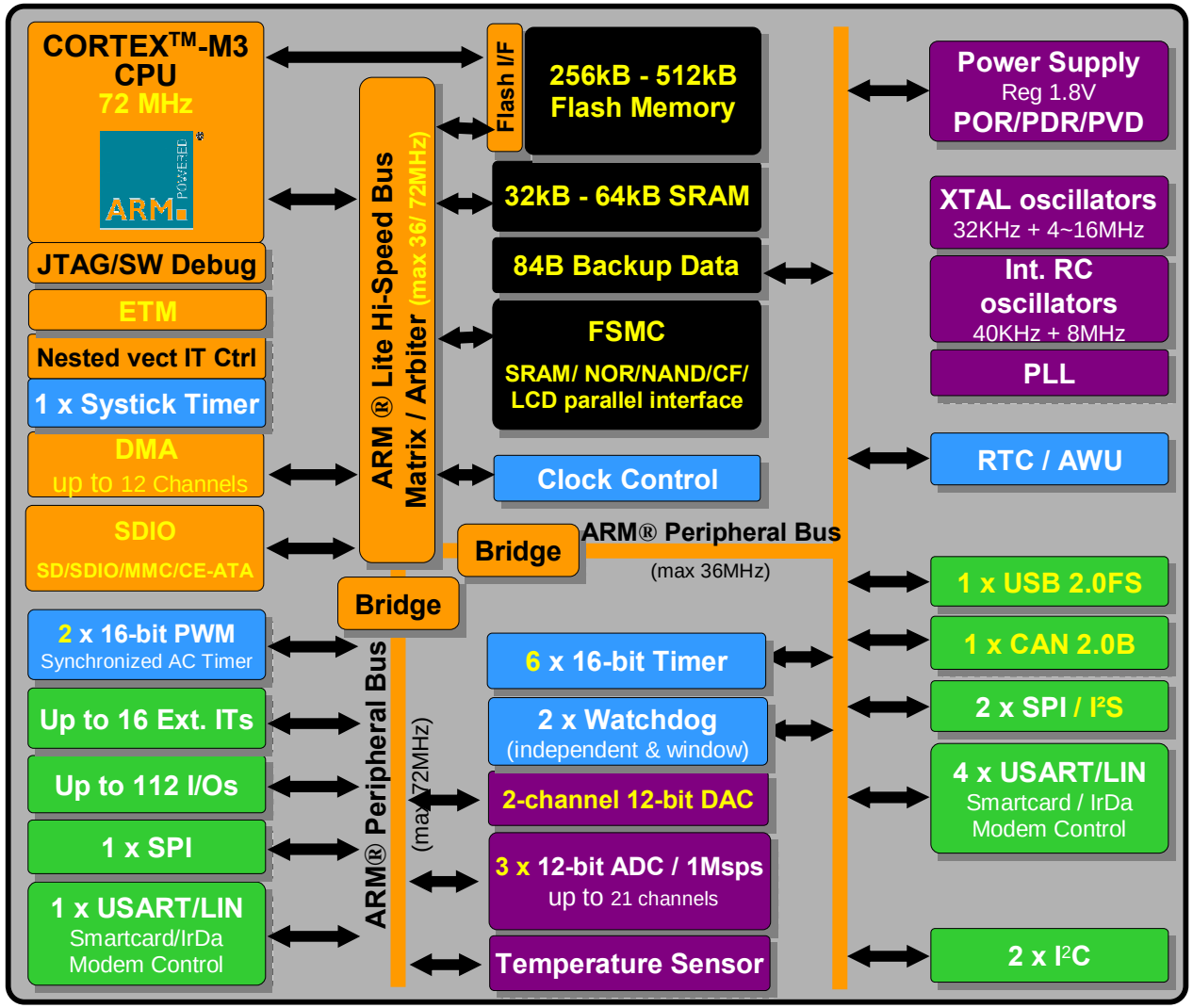
Agenda

- STM32 General Purpose (GP) technical presentation
  - STM32 architecture
  - STM32 system and standard peripherals
  - Advanced peripherals (High Density series)

- STM32 Connectivity Line technical presentation
  - New peripherals: Ethernet, USB OTG, 2 x CAN

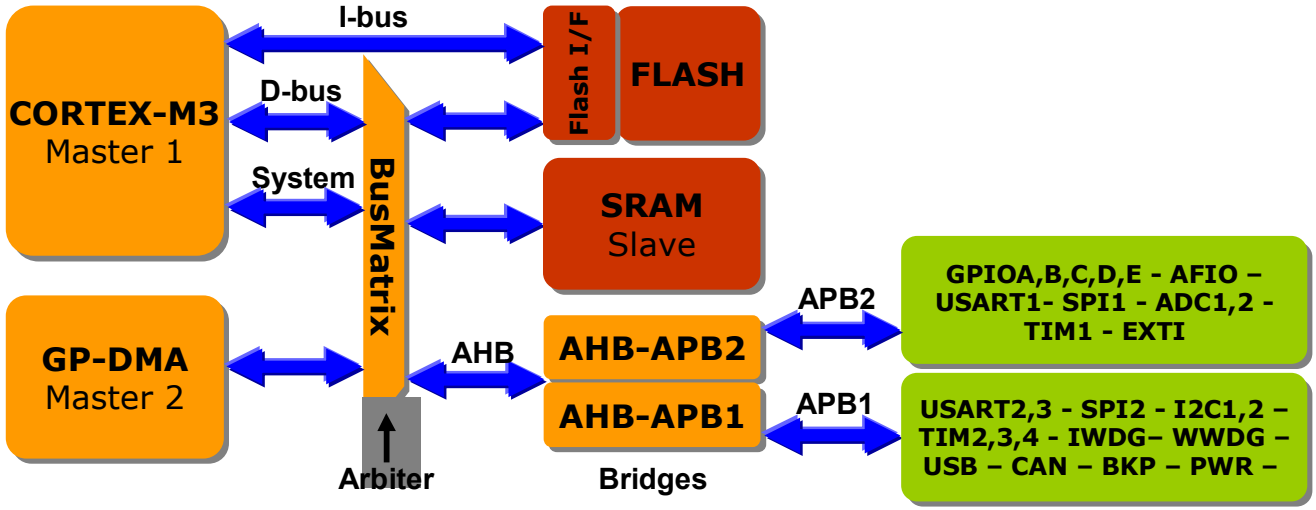
STM32F103 Performance Line 16-512Kb Flash (High Density series)

- 2-channel 12-bit DAC
- FSMC
- ETM
- SDIO
- I²S
- 12 channels DMA
- 2xPWM timers
- 3xADCs
- Up to 112 I/Os (144 pins package)



STM32 GP System Architecture

- **Multiply possibilities of bus accesses to SRAM, Flash, Peripherals, DMA**
  - BusMatrix added to Harvard architecture allows parallel access
- **Efficient DMA and Rapid data flow**
  - Direct path to SRAM through arbiter, guarantees alternating access
  - Harvard architecture + BusMatrix allows Flash execution in parallel with DMA transfer
- **Increase Peripherals Speed for better performance**
  - Dual Advanced Peripheral buses (APB) architecture w/ High Speed APB (APB2) up to 72MHz and Low Speed APB (APB1) up to 36MHz
  - ➔ Allows to optimize use of peripherals (18MHz SPI, 4.5Mbps USART, 72MHz PWM Timer, 18MHz toggling I/Os)

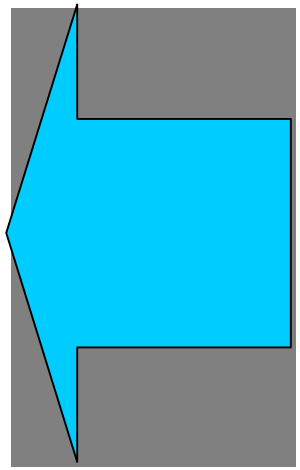


Buses are not overloaded with data movement tasks

STM32 GP standard peripherals set

Both lines have up to:

- 5 x USART
- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
- RTC
- Int 8 MHz RC
  Int 40 kHz RC
- 2xWDG
- POR/PDR/
  PVD brown out
- 12 DMA
- 80% GPIO ratio
- Up to 512KB FLASH
- Backup Domain



The STM32 has a 'standard' set of peripherals common to all versions of the family, offering unparalleled levels of flexibility for your applications

Embedded FLASH

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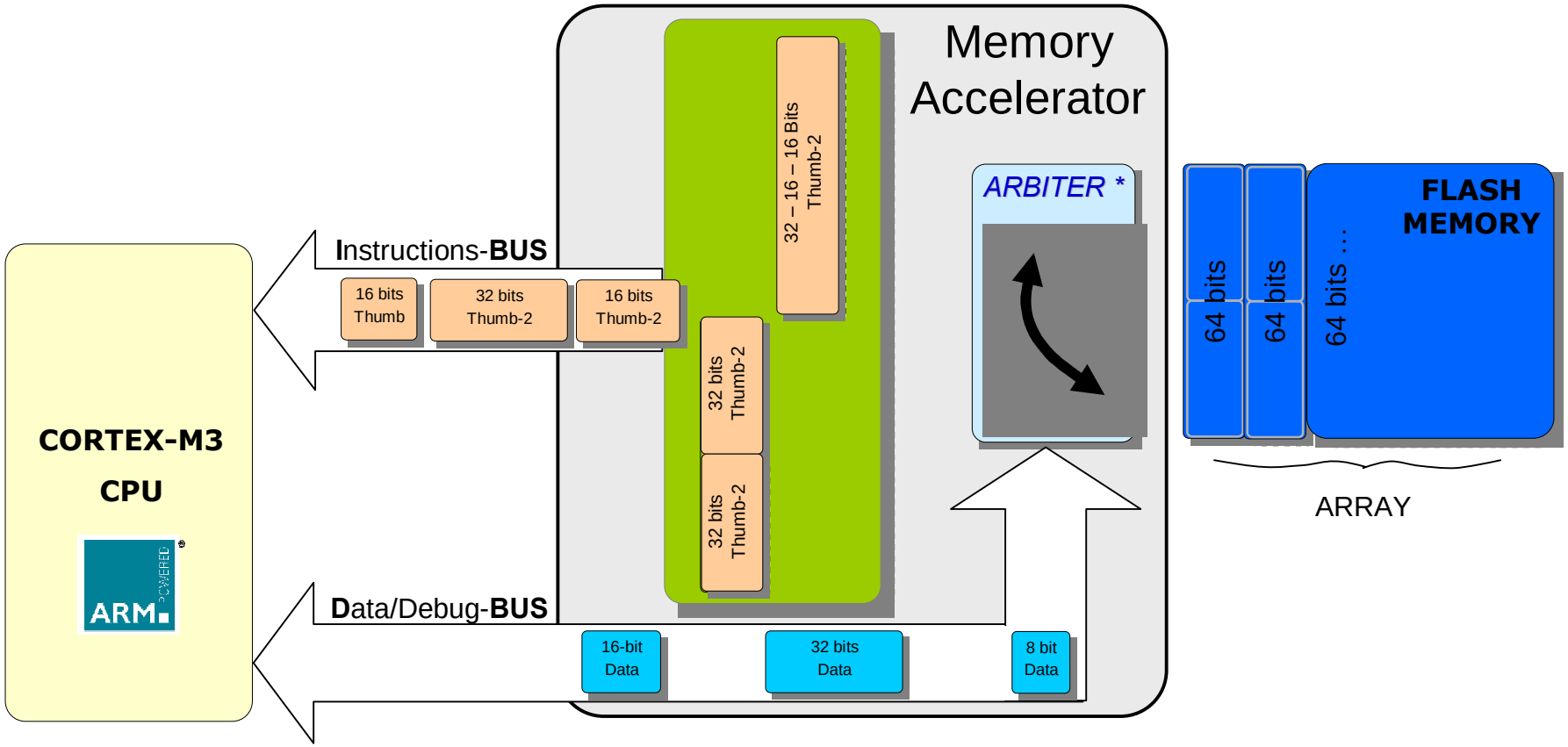
- 32K - 128K : 1K byte Page Size
- 256K – 512K : 2K Page Size
- 10K write/erase cycles
- Data Retention:
  - 30 year lifetime over whole temperature range
- Information Block
  - Big Information Block - 2K – Bootloader
  - Small Information Block – 512B – User / Option Bytes
- Protection
  - Write Protection
  - Read Protection
    - Automatically triggers write protection on 1st 4K of Flash

Flash Memory Accelerator

- Mission: Support 72 MHz operation directly from Flash memory
- 64-bits wide Flash with Prefetch (2 × 64bits buffers)



* The data (constant or literals) are provided with the highest priority using the D-Bus.

Clock System

Both lines have up to:

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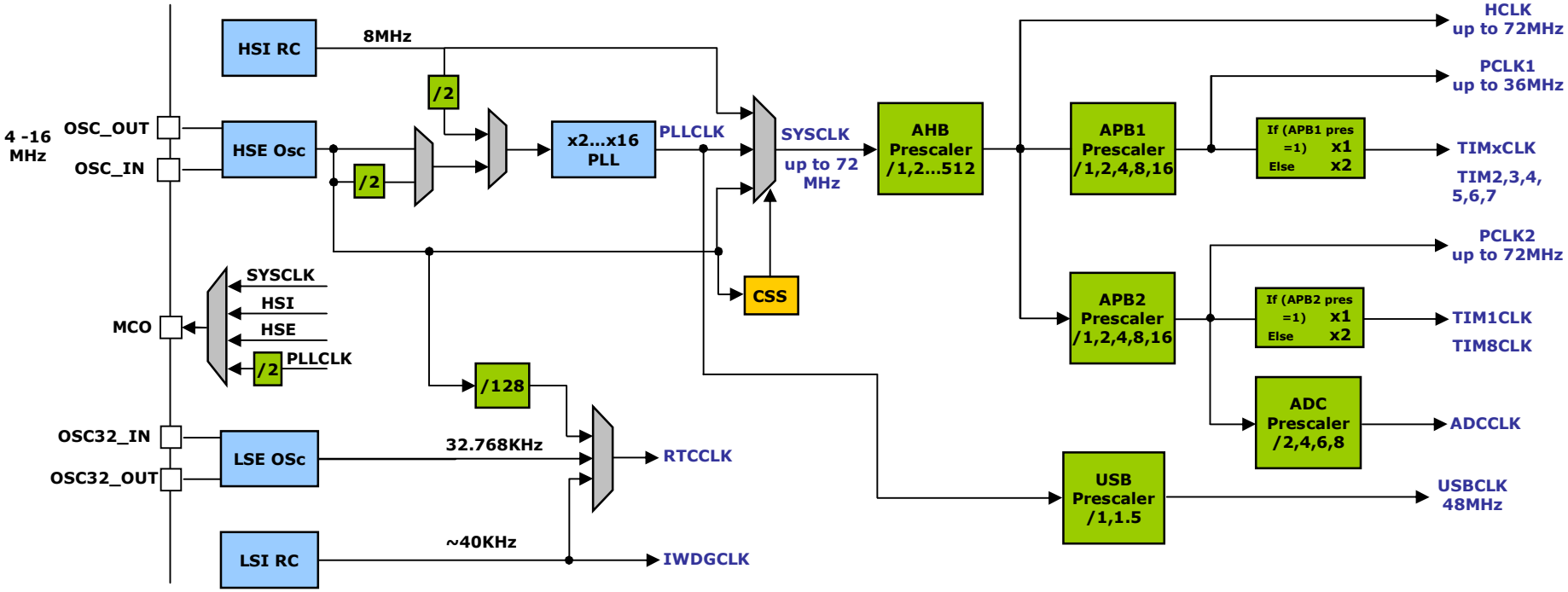
- **Multiple clock sources for full flexibility in RUN/Low Power modes**
  - HSE (High Speed External oscillator): 4MHz to 16MHz main osc which can be multiplied by the PLL to provide a wide range of frequencies
  - HSI (High Speed Internal RC): factory trimmed internal RC oscillator 8MHz +/- 1% over 0-70°C temp range
    - PLL up to 64MHz
    - Feeds System clock after reset or exit from STOP mode for fast startup
      - startup time : 2us max
    - Clock Security System; Backup clock in case HSE osc fails
  - LSI (Low Speed Internal RC): 40KHz internal RC for IWDG and optionally for the RTC used for Auto Wake-Up (AWU) from STOP/STANDBY mode
    - Can be calibrated through Timer 5
  - LSE (Low Speed External oscillator): 32.768kHz osc provides a precise time base with very low power consumption (max 1µA). Optionally drives the RTC for Auto Wake-Up (AWU) from STOP/STANDBY mode

Clock Scheme

- **System Clock (SYSCLK) sources**
  - ✓ HSI
  - ✓ HSE
  - ✓ PLL
- **RTC Clock (RTCCLK) sources**
  - ✓ LSE
  - ✓ LSI
  - ✓ HSE clock divided by 128
- **USB Clock (USBCLK) provided from the internal PLL**
- **Clock-out capability on the MCO pin (PA.08) / max 50MHz**
- **Configurable dividers provides AHB, APB1/2, ADC and TIM clocks**
- **Clock Security System (CSS) to backup clock in case of HSE clock failure (HSI feeds the system clock)**
  - Enabled by SW w/ interrupt capability linked to Cortex NMI



Power / Reset Management

Both lines have up to:

- 5 x USART
- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
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  Int 40 kHz RC
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- 80% GPIO ratio
- Up to 512KB FLASH
- Backup Domain

- POR / PDR (Power On Reset / Power Down Reset)
  - Integrated POR / PDR circuitry guarantees proper product reset when voltage is not in the product guaranteed voltage range (2V to 3.6V)
  - No need for external reset circuit
- POR and PDR have a typical hysteresis of 40mV

- Programmable Voltage Detector
  - Enabled by software
  - Monitor the VDD power supply by comparing it to a threshold
  - Threshold configurable from 2.2V to 2.9V by step of 100mV
  - Generate interrupt through EXTI Line16 (if enabled) when VDD < Threshold and/or VDD > Threshold

➔ Can be used to generate a warning message and/or put the MCU into a safe state

Backup Domain

Both lines have up to:

- 5 x USART
- 3 x SPI
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- 6 x 16-bit Timers
- RTC
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- 80% GPIO ratio
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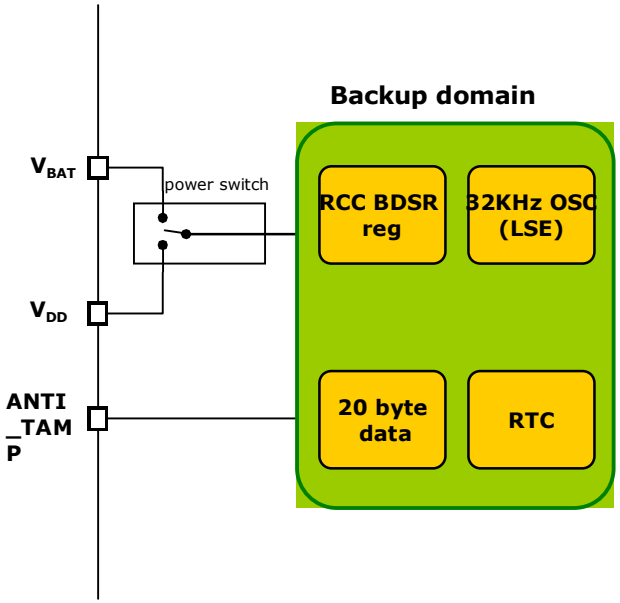
- Backup Domain

Backup Domain contains

- RTC (Counter, Prescaler and Alarm mechanism)
- Separate 32KHz Osc (LSE) for RTC
- User backup data
  - 20bytes on 32-128K Silicon
  - 80bytes on 256K+ Silicon
- RCC BDSR register: RTC source clock selection and enable + LSE config
- ➔ Reset only by Backup domain RESET



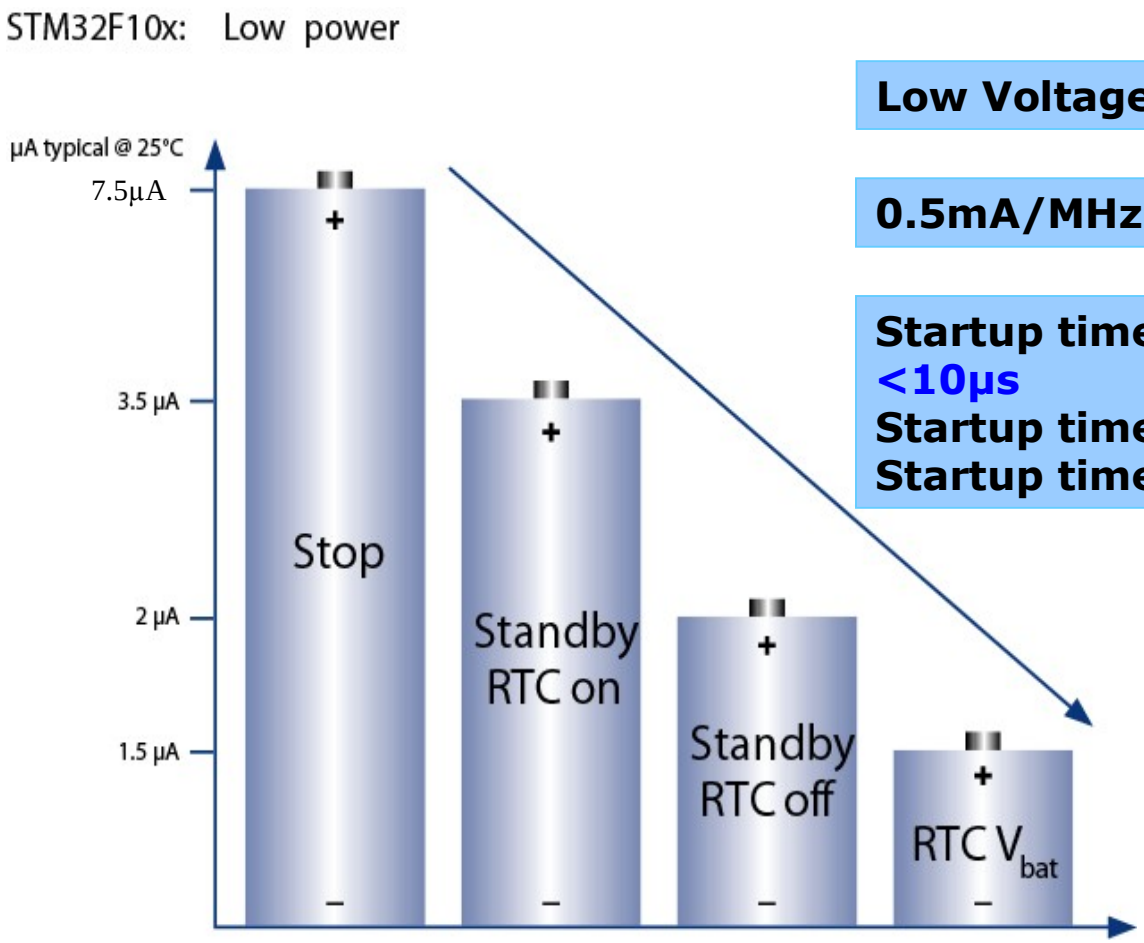
V_{BAT} independent voltage supply

- Automatic switch-over to V_{BAT} when V_{DD} goes lower than PDR level
- No current sunk on V_{BAT} when V_{DD} present

Tamper detection: resets all user backup registers

- Configurable level: low/high
- Configurable interrupt generation

STM32F10x: Low Power



Low Voltage 2.0V to 3.6V operation

0.5mA/MHz in RUN mode from Flash

Startup time From STOP (Vreg Off) **<10µs**
Startup time From STOP (Vreg On) **4µs**
Startup time From STANDBY **40µs**

STOP
- All clocks off, Reset ON, RAM ON (registers' content preserved)

STANDBY
- All clocks off, Reset ON, RAM OFF but 20 bytes available for backup

STM32 Current Consumption for DSP comparrison

- Here is where the STM32 makes the difference vs. low-end DSPs

Device	*Manufacturer*	*Condition*	*Typ(mA)*	*Max(mA)*
STM32F103x	**ST**	**72MHz**	**36**	**50**
DSPIC30F1010202X	Microchip	60MHz	223	267
DSPIC30F2010		60MHz	94	150
DSPIC33F2010		80MHz	54	90
DSPIC33FJXXXGPX06/X08/X10		80MHz	84	89
PIC32MX		80MHz	55	75
56F803x	Freescale	32MHz	67	N/A
56F8335		60MHz	207	N/A
56F802		80MHz	120	130
TMS320Lx2401	Texas Instruments	40MHz	85	132
TMS320C2802		100MHz	260	315

NB: competitors data extracted from datasheet, not verified on silicon, measurement condition might differ from on chip to the other

DMA

Both lines have up to:

- 5 x USART
- 3 x SPI
- 2 x I²C
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- POR/PDR/
  PVD brown out
- 12 DMA
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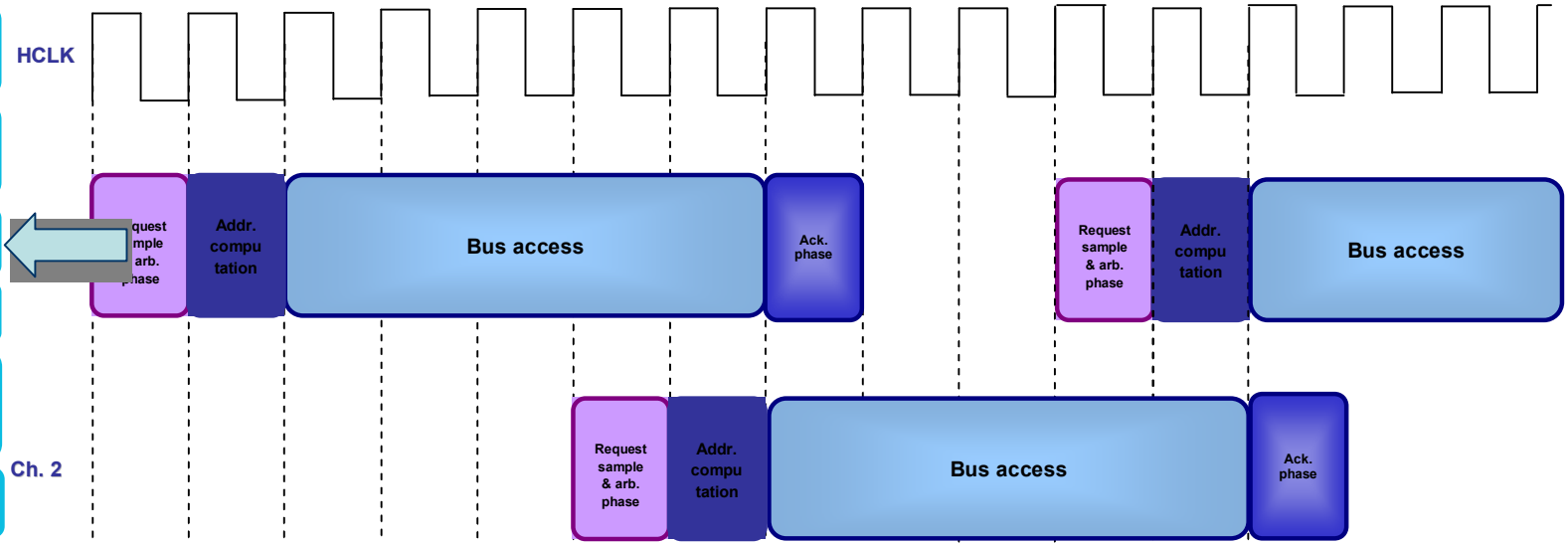
- DMA able to set up second transfer while running first transfer
- 66% of Bus Bandwidth available for DMA, no Stall of CPU core
- Better performance through 'many small packets'
- Memory-to-memory, peripheral-to-memory, memory-to-peripheral transfers and peripheral-to-peripheral
- Programmable data length of up to 65536 bytes
- Supports circular buffer management



GPIO

Both lines have up to:

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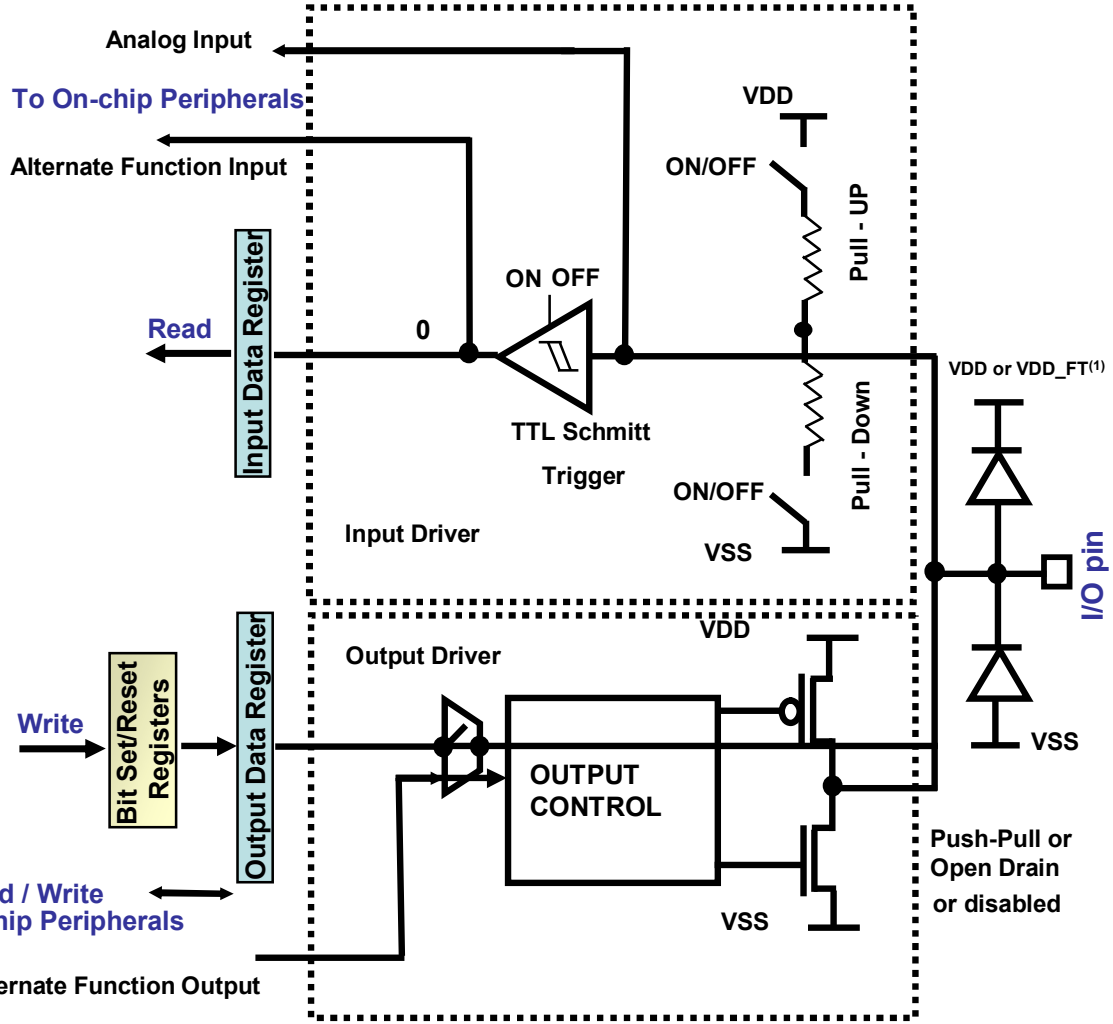
- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
- RTC
- Int 8 MHz RC
  Int 40 kHz RC
- 2xWDG
- POR/PDR/ PVD brown out
- 12 DMA
- 80% GPIO ratio
- Up to 512KB FLASH
- Backup Domain

- All I/O are 5V Tolerant, with 25mA drive
- 18MHz Toggle Speed
- Configurable output speed up to 50MHz
  - Variable slew rate
- Any of the I/O pins can be set to external Interrupt
- Configurable Schmitt Triggers (On/Off)
- Atomic Bit Set and Bit Reset
- Locking Mechanism to prevent spurious writes to registers
  - When the LOCK sequence has been applied on a port bit, it is no longer possible to modify the configuration of the port bit until the next reset
- Some alternate functions can be re-mapped on the pinout

GPIO Configuration Modes

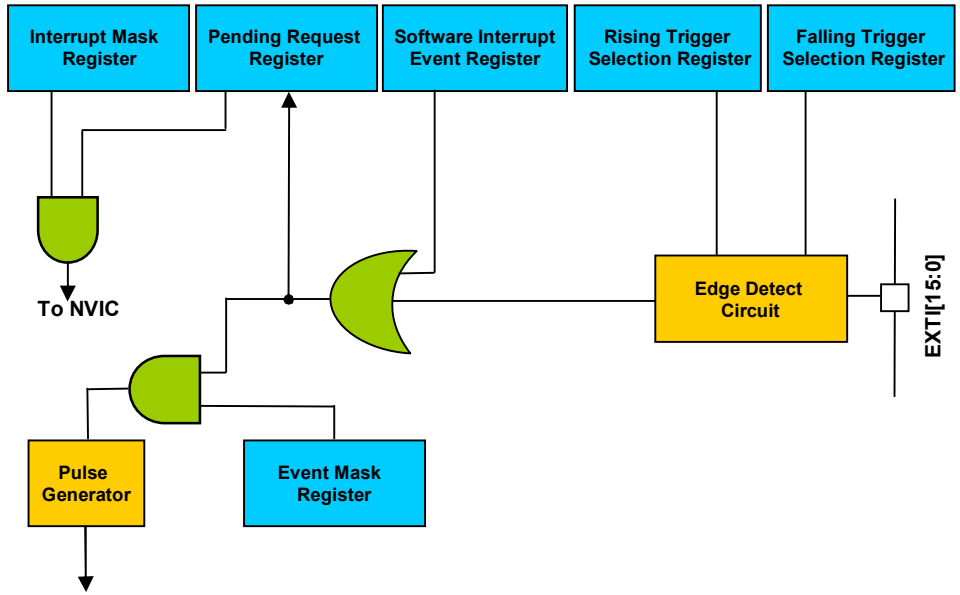
Configuration Mode	CNF1	CNF0	MOD1	MOD0
Analog Input	0	0	00	
Input Floating **(Reset State)**	0	1		
Input Pull-Up	1	0		
Input Pull-Down	1	0		
Output Push-Pull	0	0	01: 10 MHz 10: 2 MHz 11: 50 MHz	
Output Open-Drain	0	1		
AF Push-Pull	1	0		
AF Open-Drain	1	1		

(1) VDD for standard I/Os and VDD_FT is a potential specific to five-volt tolerant I/Os and different from VDD.



External Interrupt (EXTI) Features

- Up to 19 Interrupt/Events requests
  - All GPIO can be used as EXTI line(0..15)
  - EXTI line 16 connected to PVD output
  - EXTI line 17 connected to RTC Alarm event
  - EXTI line 18 connected to USB Wake-up from suspend event
- Two Configuration mode:
  - Interrupt mode: generate interrupts with external lines edges
  - Event mode: generate pulse to wake-up system from WFI, WFE and STOP modes
- Independent trigger (rising, falling, rising & falling) and mask on each interrupt/event line
- Dedicated status bit for each interrupt line
- Generation of up to 19 software interrupt/event requests



- Minimum Pulse Width : < $1*T_{PCLK2}$ (Fast APB)
- EXTI mapped on High Speed APB (APB2) to save time entering in the External Interrupt routine

USART

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- 2 x I²C
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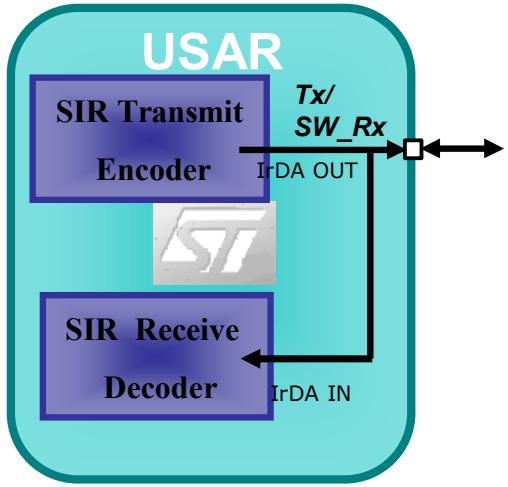
- Backup Domain

- USART 1 upto 4.5Mbps
- USART2,3,4,5 upto 2.5Mbps
- Dedicated Transmission and Receive Flags
- 10 Interrupt Sources, DMA Support
- Fractional Baud Rate Generator
- All USARTs support:
  - Lin Master/Slave
  - IrDA
- USARTS 1,2,3 also support:
  - Smart Card
  - Single Wire
- Multi Processor Communication
  - USART can enter Mute mode
  - Mute mode: disable receive interrupts until next header detected
  - Wake up from mute mode (by idle line detection or address mark detection)



IrDA Support

SPI

Both lines have up to:

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- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
- RTC
- Int 8 MHz RC Int 40 kHz RC
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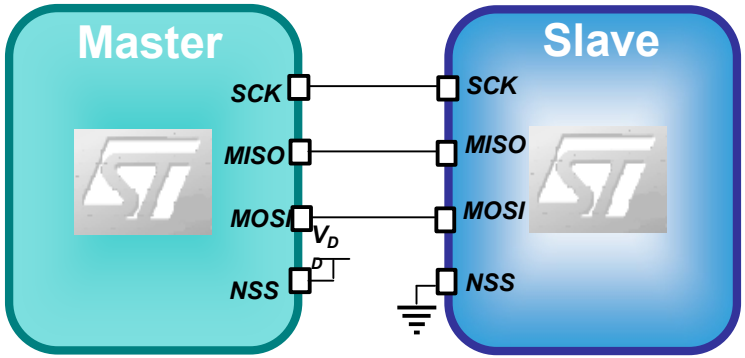
- POR/PDR/ PVD brown out
- 12 DMA
- 80% GPIO ratio
- Up to 512KB FLASH
- Backup Domain

- 8 or 16 Bit Data Frame
- Programmable data order with MSB-first or LSB-first shifting
- Programmable Bit Rate; up to 18MHz in Master/Slave Mode
- $\overline{SS}$ Management by Hardware or Software
  - Dynamic changes of Master/Slave operations
- Hardware CRC generation and Checking
- DMA Support (with 1Byte Buffer)
- Dedicated Transmit and Receive flags with interrupt



I2C

Both lines have up to:

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- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
- RTC
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- 2xWDG
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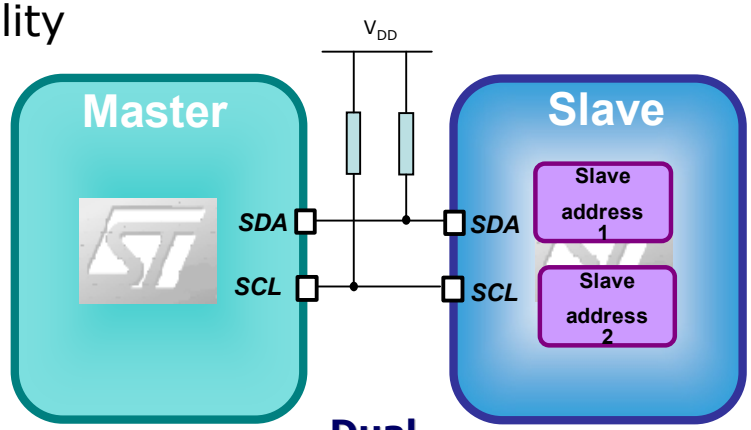
- 12 DMA
- 80% GPIO ratio
- Up to 512KB FLASH
- Backup Domain

- Standard and Fast I2C Modes (up to 400KHz)
- 7 and 10 bit Addressing Mode
- Dual Addressing Capability
  - Able to acknowledge 2 Slave Addresses
- Configurable PEC (Packet Error Checking)
  - Generation or Verification
- 2 Interrupt Vectors, DMA, 1Byte Buffer
- SMBus2.0 & PMBus Compatibility



Dual Addressing

General Purpose Timers

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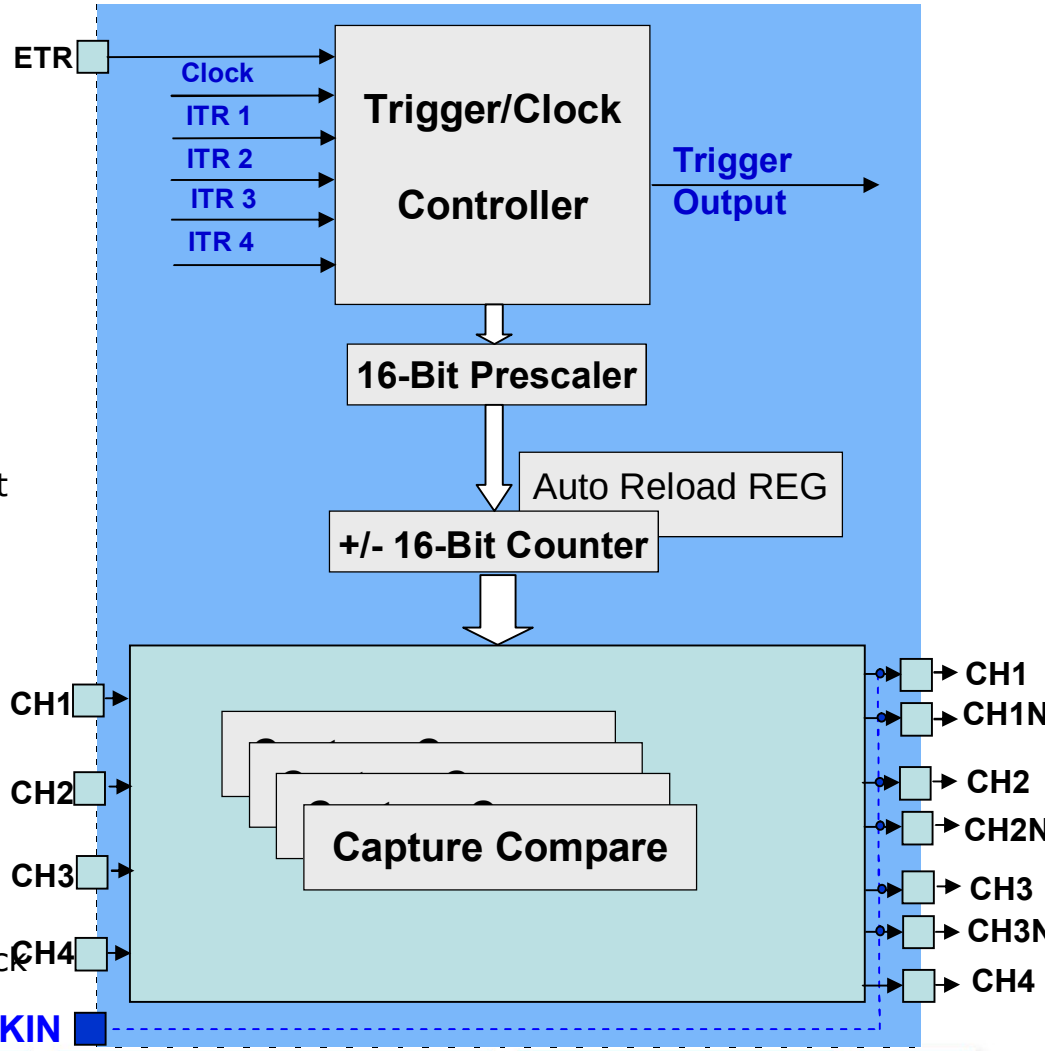
- **All Timers have Internal Clock up to 72MHz**
- **Timers 2, 3, 4 and 5 feature**
  - **4 x 16bit High Resolution Capture/Compare Channels**
    - Output Compare
    - PWM
    - Input Capture, PWM Input Capture
    - One Pulse Mode (including pulse train)
  - **Synchronisation**
    - Timer Master / Slave
    - From External Trigger
    - Trigger or Gated Mode
  - **Encoder Interface**
  - **6 Independent Interrupt / DMA requests**
- **Timers 6 and 7 Feature:**
  - 16-bit auto-reload up-counter with 16-bit Pre Scaler
  - Interrupt/DMA generation on the update event
  - Synchronization circuit to trigger the DAC

Advanced Control Timers : TIM1 and TIM8

- TIM1 and TIM8 on High Speed APB (APB2)
- Internal clock up to 72 MHz
- 16-bit Counter
  - Up, down and centered counting modes
  - Auto Reload
- 4 x 16 High resolution Capture Channels
  - Output Compare
  - PWM
  - Input Capture, PWM input Capture
  - One Pulse Mode
- 6 Complementary outputs: Channel1, 2 and 3
- Output Idle state selection independently for each output
- Polarity selection independently for each output
- Programmable PWM repetition counter
- Hall sensor interface
- Encoder interface
- 8 Independent IRQ/DMA Requests Generation
  - At each Update Event
  - At each Capture Compare Events
  - At each Trigger Input Event
  - At each Break Event
  - At each Capture Compare Update
- Embedded Safety features
  - Break input (asynchronous)
  - Lockable unit configuration: 3 possible Lock level.



Break input

- A break event can be generated by:
  - The BRK input which has a programmable polarity and an enable bit BKE
  - The Clock Security System
- When a break occurs:
  - The MOE bit (Main Output Enable) is cleared
  - The break status flag is set and an interrupt request can be generated
  - Each output channel is driven with the level programmed in the OISx bit
- Break applications:
  - If the AOE is Reset, the MOE remains low until you write it to '1' again
    - Normally used for security with break input connected to an alarm feedback from power stage, thermal sensors or any security components.
  - If the AOE (Automatic Output Enable) bit is set, the MOE bit is automatically set again at the next update event UEV
    - Typically be used for cycle-by-cycle current regulation

Smoke inhibit protections

- Safety critical registers can be “locked”, to prevent power stage damages (software run-away,…)
  - Dead time, PWM outputs polarity, emergency input enable,…
- All target registers are read/write until lock activation (and then read-only if protected)
  - Once the two lock bits are written, they cannot be modified until next MCU reset (write-once bits)
- Three programmable write protection levels
  - Level1: Dead Time and Emergency enable are locked.
  - Level2: Level1 + Polarities and Off-state selection for run and Idle state are locked.
  - Level3: Level2 + Output Compare Control and Preload are locked.
- GPIO configuration can be locked to avoid having the PWM alternate function outputs reprogrammed as standard outputs

Debug feature

- Some applications (e.g. Motor Control) are usually tricky to debug using breakpoints
  - Standard breakpoints may damage the power stage
  - Closed loop systems can hardly be stopped and re-started
- A configuration bit allows to program the behavior of the PWM timer upon breakpoint match
  - Normal mode: the timer continues to operate normally
    - May be dangerous in some case since a constant duty cycle is applied to the inverter (interrupts not serviced)
  - Safe mode: the timer is frozen and PWM outputs are shut down
    - Safe state for the inverter. The timer can still be re-started from where it stops.

RTC (Real Time Clock)

Both lines have up to:

- 5 x USART
- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
- RTC
- Int 8 MHz RC Int 40 kHz RC
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- 12 DMA
- 80% GPIO ratio
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- Backup Domain

- Clock sources
  - 32.768 kHz dedicated oscillator (LSE)
  - Low frequency (40kHz), low power internal RC(LSI)
  - HSE divided by 128
- 3 Event/Interrupt sources
  - Second
  - Overflow
  - Alarm (also connected to EXTI Line 17 for Auto Wake-Up from STOP)
- Register protection against unwanted write operations
- RTC core & clock configuration in Backup domain
  - Independent V_{BAT} voltage supply
  - Reset only by Backup domain reset
  - RTC config kept after reset or wake-up from STANDBY
- Calibration Capability
  - RTC clock can be output on Tamper pin for calibration
  - Then the clock can be adjusted from 0 to to 121ppm by a step of 1ppm
- RTC is part of the Backup Domain

Watchdogs

Both lines have up to:

- 5 x USART
- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
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  Int 40 kHz RC
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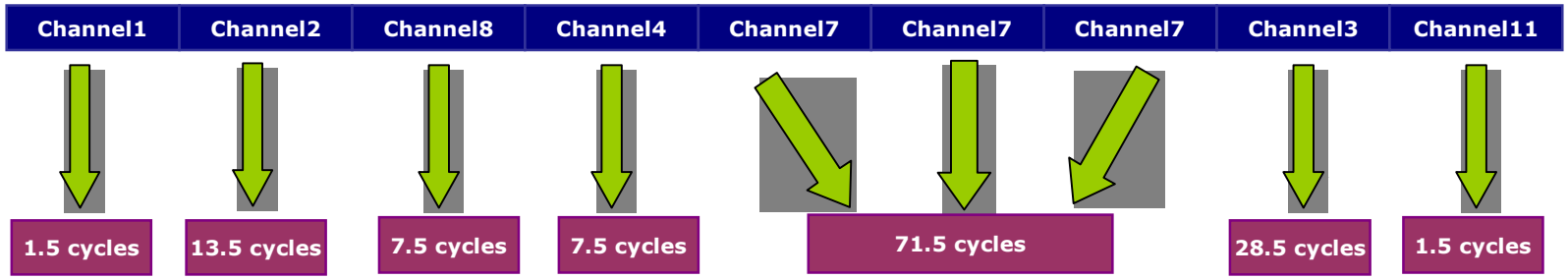
- Window Watchdog (WWDG)
  - Configurable Time Window
  - Can detect abnormally early or late application behaviour
  - Conditional Reset
  - WWDG Reset flag
- Independent Watchdog (IWDG)
  - Dedicated low speed clock (LSI)
  - IWDG clock still active if main clock fails
  - Still functional in Stop/Standby
  - Wake-up from stop/standby
  - Min-max Timeout values 125usec – 32.8sec
  - Part of the Backup Domain

ADC Main Features

- ADC conversion rate 1 MHz and 12-bit resolution
  - *1µs conversion time at 56 MHz*
  - *1.17µs conversion time at 72 MHz*
- Conversion range: 0 to 3.6 V
- ADC supply requirement: 2.4V to 3.6 V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
  - V_{REF+} and $V_{REF-pins}$ available only in 100 and 144 pins package
- 3 ADCs with up to 23 analog inputs
  - 21 external
  - 2 internal (Vrefint and Temp Sensor) connected to ADC1
- Dual mode (on devices with 2 or 3 ADCs): 8 conversion mode
- DMA Support on ADC1 (ADC2) and ADC3
- Channels conversion groups:
  - Up to 16 channels regular group
  - Up to 4 channels injected group
- Single and continuous conversion modes

ADC Features (2/3)

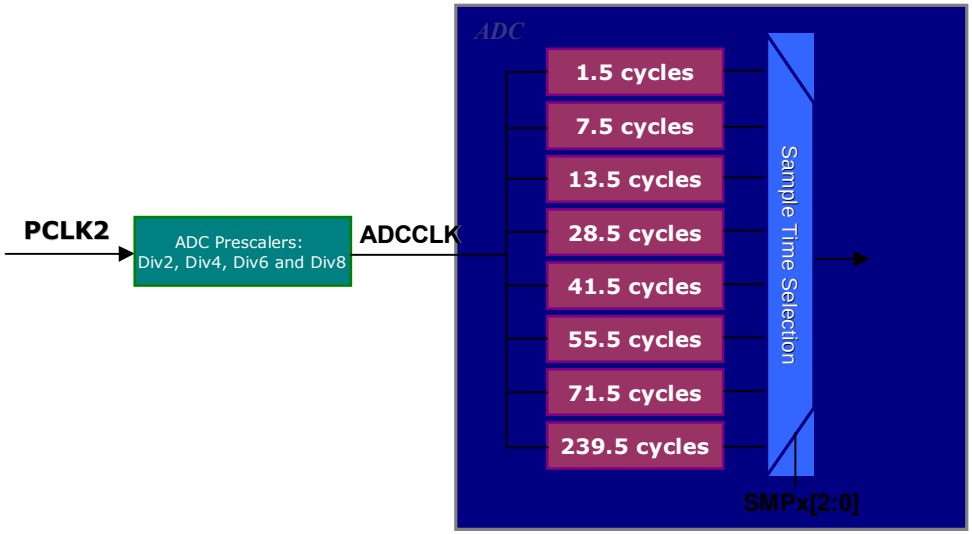
- Analog Watchdog (1 channel or all regular or all injected)
- Sequencer-based scan mode
  - Any channel, any order (e.g. Ch3, Ch2, Ch11, Ch11, Ch3)
  - up to 16 regular conversion (transferred by DMA)
  - up to 4 injected conversion stored in internal registers



- Multiple trigger sources for both regular and injected conversion
  - Each group can be started by 6 events from the 4 timers (compare, over/underflow)
  - External event and software trig also available

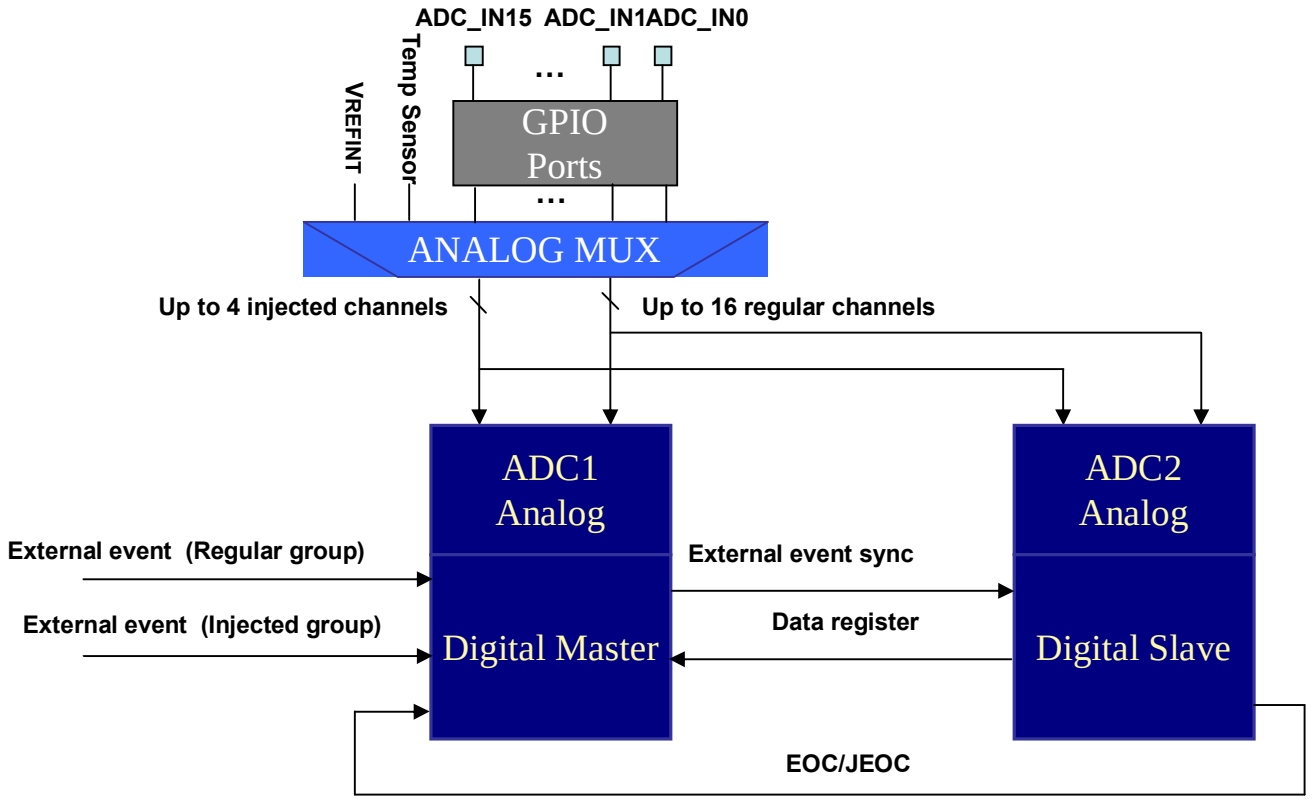
ADC Features (3/3)

- Left or right Data alignment with built-in data coherency
- 4 offset compensation registers
  - Compensates external conditioning components offsets (such as Operational Amplifiers). Provides signed results if needed.
- Channel-by-channel programmable sampling time to be able to convert signals with various impedances
  - From 1µs (for Rin < 1.2KΩ) to 18µs (Rin < 350KΩ), 8 values



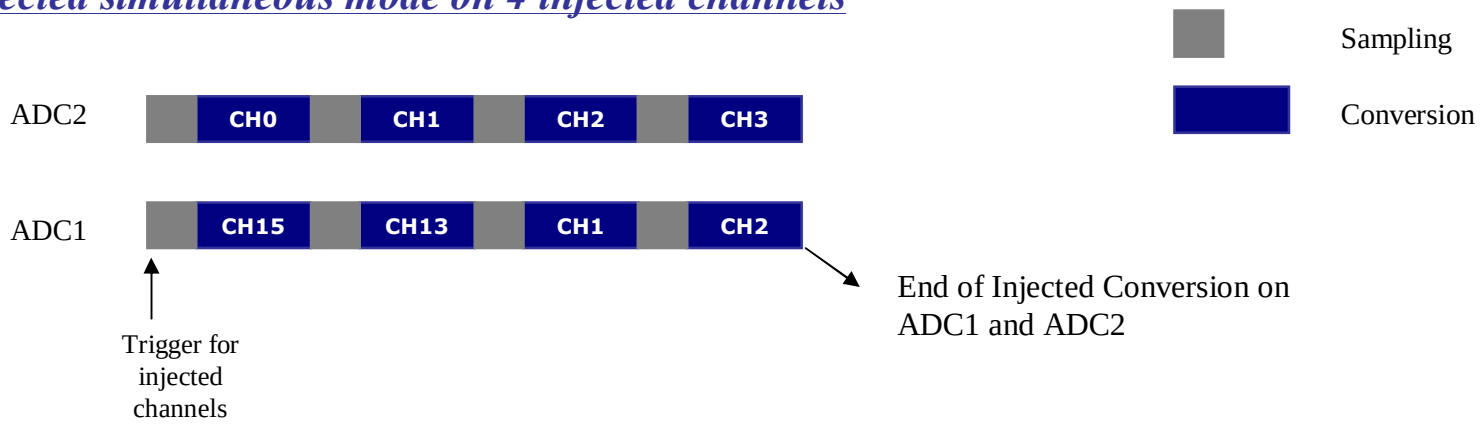
ADC dual modes (1/2)

- Available in devices with two ADCs (Performance line)
  - ADC1 and ADC 2 can work independently or coupled (master/slave)
- 8 ADC dual modes

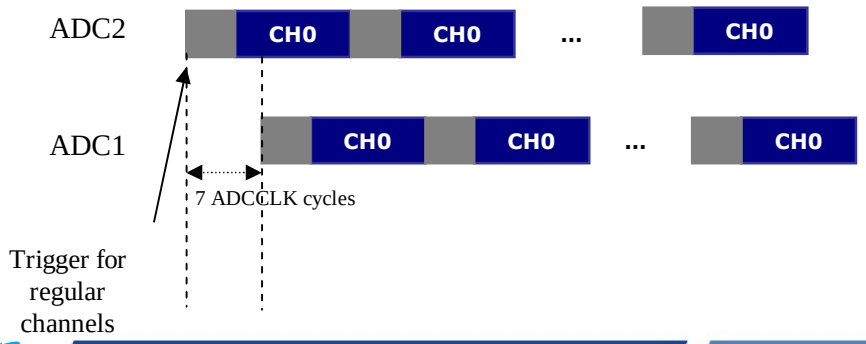


ADC dual modes example (2/2)

Injected simultaneous mode on 4 injected channels



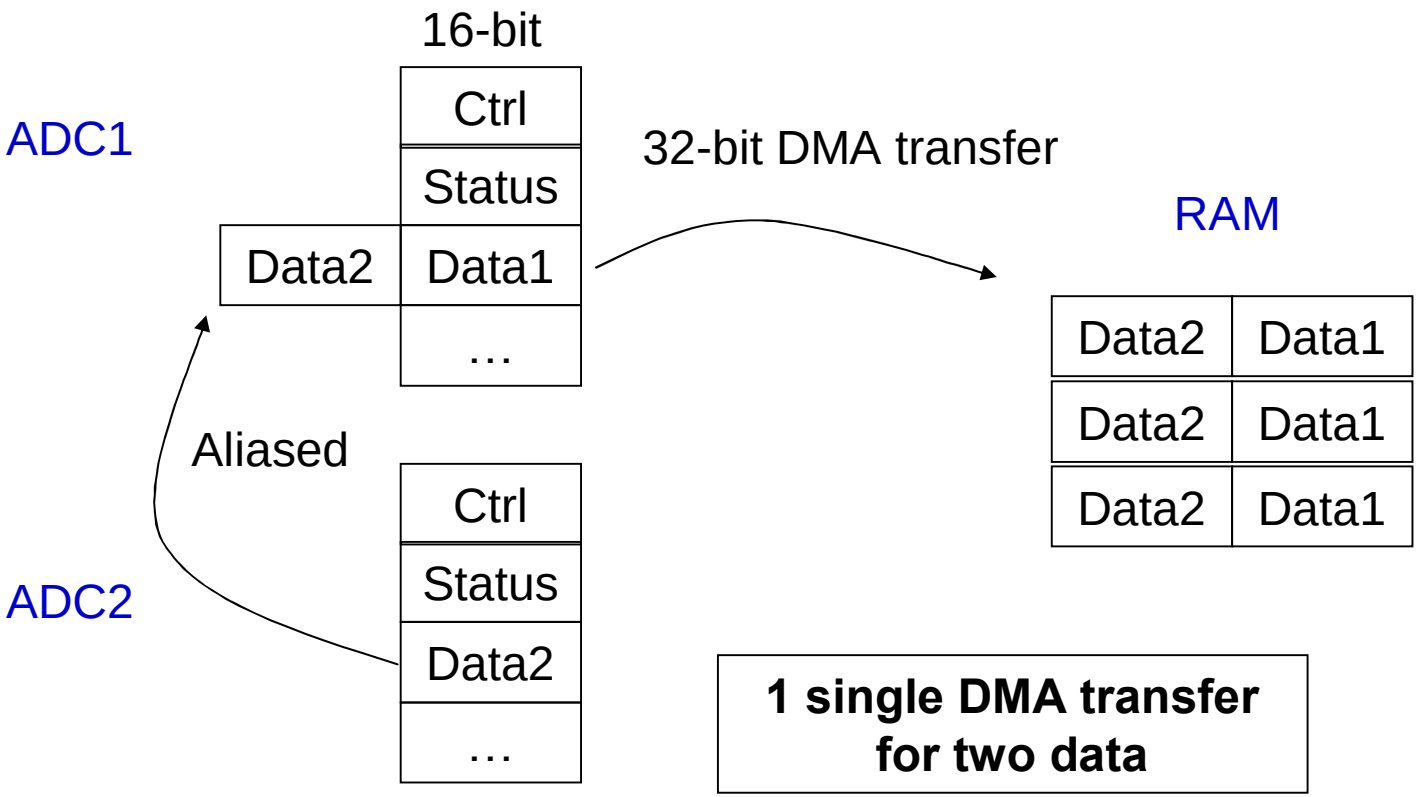
Fast Interleaved mode on 1 regular channel in continuous conversion mode



Up to 2 MSps data throughput (DMA-based)

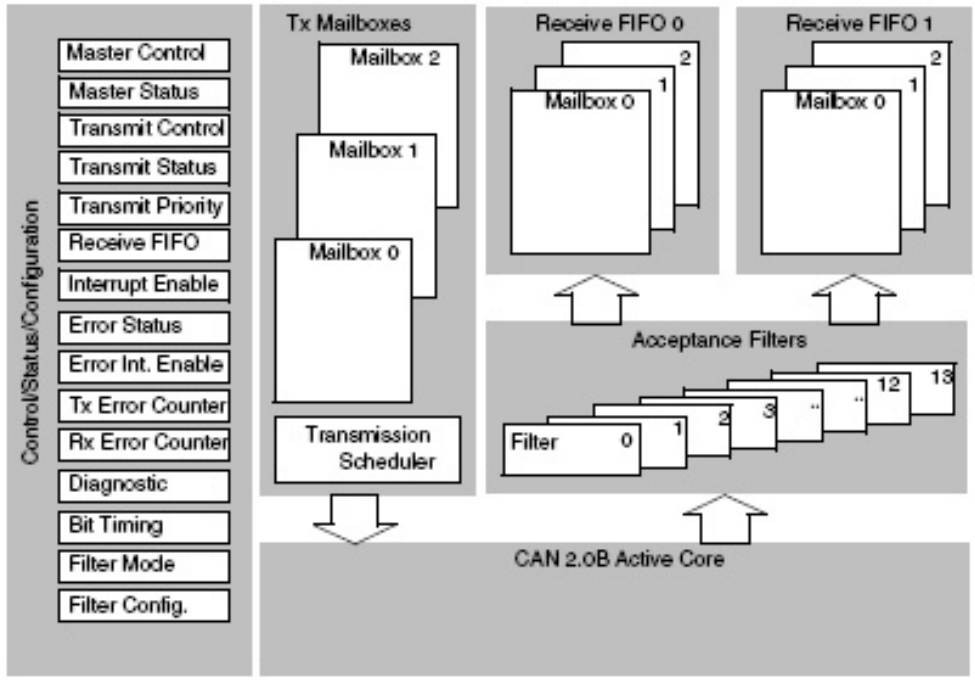
DMA transfers in interleaved mode

- Interleaved mode: continuous conversions of the two ADCs on the same channel with aliased data register

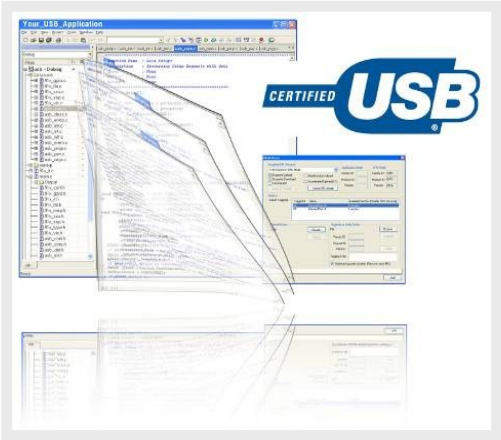


CAN Main Features

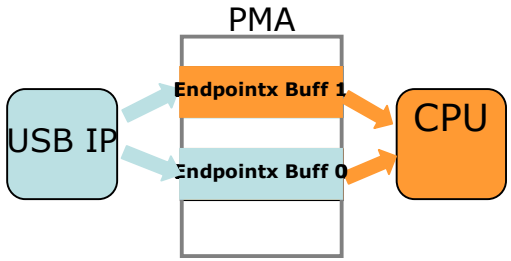
- Main features:
  - Supports CAN protocol version 2.0 A, B Active
  - Bit rates up to 1Mbit/s
  - Support the time Triggered Communication option
  - 512B Reserved RAM buffer
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
  - Time Stamp on SOF transmission
- Reception
  - Two receive FIFOs with three stages
  - 14 scalable filter banks
    - (16 or 32 bit Filter size)
  - Identifier list features
  - Configurable FIFO overrun
  - Time Stamp on SOF reception



USB Main Features



- Fully Certified USB2.0 12Mbps (Full Speed) Device
- Configurable endpoints transfer mode type:
  - control, bulk, interrupt and Isochronous.
- Configurable number of endpoints:
  - up to 8 bidirectional endpoints and 16 mono-directional endpoints.
- USB suspend/resume support.
- Dedicated SRAM Area (**P**acket **M**emory **A**rea) up to 512bytes
  - (shared with bxCAN).
- Dynamic buffer allocation according to the user needs.
- Special double buffer support for Isochronous and Bulk transfers.



Advanced Peripherals of High Density series

Both lines have up to:

- 5 x USART
- 3 x SPI
- 2 x I²C
- 6 x 16-bit Timers
- RTC
- Int 8 MHz RC
  Int 40 kHz RC
- 2xWDG
- POR/PDR/ PVD brown out
- 12 DMA
- 80% GPIO ratio
- Up to 512KB FLASH
- Backup Domain

Access Line

36MHz CPU | Up to 48KB SRAM | EMI* | DAC* | 12b ADC (1µs) Temp sensor

+

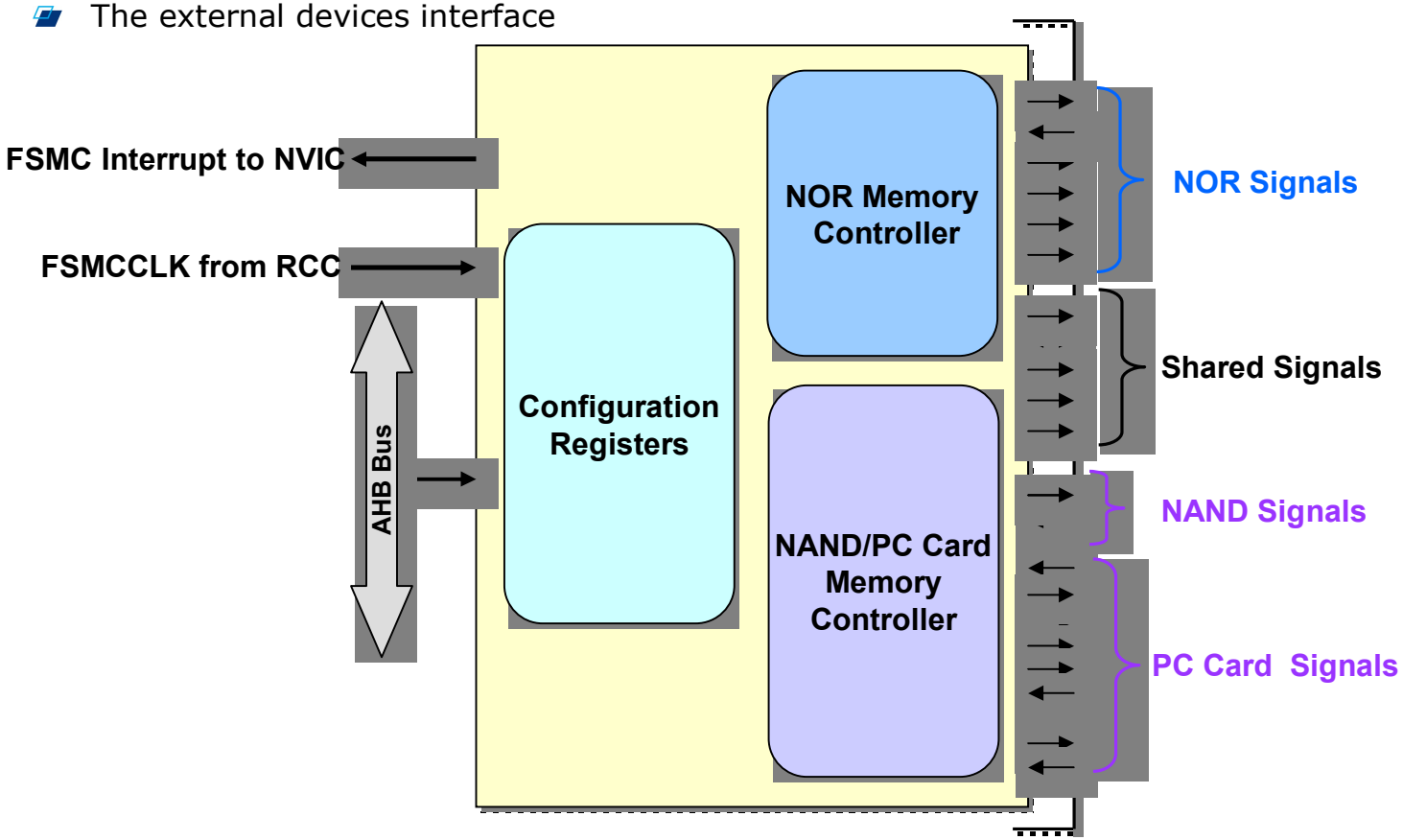
Performance Line

72MHz CPU | Up to 64KB SRAM | EMI* | DAC* | 2x12b ADC 3x12b ADC * (1µs) Temp sensor | USB | CAN | AC Timer (x2)* | I2S* | SDIO*

*** for sales types starting at 256kB Flash**

External Memory Interface: EMI / FSMC

- The FSMC consists of four main blocks:
  - The AHB interface (including the IP configuration registers)
  - The NOR Flash/PSRAM controller
  - The NAND Flash/PC Card controller
  - The external devices interface

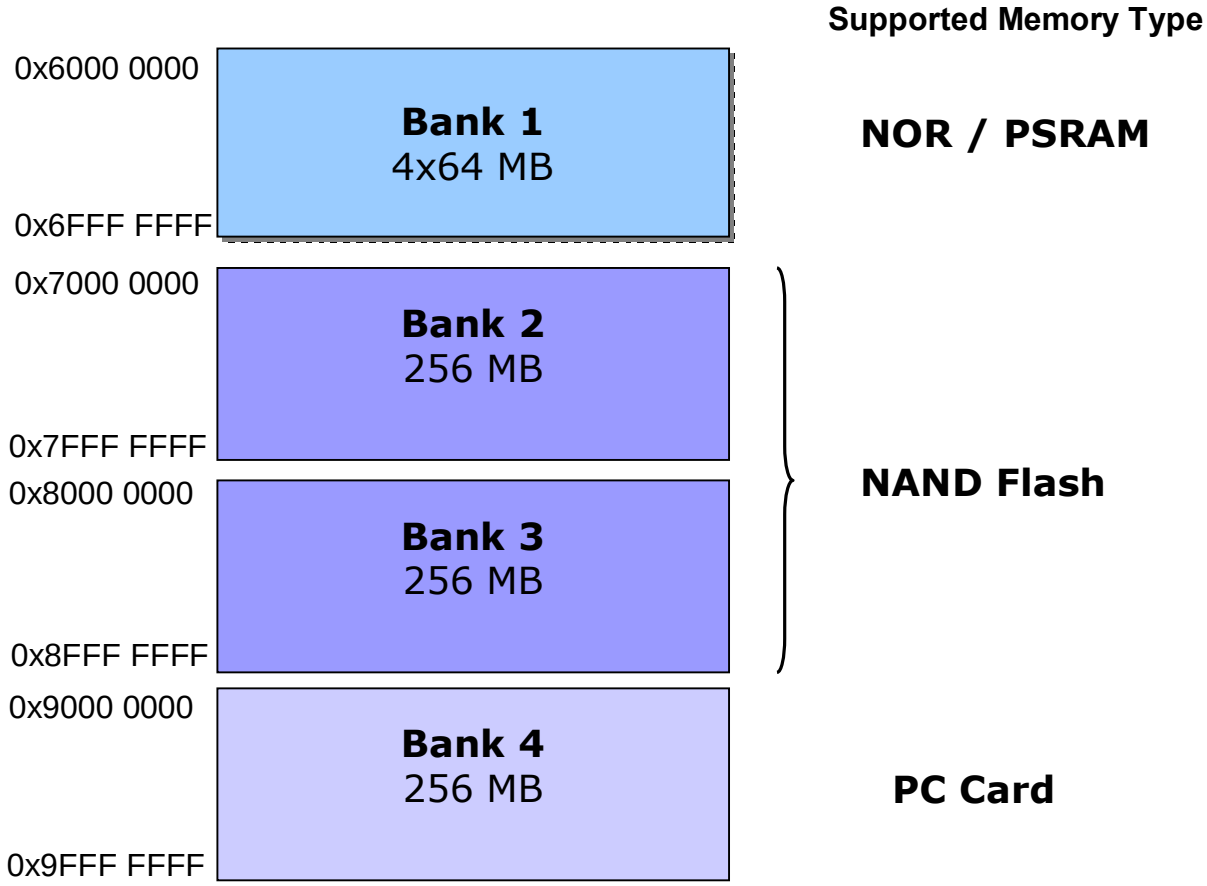


EMI / FSMC Main Features

- The Flexible Static Memory Controller has the following main features:
  - 4 Banks to support External memory
  - FSMC external access frequency is 36MHz when system is at 72MHz
  - Independent chip select control for each memory bank
  - Independent configuration for each memory bank
  - Interfaces with static memory-mapped devices including:
    - static random access memory (SRAM)
    - read-only memory (ROM)
    - NOR Flash memory
    - PSRAM
  - Interfaces with Cellular RAM and COSMO RAM, both synchronous and asynchronous random accesses
  - NAND Flash and 16-bit PC Cards
    - With ECC hardware up to 8 Kbyte for NAND memory
    - 3 possible interrupt sources (Level, Rising edge and falling edge)
  - Programmable timings to support a wide range of devices
  - External asynchronous wait control
  - Code execution from external memory except for PC Cards

EMI / FSMC Bank memory mapping

- For the FSMC, the external memory is divided into 4 fixed size banks of 4x64 MB each:
  - Bank 1 can be used to address NOR Flash or PSRAM memory devices.
  - Banks 2 and 3 can be used to address NAND Flash devices.
  - Bank 4 can be used to address a PC Card device.



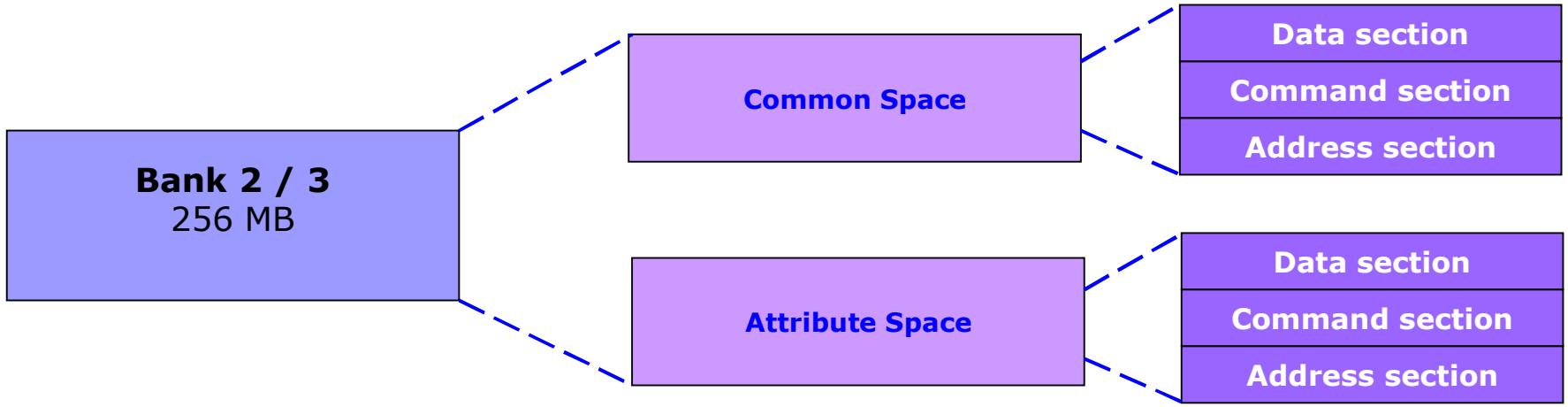
NOR/PSRAM Controller

- The FSMC NOR/PSRAM Controller can control the following features:
  - Memory type:
    - NOR, OneNand, Cram, SRAM, etc…
  - Memory data width:
    - 8 Bit or 16 bit
  - Synchronous or asynchronous Mode
  - Multiplexed or not multiplexed memory
  - Wait feature enable or disable
  - Extended mode: read timings and protocol is different to write.

- The FSMC NOR/PSRAM Controller used also to set the different timings of the memory connected to the bank
  - Address setup phase duration
  - Address-hold phase duration
  - Data-phase duration
  - Bus turnaround phase duration
  - Clock divide ratio
  - Data latency (for synchronous burst NOR Flash)
  - Access mode

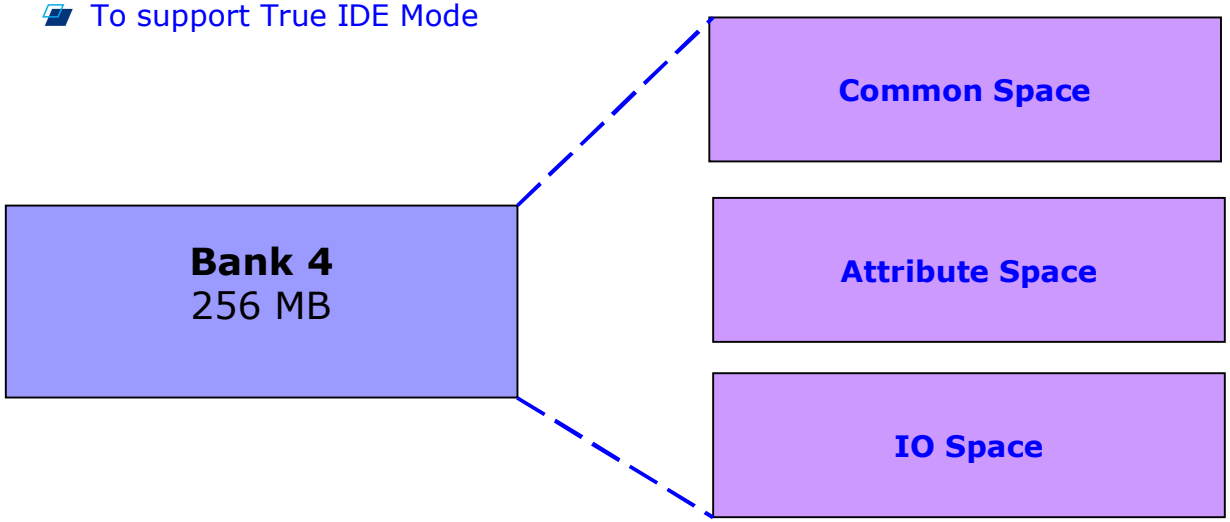
NAND Address mapping

- Bank2 and 3 are used t support the NAND Flash memory
- Bank2 and 3 are divided into two memory space
  - Common memory space
  - Attribute memory space
- Each memory space is divided into 3 subsection:
  - Data section: first 32KB in the common/attribute memory space
    - Used to read or write data
  - Command section: second 32 Kbytes in the common / attribute memory space
    - Used to send a command to NAND Flash memory
  - Address section: next 64 Kbytes in the common / attribute memory space
    - Used to specify the NAND Flash address that must be read or written



PCCARD Address mapping

- Bank4 is used to support the PC CARD Memory
- Bank4 is divided into three memory space
  - Common memory space
    - To support the PC Card Memory Mode
  - Attribute memory space
  - IO memory space
    - To support PC Card I/O Mode
    - To support True IDE Mode

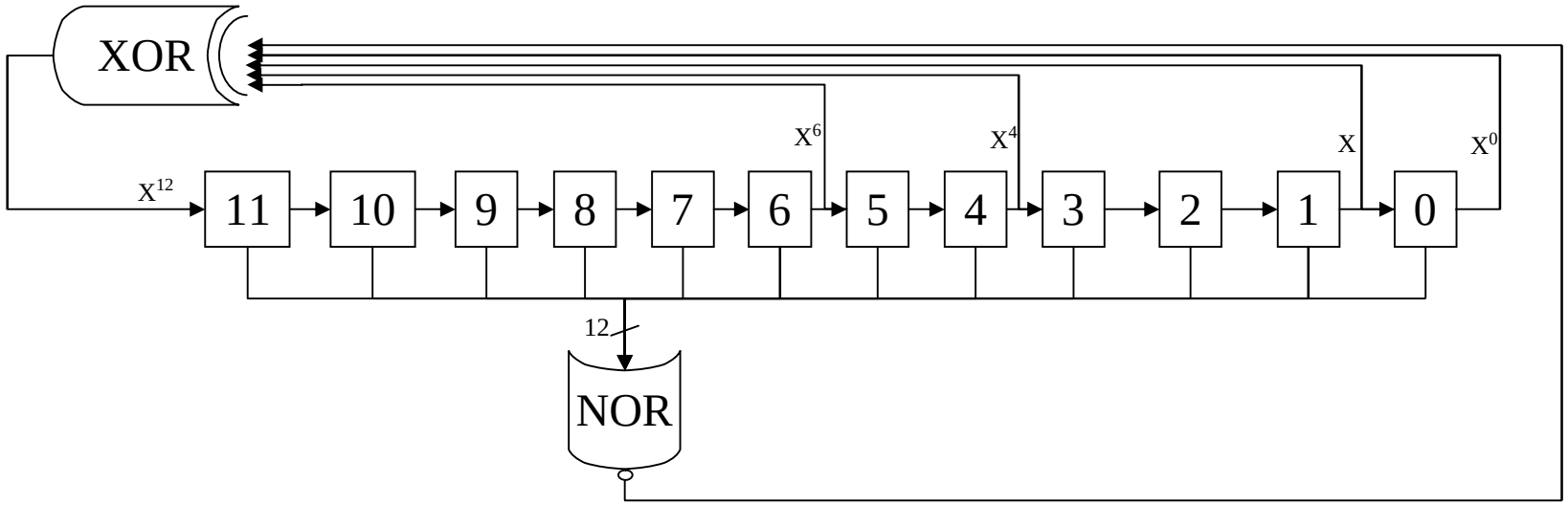


DAC : Main Features

- Two DAC converters: one output channel for each one
- 8-bit or 12-bit monotonic output
- Left or right data alignement in 12-bit mode
- Synchronized update capability
- Noise-wave or Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
  - Request generated when External Trigger occurs
- External triggers for conversion
- DAC supply requirement: 2.4V to 3.6 V
- Conversion range: 0 to 3.6 V
- DAC outputs range: $0 \leq DAC\_OUTx \leq V_{REF+}$ (V_{REF+} and V_{REF-} available only in 100 and 144 pins package)
  - ADC and DAC share the same V_{REF+}

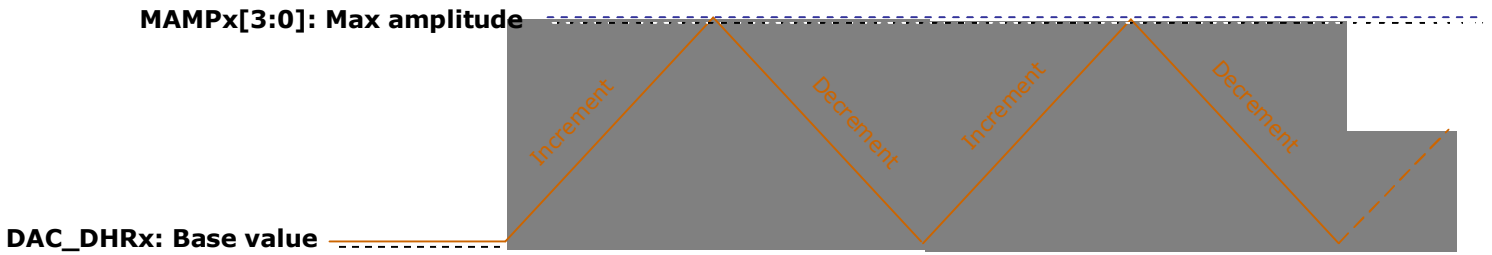
Noise Wave Generation

- Generate a variable amplitude pseudo-noise based on a Linear Feedback Shift Register (LFSR): used in ADC over sampling purposes for example
- Initial Linear Feedback Shift Register value is 0xAAA.
- The LFSR 12bits value can be masked partially or totally
- Anti lock-up mechanism: if LFSR equal to 0 then a 1 is injected on it
- Calculated noise value, updated through external trigger, is added to the DAC_DHRx content without overflow



Triangle Wave Generation

- Add a small-amplitude triangular waveform on a DC or slowly varying signal: used as basic waveform generator for example
- Calculated triangle value, updated through external trigger, is added to the DAC_DHRx content without overflow to reach the configurable max amplitude
- Up-Down triangle counter:
  - Incremented to reach defined max amplitude value
  - Decremented to return to the initial base value
- Triangle max amplitude values are: (2^N-1) with N=[1..12]

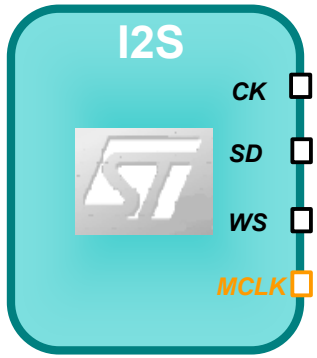


Dual DAC Channel mode

- Both DAC channels can be used together: generate differential or stereo signals in simultaneous conversion mode
- 11 DAC dual modes:
  - Independant trigger, without or with, same or different wave generation (LFSR or Triangle)
  - Simultaneous software start
  - Simultaneous trigger, without or with, same or different wave generation (LFSR or Triangle)

I2S audio protocol

- The I2S protocol is used for audio data communication between a microcontroller/DSP and an audio Codec/DAC.
- The Data are coded according to a specific audio protocol (I2S Phillips/MSB/LSB/PCM) and are time-multiplexed on two channels (Left and Right).
- The protocol uses three/four communication lines:
  - CK : Serial clock
  - SD : Serial data
  - WS : Word Select, control signal
  - MCLK : Master Clock signal (optional)

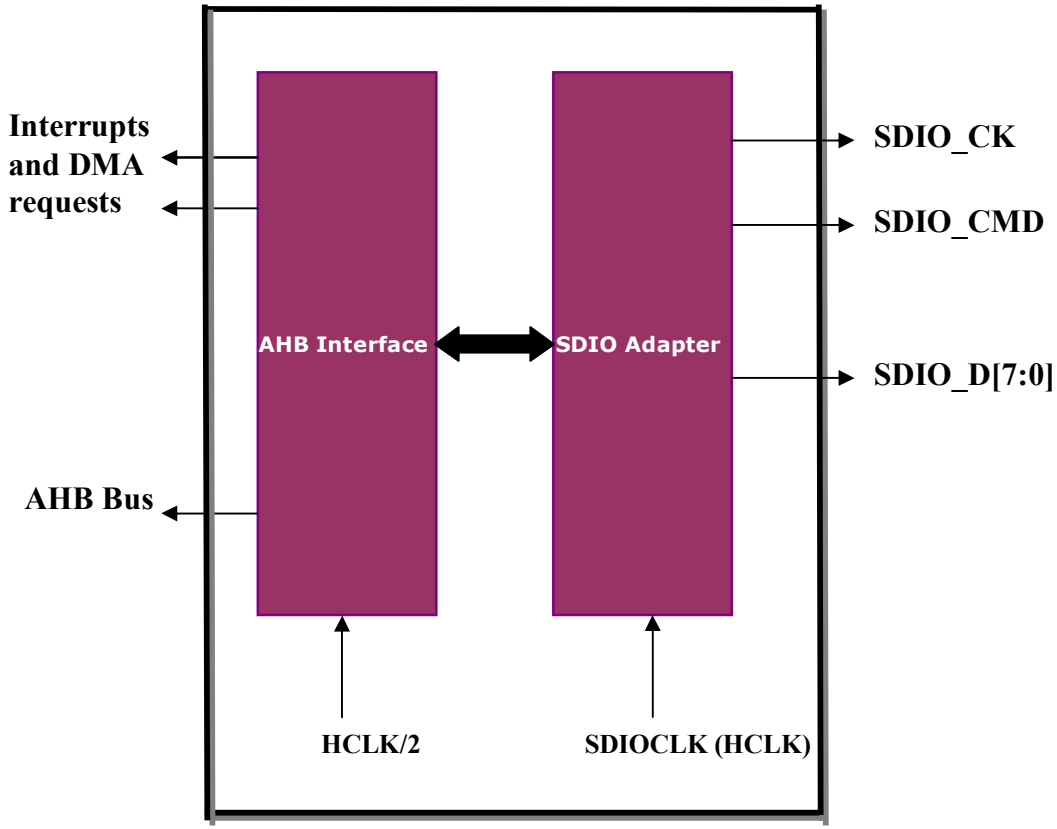


I2S Main Features

- Two I2Ss: Available on SPI2 and SPI3 peripherals.
- Simplex communication (only transmitter or receiver)
- Master or slave operations.
- 8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8KHz to 48KHz)
- Programmable data format (16-, 24- or 32-bit data formats)
- Programmable packet frame (16-bit and 32-bit packet frames).
- Underrun flag in slave transmit mode and Overrun flag in receive mode.
- 16-bit register for transmission and reception.
- I2S protocols supported:
  - I2S Phillips standard.
  - MSB Justified standard (Left Justified).
  - LSB Justified standard (Right Justified).
  - PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)

SDIO : Functional Diagram

- The SDIO consists of two parts:
  - The SDIO adapter block provides all functions specific to the MMC/SD/SD I/O card such as the clock generation unit, command and data transfer.
  - The AHB interface accesses the SDIO adapter registers, and generates interrupt and DMA request signals.



SDIO Main Features (1/2)

- Full compliance with Multimedia Card System Specification Version 4.2. Card support for three different data bus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of Multimedia Cards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0 : card support for two different data bus modes: 1-bit (default) and 4-bit
- Full support of the CE-ATA features (full compliance with CE-ATA digital protocol Rev1.1)
- Data transfer up to 48 MHz for the 8 bit mode

SDIO Main Features (2/2)

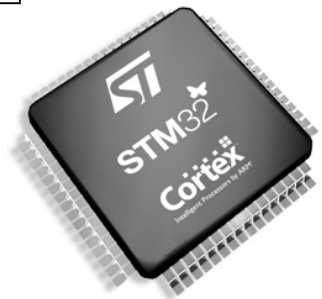
- Cards Clock Management: Rising and Falling edge, 8-bit prescaler, bypass, power save..
- Hardware Flow Control: to avoid FIFO underrun (TX mode) and overrun (RX mode) errors.
- A 32-bit wide, 32-word FIFO for Transmit and Receive
- DMA Transfer Capability
- Data Transfer: Configurable mode (Block or Stream), configurable data block size from1 to 16384 bytes, configurable TimeOut
- 24 interrupt sources to ease software implementation
- CRC Check and generation
- SD I/O mode: SD I/O Interrupt, suspend/resume and Read Wait
- CE-ATA: CE-ATA end of completion command (CMD61), CE-ATA interrupt

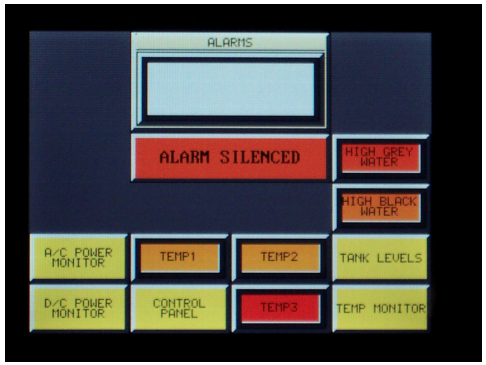
STM32 Peripherals in Action
(Alarm Control Panel)

Serial coms and I/Os
5 Uarts/ 3 SPI/ 2I2C
5 timers, up to 112 I/Os
3 ADC, 21 channels

To phone line, alarm sensors and I/Os

FSMC
Parallel interface to graphic module



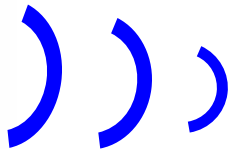


Audio for the user
Voice and music

I2S
Interface to audio DAC for superior audio quality

SDIO
SD card and SD modules

SD card for software upgrade



Wi-Fi to home network

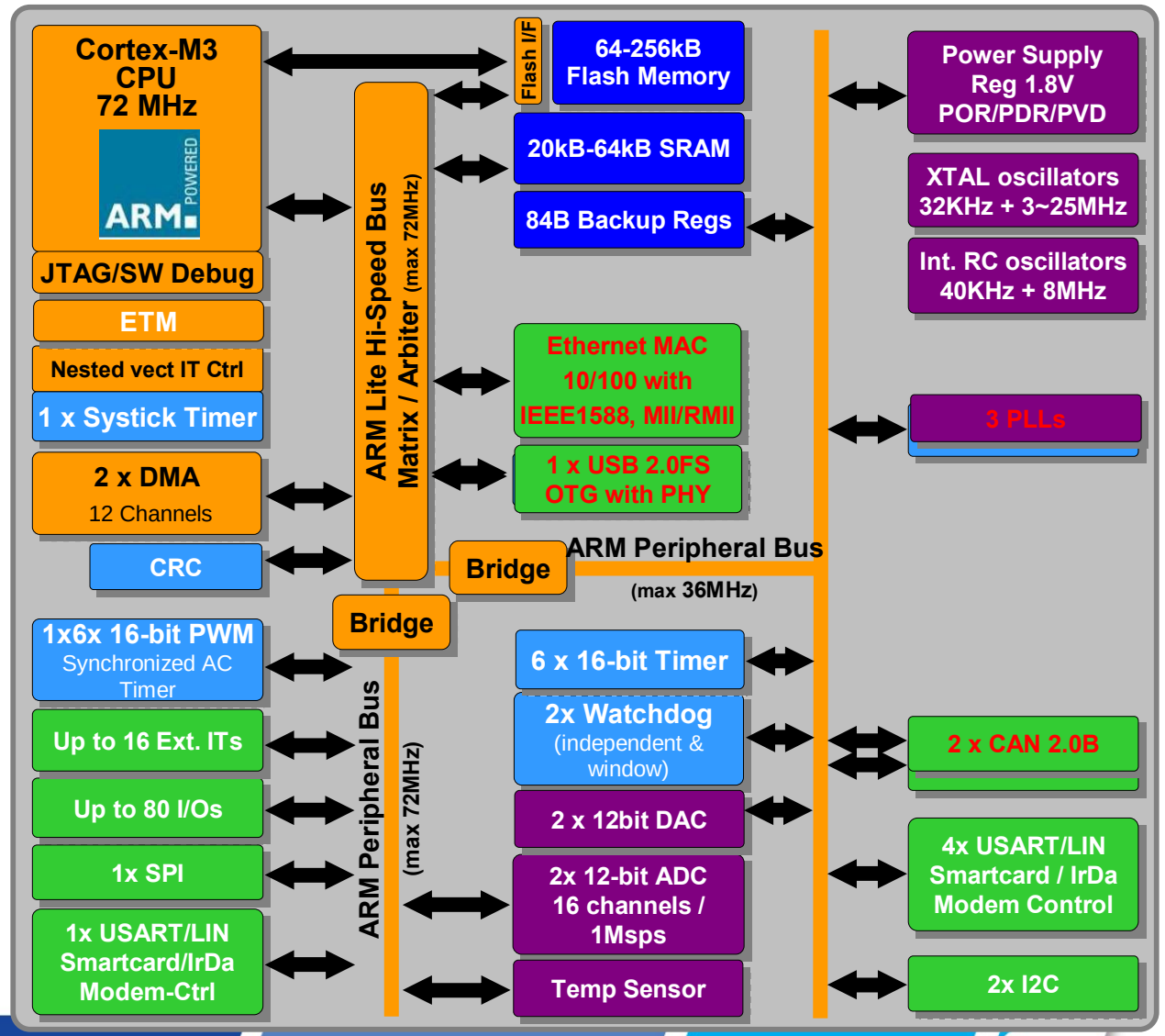
STM32F105/7 Connectivity Line

Fully compatible with the STM32 platform

- Pin-to-pin and function compatible with the current STM32 family for easy migration

Outstanding new features

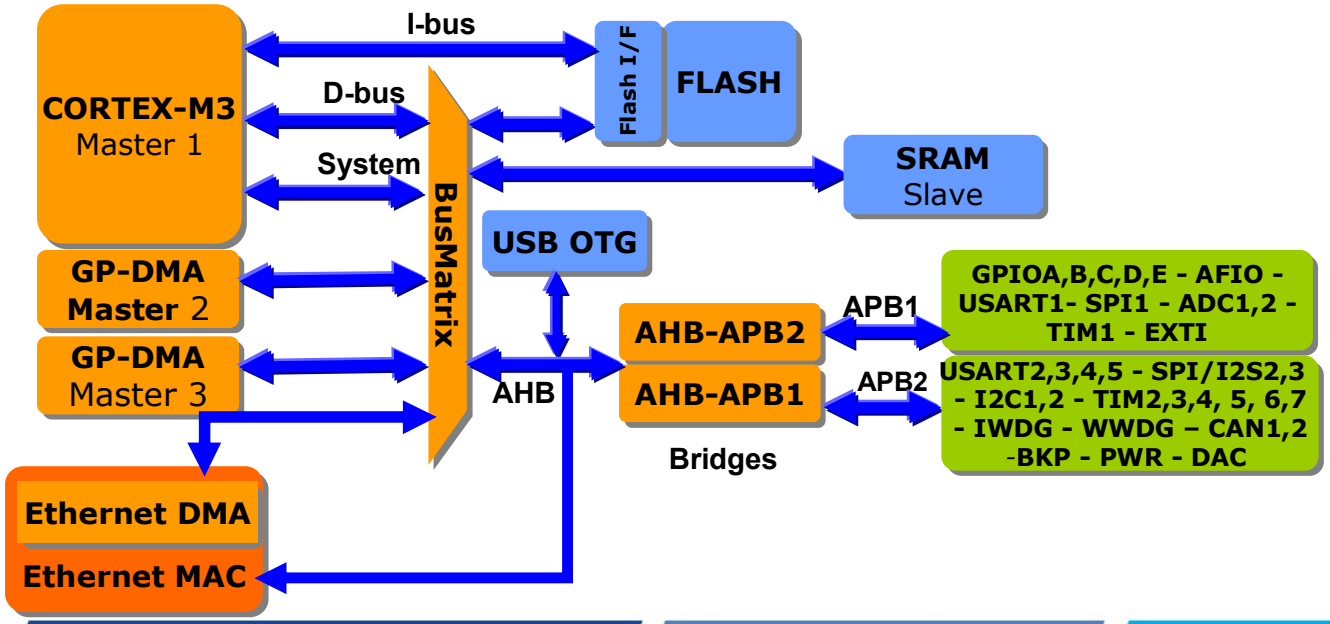
- Ethernet MAC 10/100
  - IEEE1588 v1.0 (PTP) HW support
  - PHY interface: MII and RMII both supported on all packages
- USB 2.0 OTG Full Speed (12Mbps) controller with embedded OTG PHY
- Audio class I2S via advanced PLL schemes, supporting audio sampling frequencies from 8kHz up to 96kHz with less 0.5% accuracy on the I2S Master Clock
- Dual CAN 2.0B Active capable to work simultaneously with USB OTG
- LQFP64, LQFP100, LFBGA100



System Architecture

- **Multiply possibilities of bus accesses to SRAM, Flash, Peripherals, DMA**
  - Bus Matrix added to Harvard architecture allows parallel access
- **Efficient DMA and Rapid data flow**
  - Direct path to SRAM through arbiter, guarantees alternating access
  - Harvard architecture + Bus Matrix allows Flash execution in parallel with DMA transfer
- **Increase Peripherals Speed for better performance**
  - Dual Advanced Peripheral buses (APB) architecture w/ High Speed APB (APB2) up to 72MHz and Low Speed APB (APB1) up to 36MHz

  ➔ Allows to optimize use of peripherals (18MHz SPI, 4.5Mbps USART, 72MHz PWM Timer, 18MHz toggling I/Os)



Enhanced Clock Scheme: Overview

- Connectivity Line implements an enhanced clock scheme w/ 3 PLLs and multiple selection of clock output sources (MCO pin)
  - Up to 8 clock signals can be output onto the external MCO pin (PA.08).
    - SYSCLK
    - HSI
    - HSE
    - PLL clock divided by 2 selected
    - PLL2 clock selected
    - PLL3 clock divided by 2 selected
    - XT1 external 3-25 MHz oscillator clock selected (for Ethernet)
    - PLL3 clock selected (for Ethernet)
  - With single *25MHz crystal* you can have at the same time
    - System clock up to 72MHz
    - 48MHz for USB OTG
    - 25/50MHz for external Ethernet PHY
  - With *14.7456MHz audio crystal* you can have at the same time
    - System clock up to 71.88MHz
    - Best in class I2S master clock capable to generate all standard sampling frequencies from 8 kHz to 96 kHz with less than 0.5% accuracy
    - Functional USB OTG (47.9232MHz input clock w/ 0.16% accuracy)

Enhanced Clock Scheme: PLLs Configuration

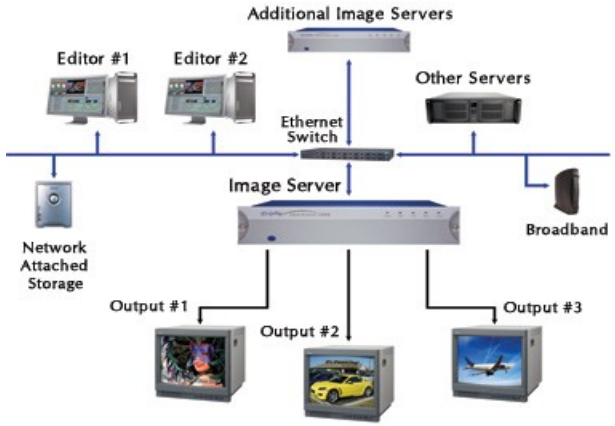
PLL Configuration Table is available in STM32F105/107 Datasheet:

“Appendix A Applicative block diagrams”

Application	Crystal Value (XT1)	PREDIV2	PLL2MUL	PLLSRC	PREDIV1	PLLMUL	USB Prescaler (PLL VCO output)	PLL3MUL	I2Sn Clock Input	MCO (Main Clock Output)
Ethernet Only	25MHz	/5	PLL2ON x8	PLL2	/5	PLLON x9	Don’t care	PLL3ON x10	Don’t care	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25MHz	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	Don’t care	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Basic Audio	25MHz	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	PLL	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + High Quality Audio *	14.7456 MHz	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3	Don’t care. ETH PHY must use its own crystal
OTG Only	8MHz	Don’t care	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	Don’t care	Don’t care
OTG + Basic Audio	8MHz	Don’t care	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	PLL	Don’t care
OTG + High Quality Audio *	14.7456 MHz	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3	Don’t care.
High Quality Audio Only *	14.7456 MHz	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	Don’t care	PLL3ON x20	PLL3	Don’t care.

* The SYSCLK is 72MHz except in this case SYSCLK will be at 71.88MHz

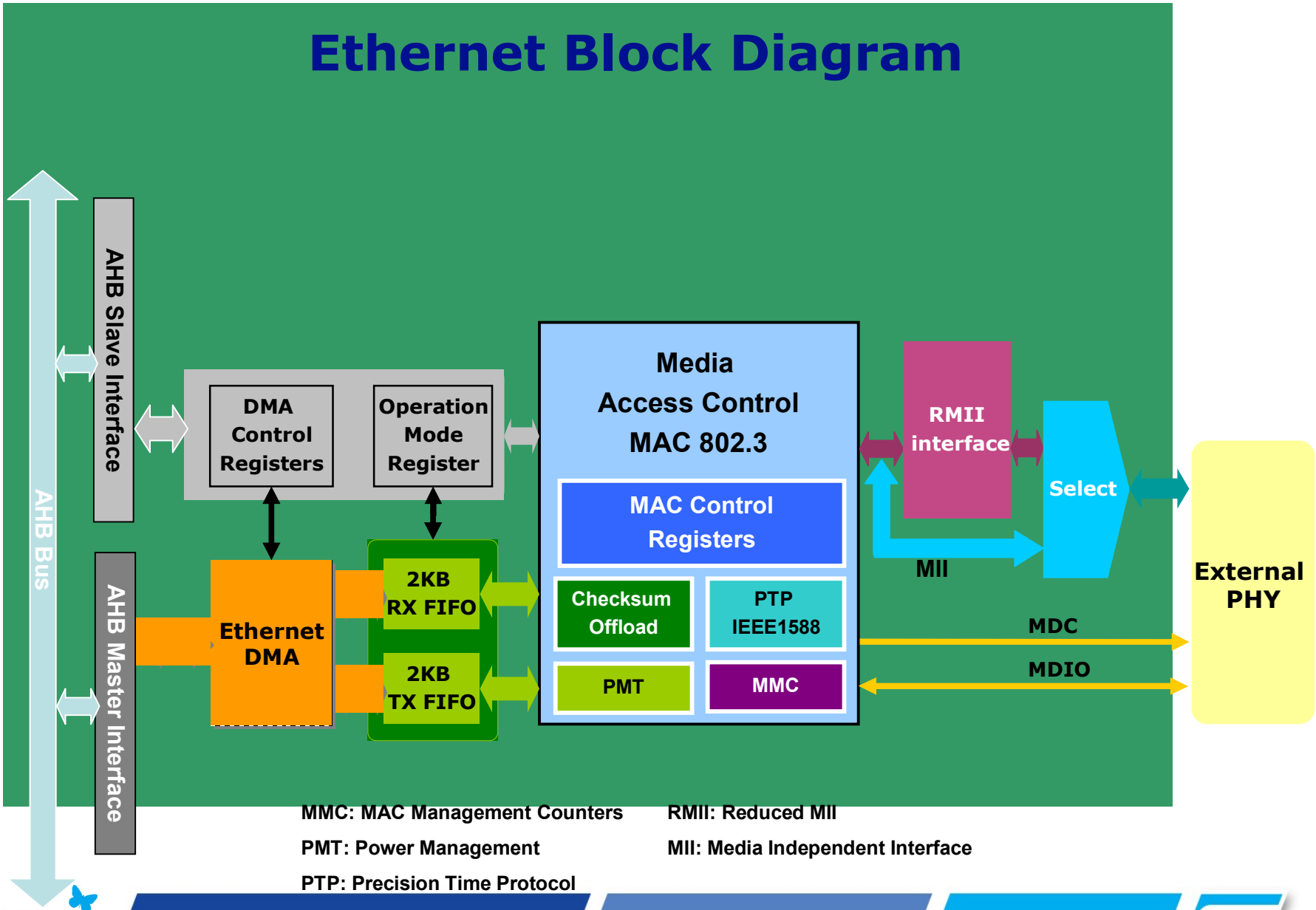
Ethernet MAC 10/100



STM32F107 Ethernet Interface Overview

- Supports 10/100Mbits, Half/Full-duplex operations modes, with external PHY interface.
- Dedicated DMA controller with two sets of FIFOs.
- Supports Ethernet frame time stamping.
- Supports Power-down mode.
- Two interrupt vectors:
  - Ethernet normal operations.
  - Ethernet wakeup event.
- Compliant with the following standards:
  - IEEE 802.3-2002 for Ethernet MAC
  - IEEE 1588-2002 standard for precision networked clock synchron
  - RMII specification from RMII consortium

Ethernet Block Diagram



MMC: MAC Management Counters

PMT: Power Management

PTP: Precision Time Protocol

RMII: Reduced MII

MII: Media Independent Interface

Media Access Controller: MAC Features

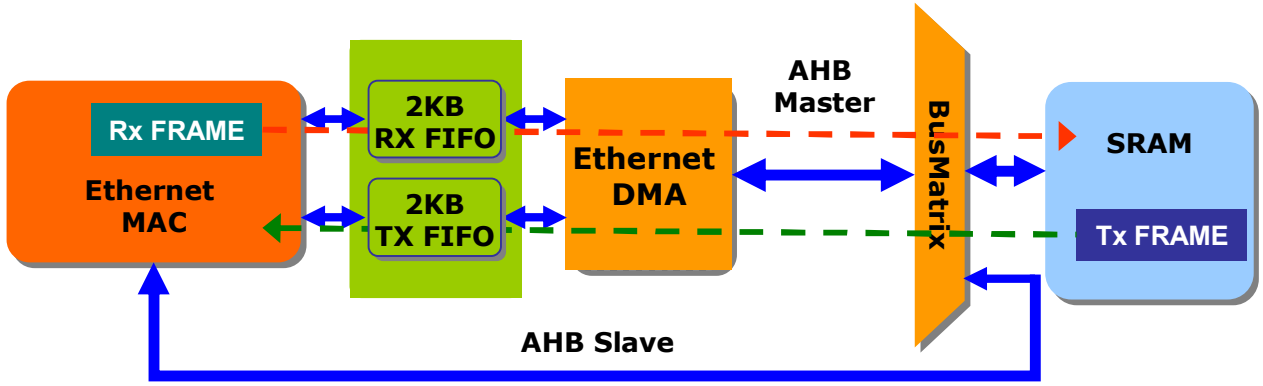
- 10/100 Mbit/s transfer rates and Full/Half-duplex operation modes.
- Programmable frame length with size up to 16 KB.
- IEEE 802.1Q VLAN tag detection for reception frames.
- Checksum offload engine for transmit and receive of TCP/IP frames.
- Network statistics with RMON/MIB counters (RFC2819/RFC2665).
- Flexible address filtering modes.
- Power-down mode with Ethernet wakeup event.
- IEEE1588 Ethernet frame time stamping.
- Internal loopback on the MII for debugging.

MAC Filtering

- The Ethernet controller can have up to 4 MAC address:
  - One default address: MACAddr0, always enabled.
  - Three optional address: MACAddr1, MACAddr2 and MACAddr3.
- The three optional address can be:
  - Enabled or disabled.
  - Used as Source or Destination address for Unicast filtering.
- MAC address filtering can be based on the MAC address or the Hash table.
- The MAC filtering block allows to:
  - Accept or reject Multicast and Broadcast frames.
  - Accept all incoming frames, *useful for network monitoring*.
  - Inverse filtering capability for both destination and source addresses.
  - Use Hash Table to filter Multicast and Unicast destination addresses.
- Hash filtering is supported

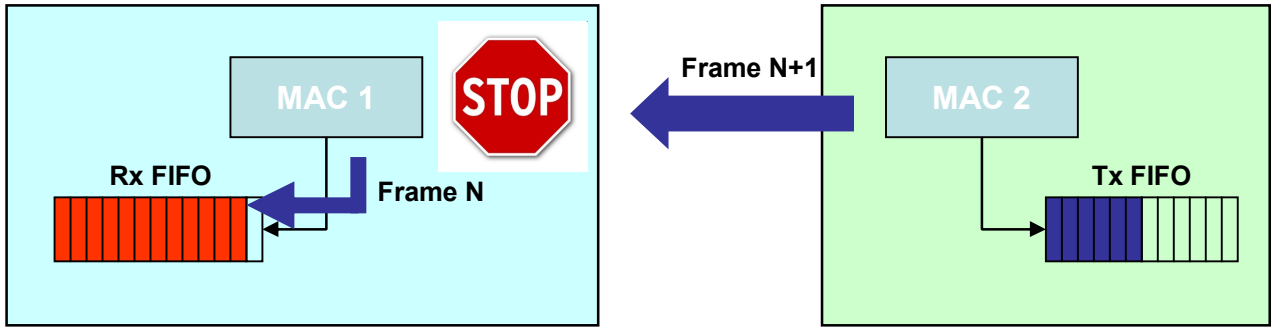
MAC FIFOs

- The MAC core has two sets of FIFOs, of 2KB each one, with a configurable threshold.
- Two modes for popping data towards the MAC, for frames transmission:
  - Threshold mode: as soon as the threshold level is reached.
  - Store-and-Forward mode: a complete frame is stored into the FIFO.
- Two modes for popping data towards the DMA, for frames reception:
  - Cut-through mode: as soon as the threshold level is reached.
  - Store-and-Forward mode: a complete frame is received into the FIFO.



Flow Control

- Ethernet Flow Control consists on stopping temporarily data transmission.
- STM32F107 MAC supports Flow Control for Half/Full-duplex modes and can be:
  - Started automatically when the RX FIFO is Full.
  - Started by the Application.
- The Half-duplex Flow Control is provided by the Back Pressure mechanism.
- The Full-duplex Flow Control is provided by the Pause Frame mechanism:
  - Pause Frame is sent with multicast destination address 01-80-C2-00-00-01.
  - Pause Time is a 16bit multiple of 512 Bit-Time.



Checksum Offload

- The Ethernet MAC implements checksum offload feature for IPv4, ICMP, TCP and UDP protocols.
- Checksum offload engine supports:
  - Checksum calculation and insertion for the transmit path.
  - Error detection for the receive path.
- Checksum offload feature can be enabled only with Store-and-Forward mode.
- The following special frames are bypassed by the checksum engine:
  - Fragmented IP.
  - IP frames with security features.
  - IPv6 with routing headers.

Power Management Block

- Power Management mechanism allows:
  - Setting the Ethernet controller in power down mode.
  - Receive wakeup frames and Magic Packet frames.
  - Generate external event, on the line 19, to wakeup the system from the STOP mode.
- Remote wakeup frames are identified using 4 filters.
- Interrupt and wakeup event generation for wakeup frames and Magic Packets received by the MAC.
- Ethernet wakeup event is connected to the EXTI_Line19 and can be used to exit the system from the STOP mode.

Ethernet Dedicated DMA Controller

- Independent DMA engines for transmit and receive.
- Round-robin or fixed-priority arbitration between transmit and receive engines.
- Byte-aligned addressing for data buffer support.
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 8 KB of data.
- Dual-buffer (ring) or linked-list (chained) descriptor chaining.
- Comprehensive status reporting for normal operation and transfers with errors.
- Programmable burst size for transmit and receive.
- Interrupt control for transmit and receive.

IEEE 1588 Precision Time Protocol

- PTP applies to local area networks supporting multicast messaging and aims to synchronize heterogeneous systems clocks with minimum network and local computing resources.

- The target accuracy of PTP IEEE1588-2002 V1 is the sub-microsecond range.

- IEEE1588 V2 improvements:
  - Sub-nanosecond accuracy.
  - Faster synchronization (SYNC) message rates.
  - Shorter PTP messages, unicast messaging, new messages (path delay request/response/response follow-up) and message fields:
  - Transparent Clocks.
  - Fault Tolerance.

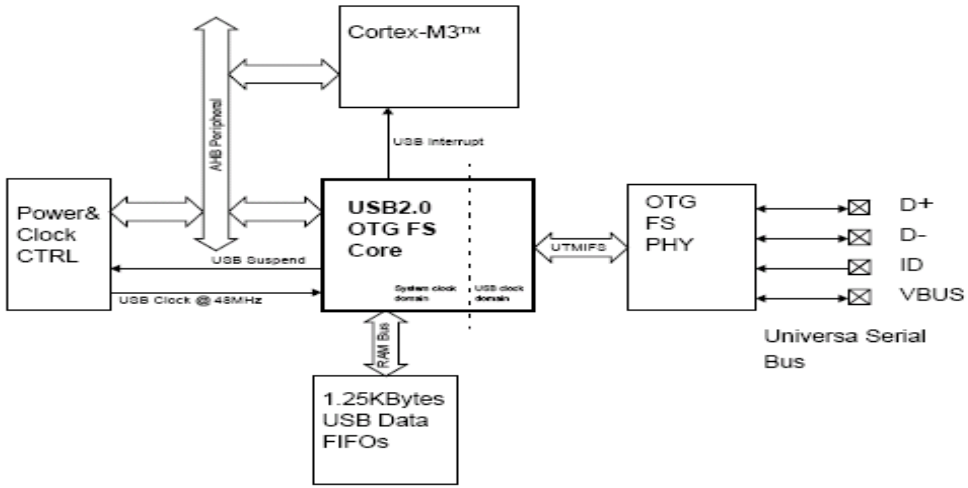
Precision Time Protocol: PTP Feature

- Ethernet frame time stamping as described in IEEE V1, for both receive and transmit.
  - PTP V2 can by implemented by firmware over the V1 hardware.
- 64bit PTP clock split into two 32bit counters:
  - 32bit second counter.
  - 32bit nanoseconds counter.
- PTP trigger generation when system time becomes greater than a pre-defined target time.
- PTP trigger is internally connected to the TIM2 ITR1 input.
- Pulse per-second output generation to check the synchronization between all nodes in the PTP network.

USB 2.0 On-The-Go Full Speed (OTG FS)

USB OTG FS core features 1/2

- **Main features**
  - Complies with the On-The-Go Supplement to the USB 2.0 Specification (Rev 1.3)
  - Operates in Full-Speed and Low Speed (FS, 12-Mbps, LS 1.5 Mbps) mode.
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
  - Operate in Host, device and OTG modes.



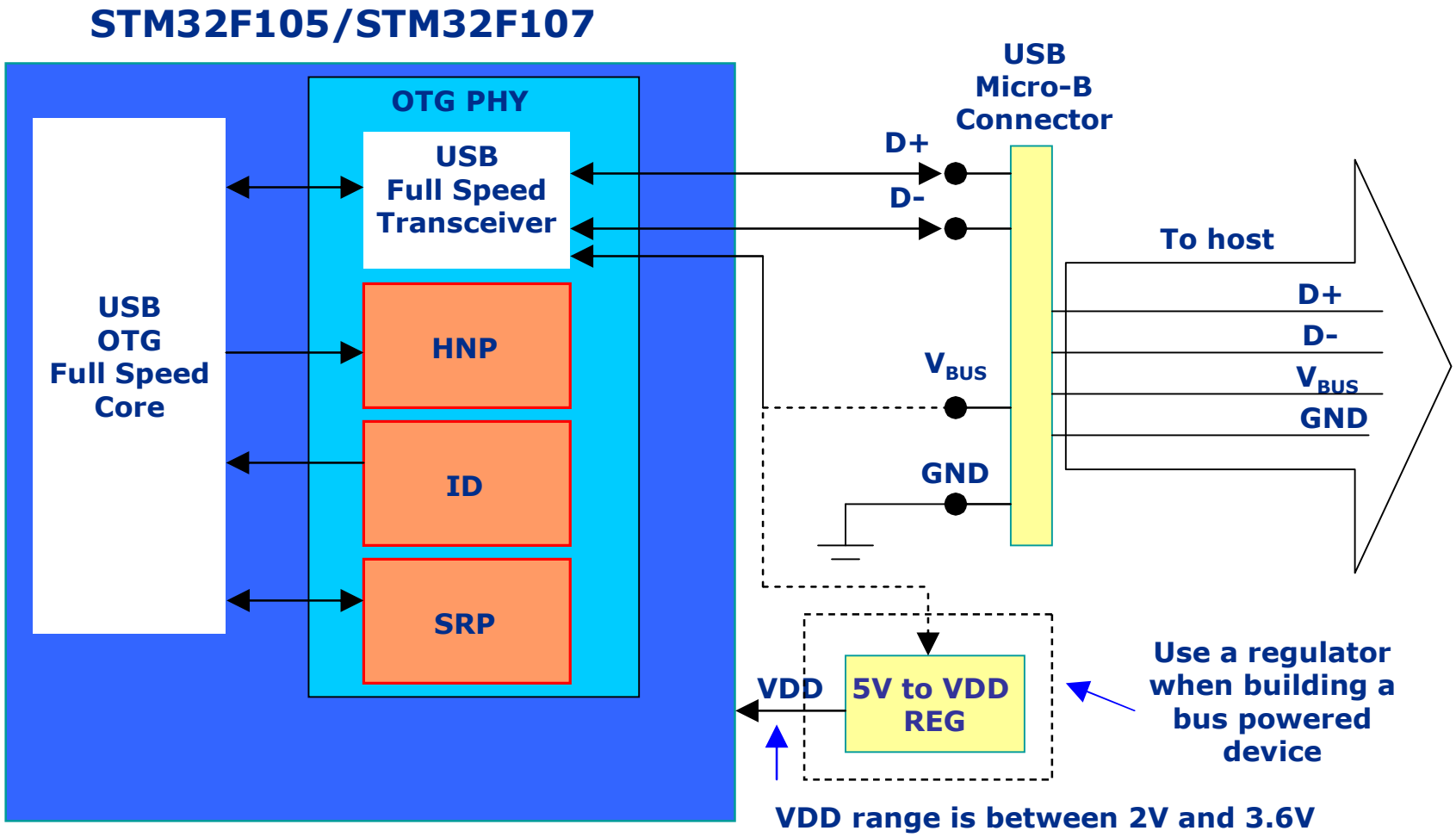
USB OTG FS core features 2/2

Characteristics

- 4 bidirectional endpoints, including:
- 1 control endpoint 0 and 3 device endpoints which support bulk interrupt, isochronous.
- 8 host channels with periodic OUT support.
- Dedicated transmit FIFO for each of the 4 device IN endpoints. Each FIFO can hold multiple packets.
- Combined Rx and Tx FIFO size of 320 x 35bit with Dynamic FIFO sizing (1.25 KB).
- 8 entries in periodic Tx queue, 8 entries in non periodic Tx queue.
- Controls OTG FS PHY on-chip for Host, Device or OTG operation
- Requires an external Charge pump for VBUS Voltage.
- 32-bit AHB Slave interface for accessing Control and Status Registers (CSRs), Data FIFO.
- Provides a trigger interrupt in each SOF, connected to Timer 2.

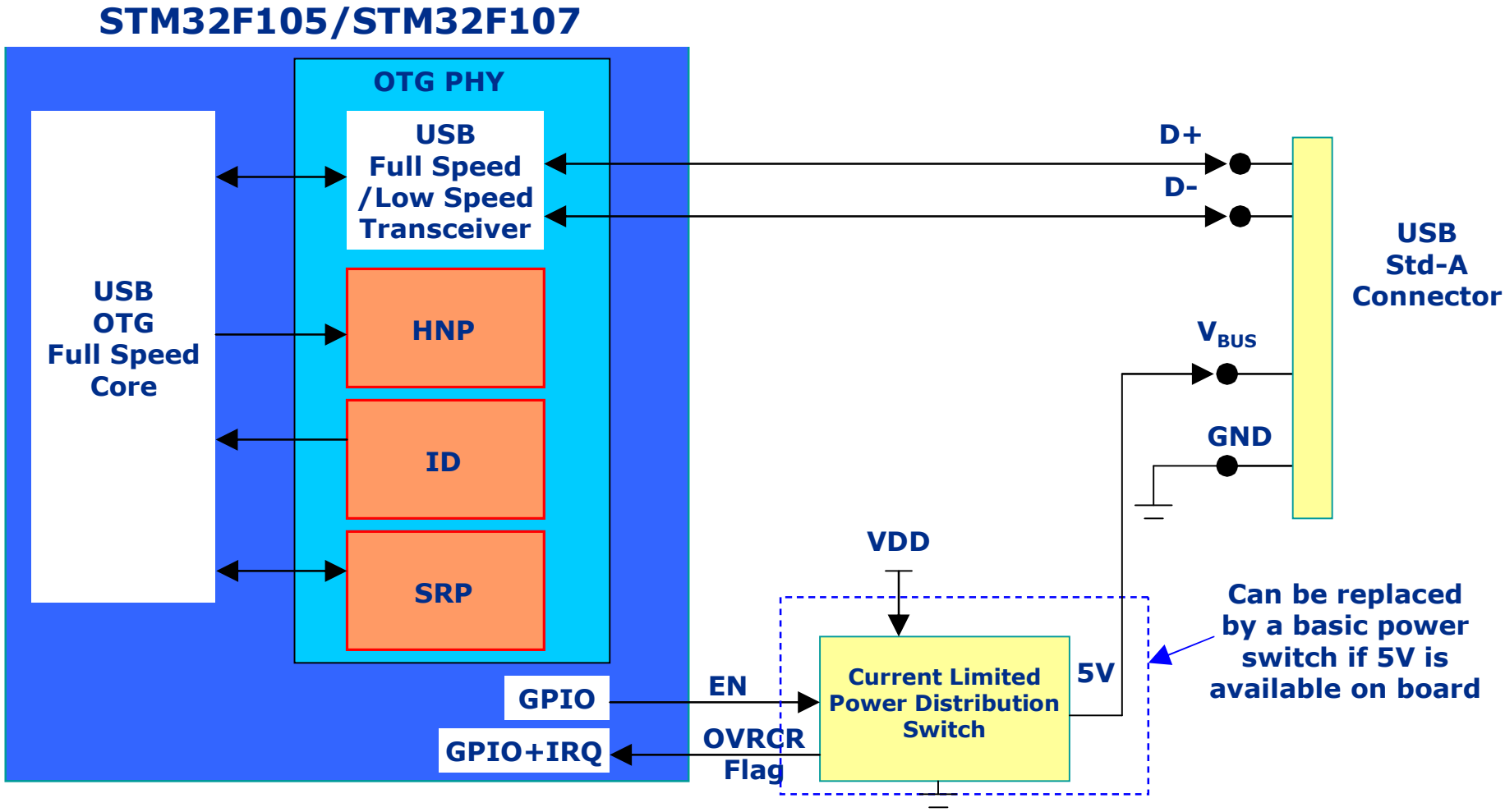
USB interface solution (1/3)

STM32: USB device mode



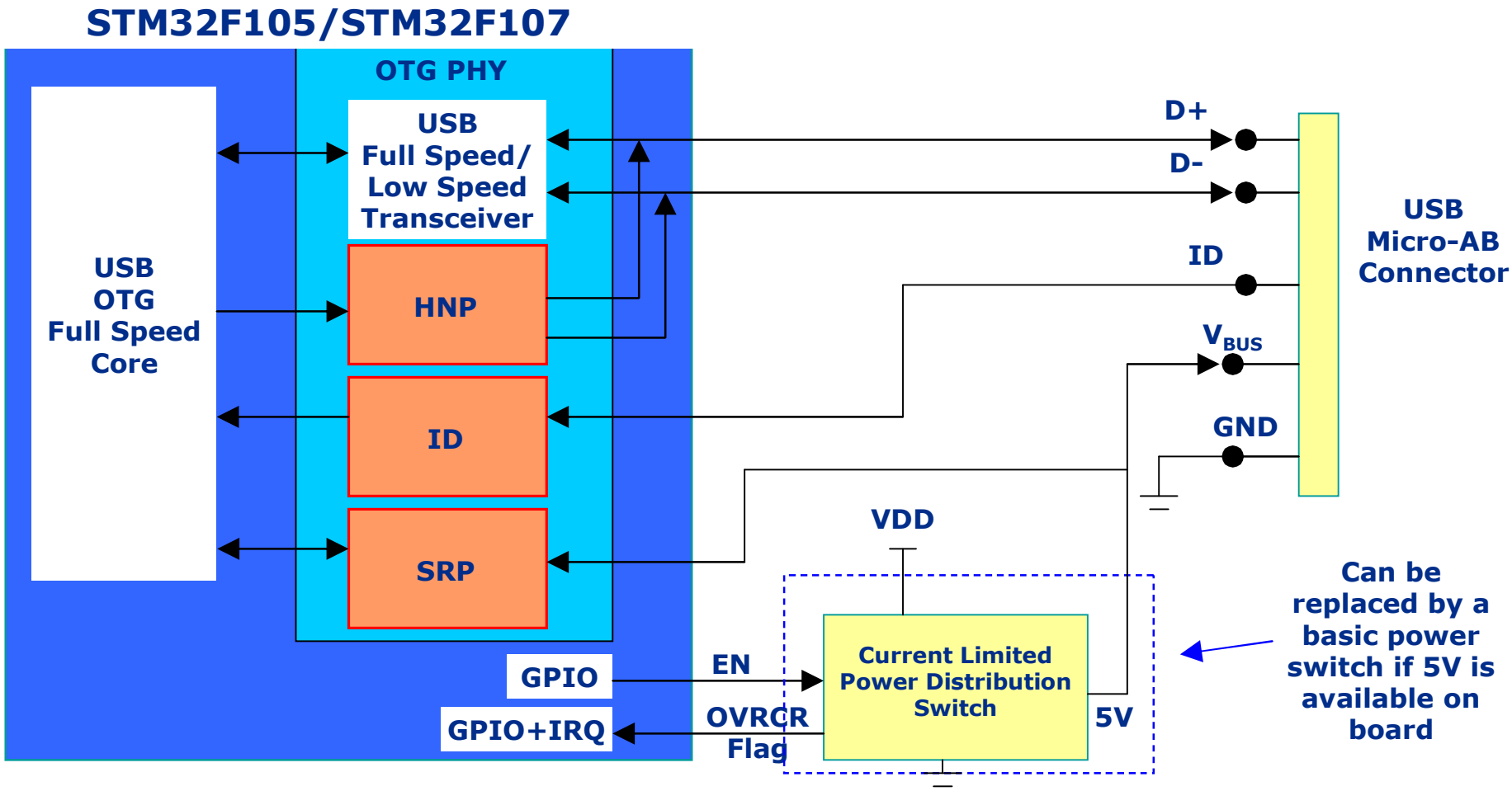
USB interface solution (2/3)

Host connection

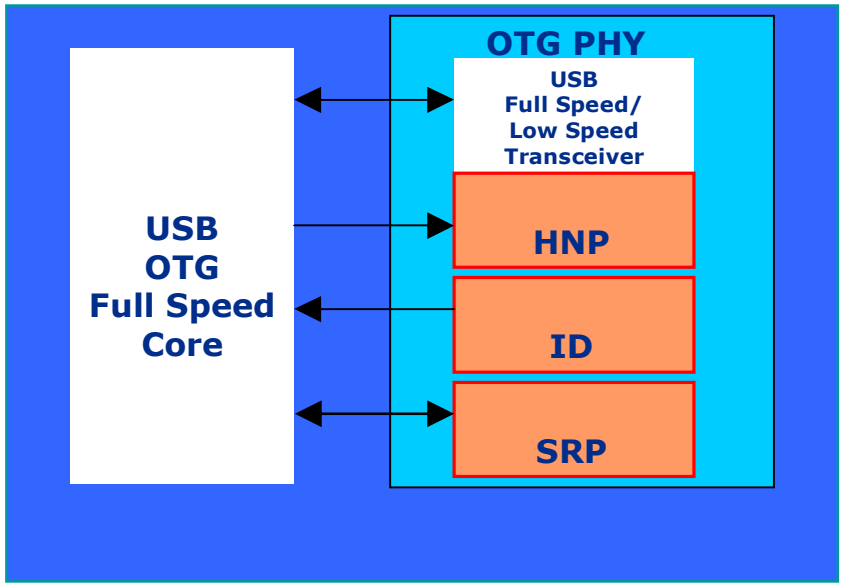


USB interface solution (3/3)

OTG connection



OTG features



Session Request Protocol (SRP)

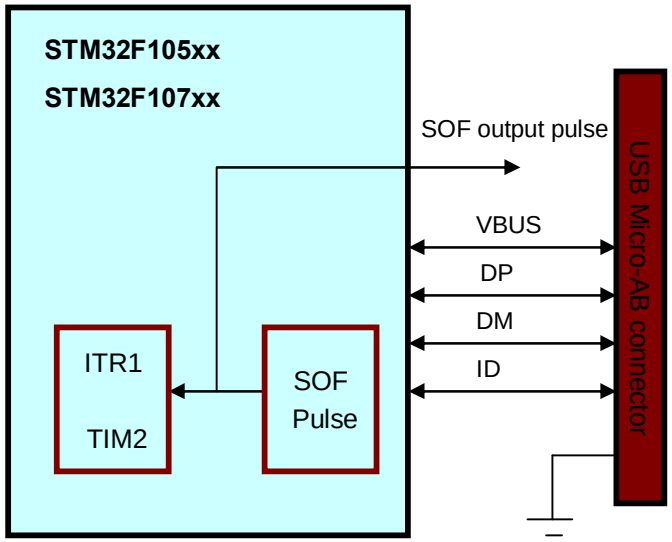
- Allows B-device to request VBUS be turned on
- SRP is not supported through hubs

Host Negotiation Protocol (HNP)

- Allows the B-device to communicate to the A-device as a host avoiding unplugging and turning the cable around.
- HNP is not supported through hubs

SOF Trigger Feature

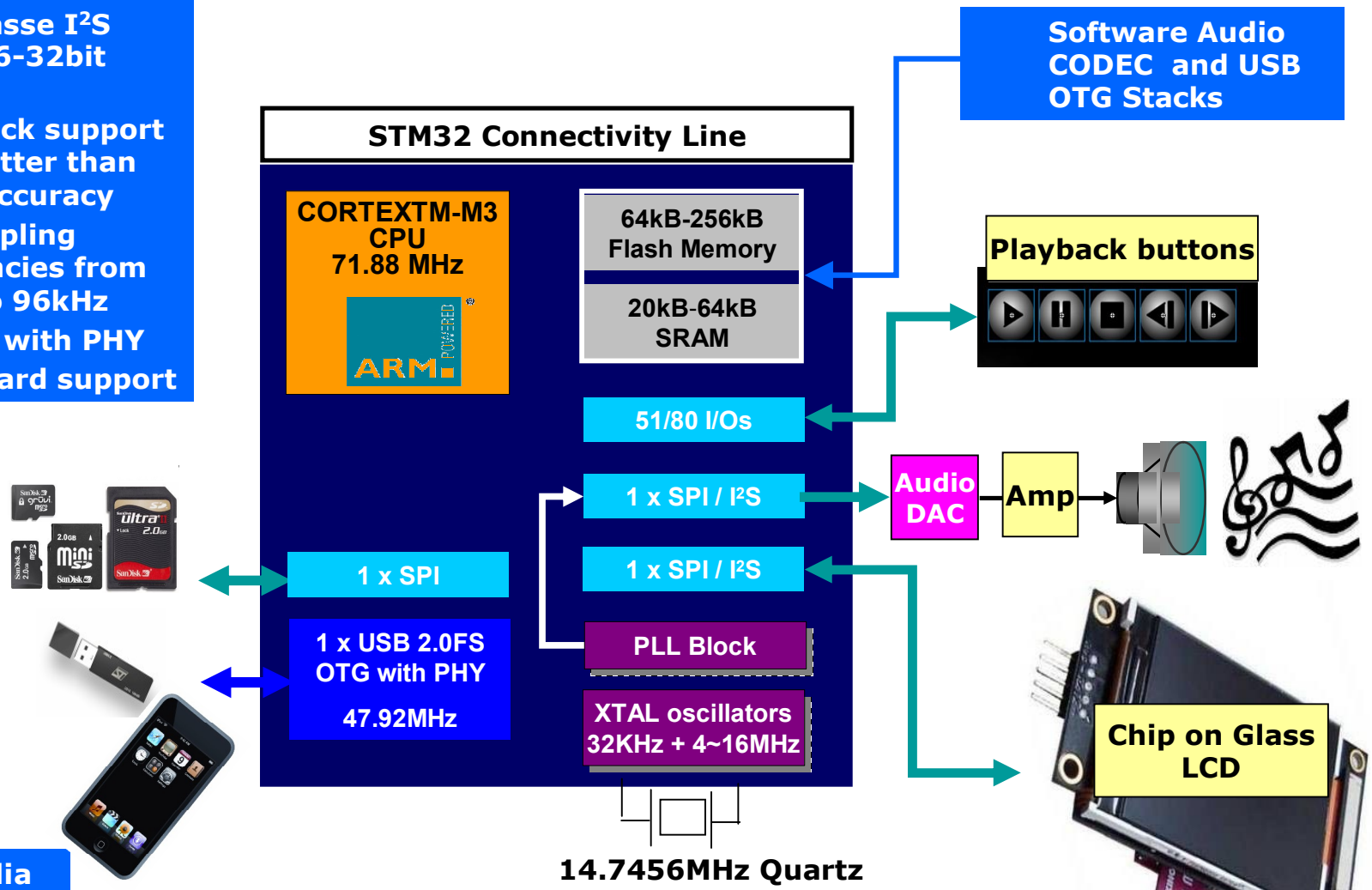
- The SOF is generated every 1 ms.
- The trigger can be used to synchronize an external device with the USB clock.
- Internally connected to the timer 2 (TIM2) input trigger.
- the input capture feature, the output compare feature are triggered by the SOF signal.
- The connection is enabled through bit 29 in the REMAP_DBGAFR register.



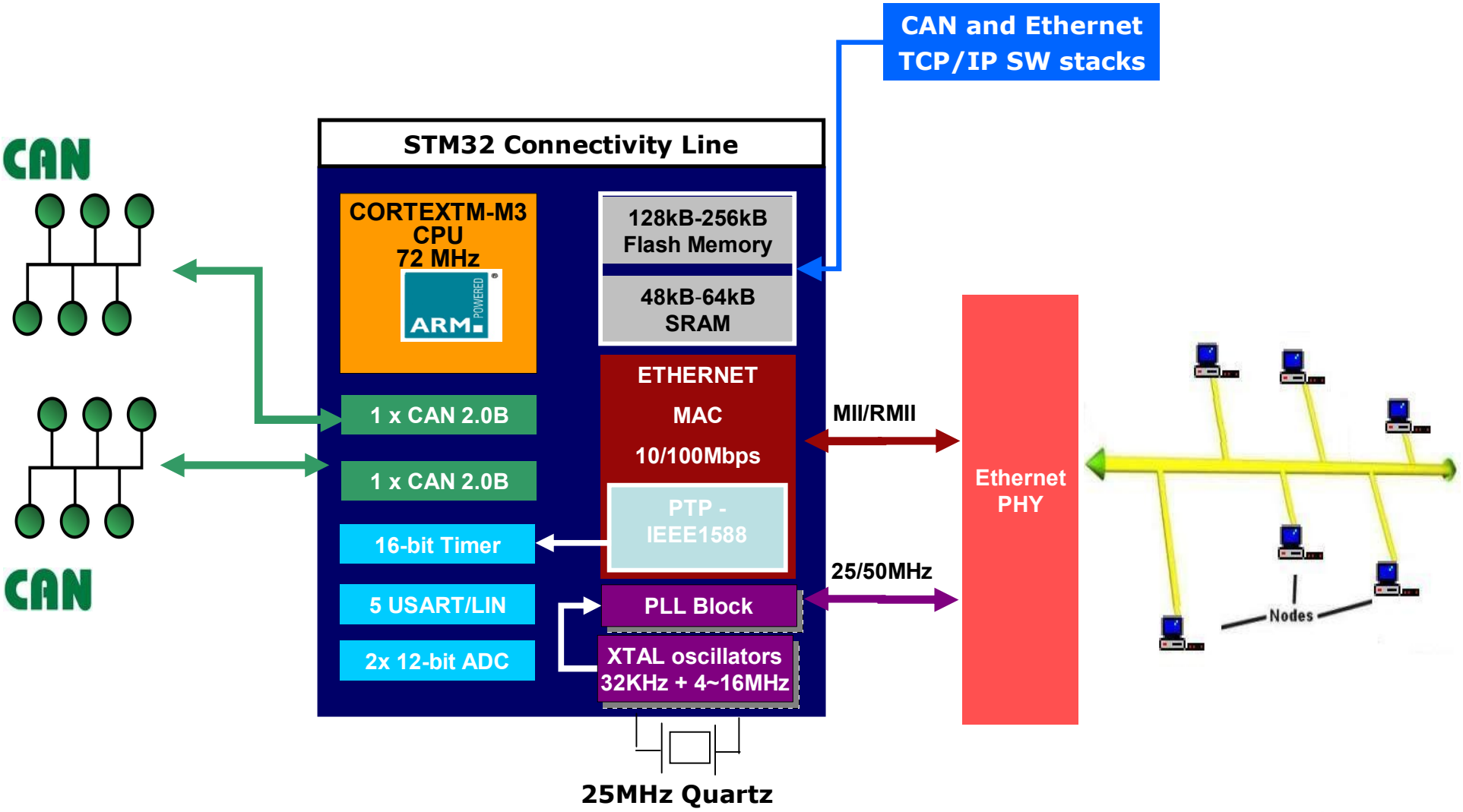
The USB SOF output for audio applications to synchronize the audio rate

STM32 Connectivity Line Audio Applications Implementation example

- 147.46MHz PLL
- 2x Audio Classe I²S interface (16-32bit data)
  - →Master Clock support with better than 0.5% accuracy
  - →Audio sampling frequencies from 8kHz to 96kHz
- USB FS OTG with PHY
- SPI for SD card support

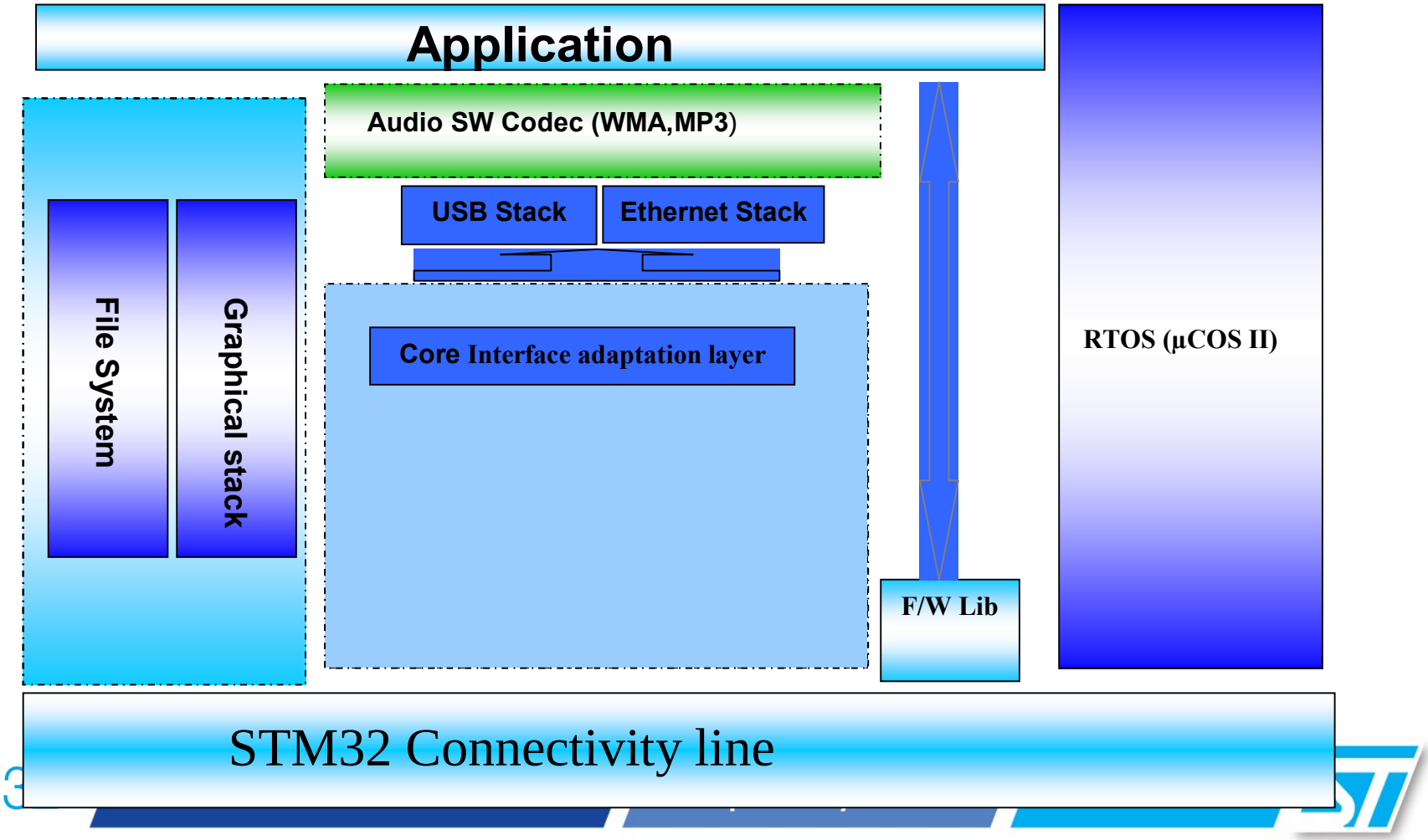


STM32 Connectivity Line Industrial gateway implementation example



Firmware Packages & Applications Architecture

- Standard F/W library
- Micrium: µCOS2 RTOS
- Micrium: USB OTG/host/device stacks
- Micrium: USB OTG/host/device stacks
- SEGGER: Graphical stack & File System
- Interniche: Ethernet TCP/IP stack
- Software MP3 decoder
- Software WMA decoder



Thank You !