SPIRIT1
Technical Details

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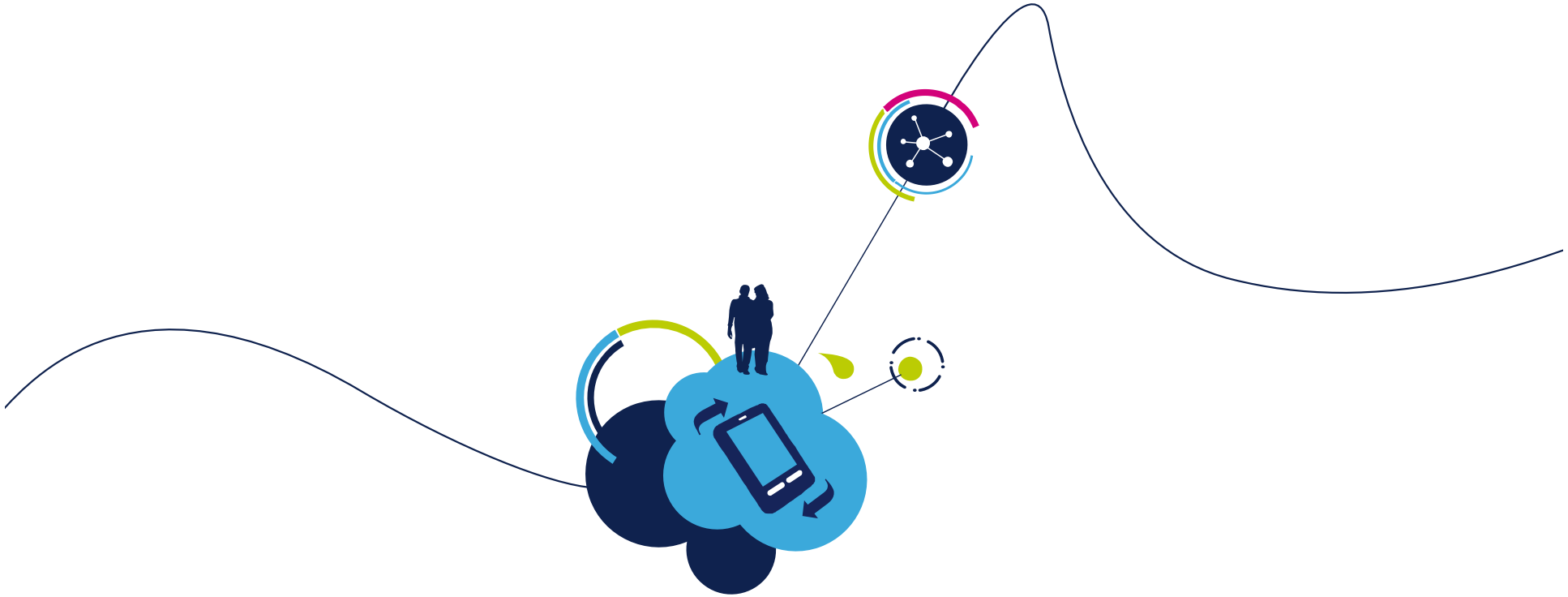

State Machine, MCU Control Interface & AES128

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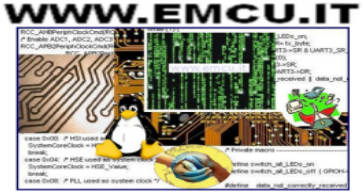
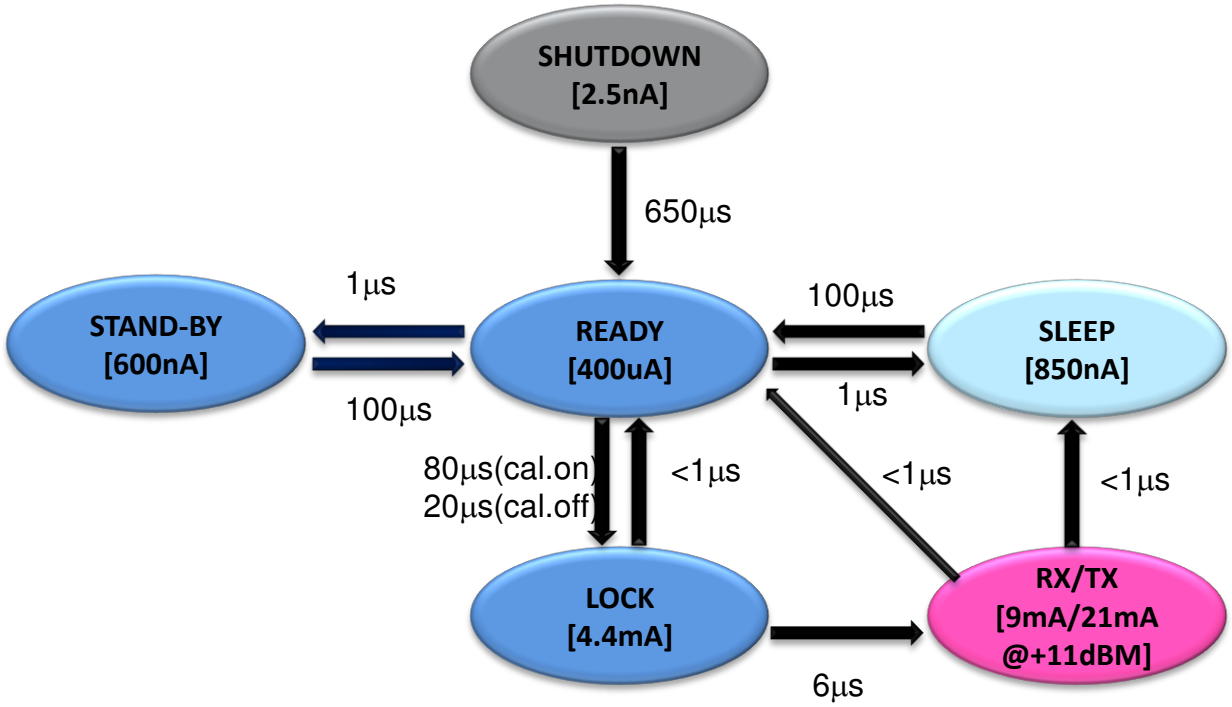
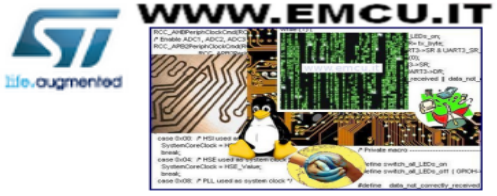


Operating Modes/Consumption



Mode	Description
Shutdown	Off, no register retention
Standby	SPI On, register retention
Sleep	SPI on, register retention, Wakeup timer on
Ready	SPI on, XTAL on
RX	SPI on, XTAL on, RF Synth on
TX	SPI on, XTAL on, RF Synth on

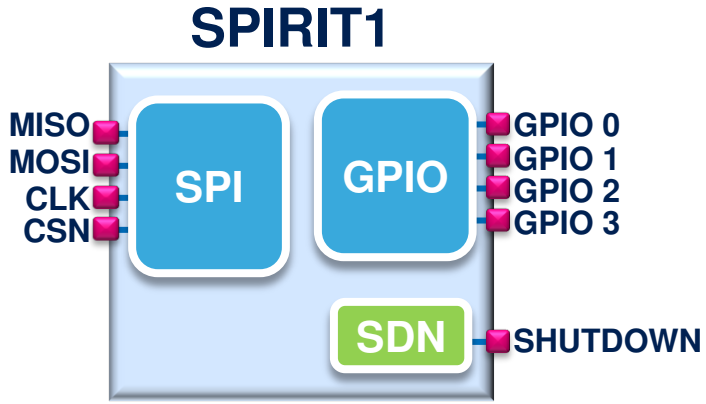
Built-in main controller handles operating mode transitions



MCU interface

SPI communication

- Write registers or FIFOs
- Read registers or FIFOs
- 17 Commands (State diagram, AES, FIFO flush)

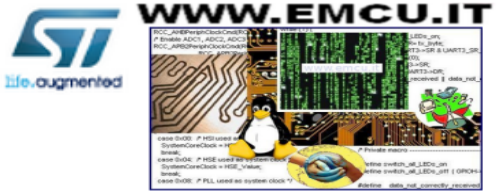


GPIO communication

- Interrupt signals
- Monitoring signals (Valid preamble detected, valid sync word detected, …)
- Commands (TX/RX mode, Wake-up from external input, …)
- Input/output data (direct mode)
- Input/output reference clock (MCU clock out, 34.7 kHz for LDC mode input)
- Analog output: temperature sensor (GPIO 0)

SDN pin

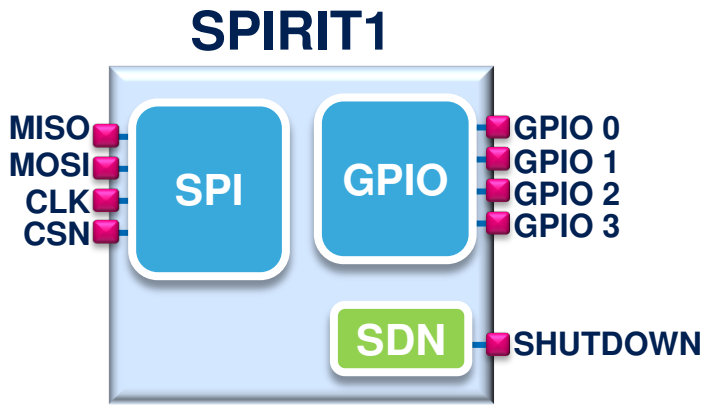
- Shutdown signal



Monitoring signals

GPIO communication

- **Monitoring signals**



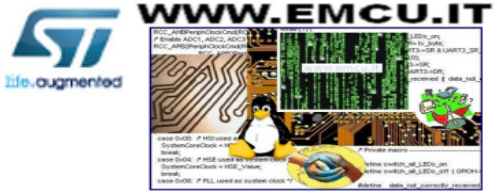
Packet oriented
Valid preamble detected
Sync word detected
RSSI above threshold

FIFOs oriented
TX FIFO almost full
TX FIFO almost empty
RX FIFO almost full
RX FIFO almost empty

Status oriented
Device in READY state
Device in SLEEP or STANDBY states
TX state indication
RX state indication
TX or RX mode indicator
Device in LOCK state

Status oriented
Low battery level
Power-On Reset
Antenna switch used for antenna diversity

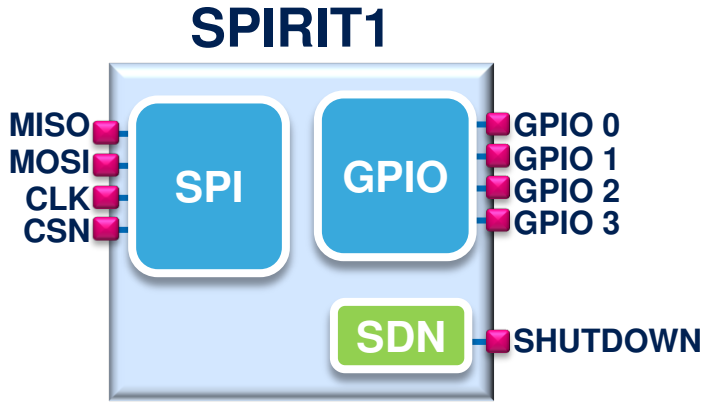
Other
VDD/GND (to emulate an additional GPIO of the MCU)
Wake-Up timeout in LDC mode



Interrupts

GPIO communication

- **Interrupt signals**



Packet oriented
RX data ready
RX data discarded
TX data sent
CRC error
Valid preamble detected
Sync word detected
RSSI above threshold

FIFOs oriented
TX FIFO underflow/overflow error
RX FIFO underflow/overflow error
TX FIFO almost full
TX FIFO almost empty
RX FIFO almost full
RX FIFO almost empty

Protocol oriented
Max re-TX reached
Max number of back-off during CCA
Wake-up timeout in LDC mode
AES End–Of – Operation

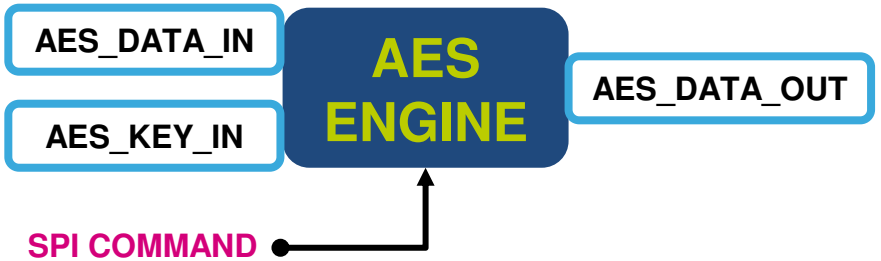
Status oriented
READY state in steady condition
STANDBY state switching in progress
Low battery level
Power-On Reset
RX operation timeout

SPIRIT1 AES-128 Engine

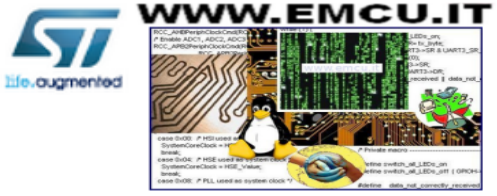
The SPIRIT1 provides data security support as it embeds the Advanced Encryption Standard (AES) 128-bit core.

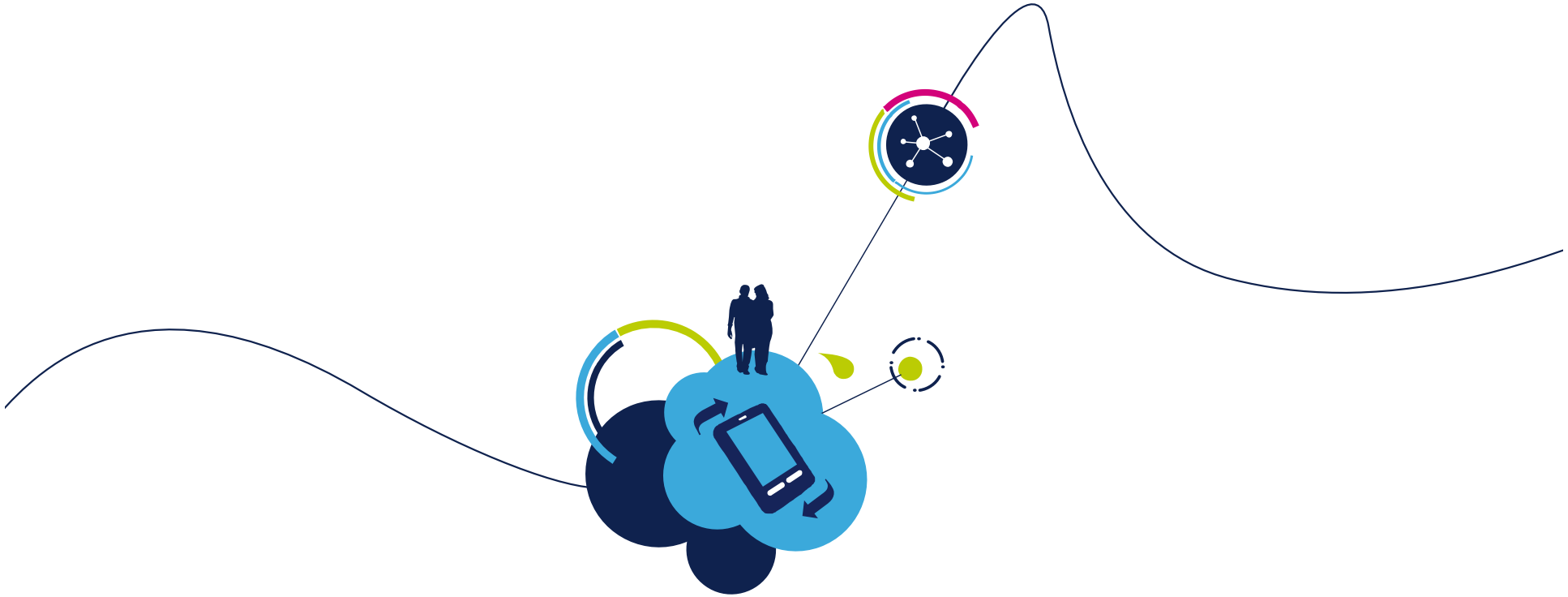
The AES-128 engine can be used at anytime.

- The SPIRIT1 provides 3 banks of 128 bits registers:
  - Input register (*AES_DATA_IN*)
  - Output register (*AES_DATA_OUT*)
  - Key register (*AES_KEY_IN*).



- Four operations are available:
  - Encryption using a given encryption key.
  - Decryption key derivation starting from an encryption key.
  - Data decryption using a decryption key.
  - Data decryption using a encryption key.





Transmission & Reception

RF Related Features

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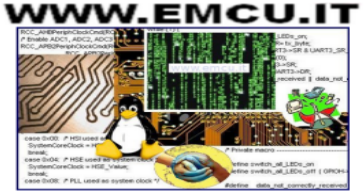
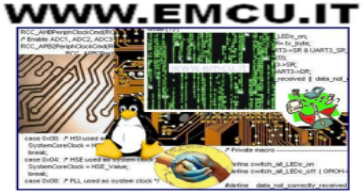


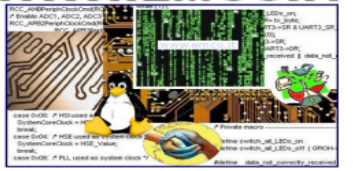
SPIRIT1 Oscillator and RF synthesizer

- **An external XTAL (24, 25, 26, 48, 50, 52 MHz), provide a clock signal to the RF frequency synthesizer.**
  - The digital part of the silicon always requires clock in the range (24-26 MHz), so the clock must be divided when using 48-52 MHz XTAL.
- **RF Frequency Synthesizer**
  - has fractional sigma delta architecture for fast settling and narrow channel spacing
  - contains an integrated PLL capable to synthesize frequencies in the bands (150÷174) MHz, (300÷348) MHz, (387÷470) MHz, (779÷956) MHz, providing the LO signal for the RX chain and the input signal for the PA in the TX chain. No external PLL loop filter is needed.
  - uses a multi-band VCO to cover the whole frequency range
- **The base Carrier frequency is programmed using SYNT0-SYNT3 registers of SPIRIT1 (easiest way is to use SPIRIT1 SW library)**
- **Calibration can be automatic (80 us) or manual (20 us), in the latter case the micro should save/restore the calibration words and take into account for temperature/VBAT variation which could require recalibration.**



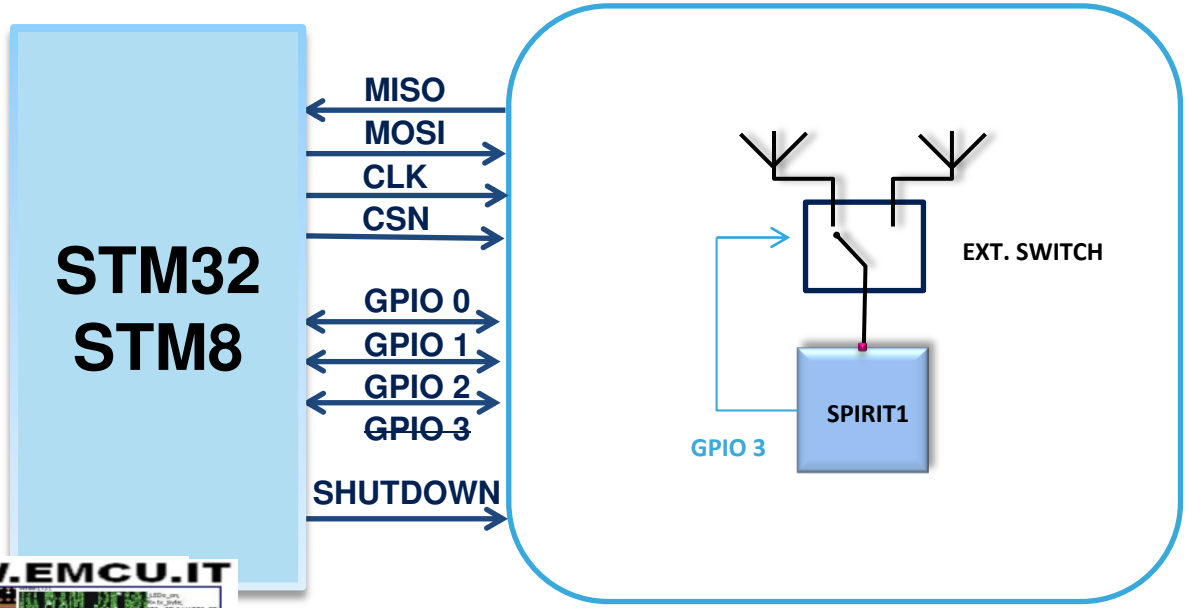
Receiver Quality Indicators

- **Received signal strength indicator (RSSI) – 8 bits**
  - Measured received signal power. RSSI reading is available after the reception of a packet in a register
- **Carrier Sense (CS) – 1 bit**
  - Based on RSSI (threshold, static/dynamic mode)
- **Link quality indicator (LQI) – 4 bits**
  - Level of noise power on the demodulated signal
- **Preamble quality indicator (PQI) – 8 bits**
  - Best correlation between the received preamble and the expected one
  - Preamble valid IRQ can be used
  - Packet demodulation can be stopped when PQI is below threshold
- **Synchronization quality indicator (SQI) – 7 bits**
  - Measurement of the best correlation between the received synchronization word and the expected one
  - Sync word detected IRQ can be used
  - Packet demodulation can be stopped when SQI is below threshold

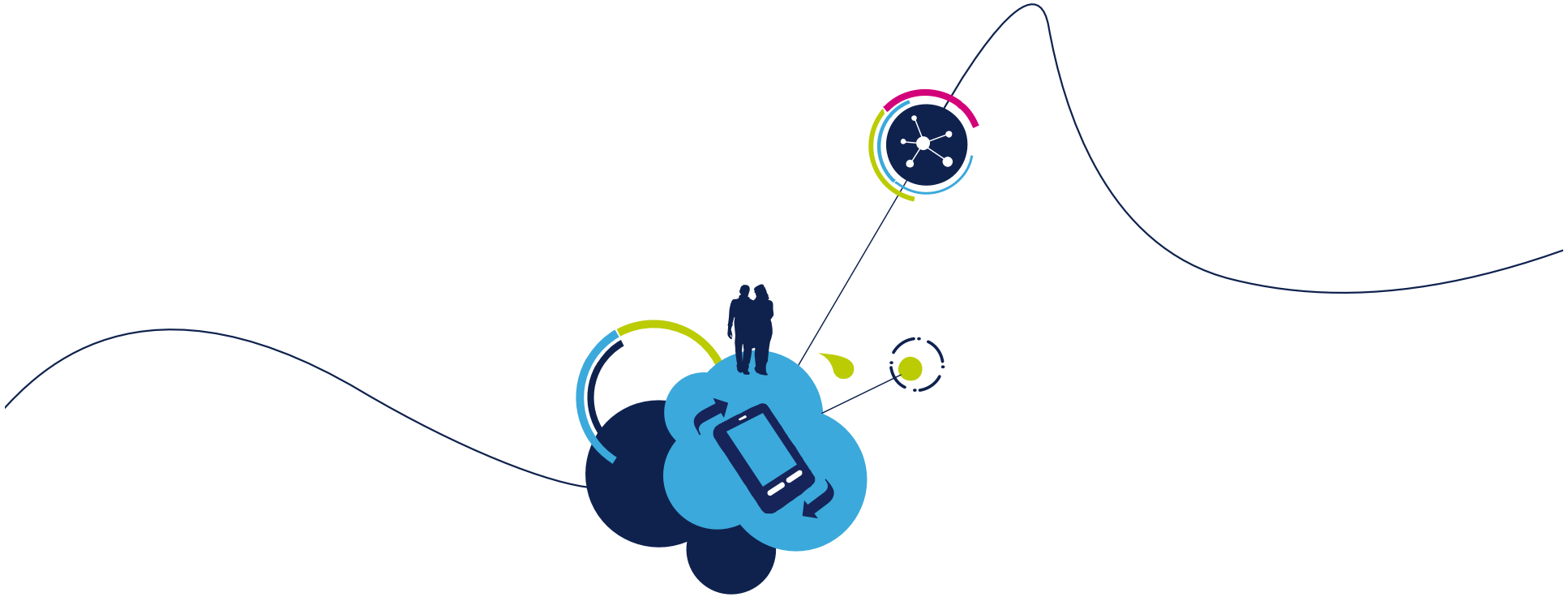


Automatic Antenna diversity algorithm

- An external switch is controlled to select the antenna with the highest RSSI (through programmable SPIRIT1 GPIO)
- While receiving the packet preamble, the antennas are repeatedly switched until the RSSI > threshold .
- The switch is then disabled and the selected antenna is used.



Any GPIO of SPIRIT1 can be programmed to control the ext. switch



Transmission & Reception

Packet handler Engine

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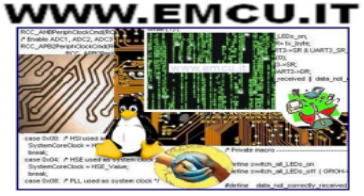


SPIRIT1 Packet Handler Engine

Embedded packet formats

- **STack**

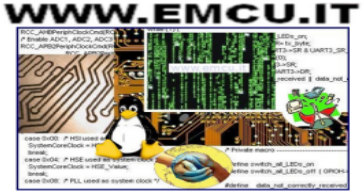
Preamble 1 – 32 Bytes	Sync 1 – 4 Bytes	Length 0 – 16 Bits	Destination Address 1 Byte	Source Address 1 Byte	Control 0 – 4 Bytes	Seq. No. 2 bits	No ACK 1 bit	Payload	CRC 0, 8, 16, 24 bits

- **WM-Bus**

Preamble	Sync	Payload	Postamble

- **BASIC**

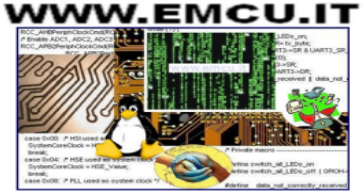
Preamble	Sync	Length	Destination Address	Control	Payload	CRC



SPIRIT1 Direct mode

The purpose of the direct modes is to by-pass completely the packet handler engine and to give the user more flexibility. The direct modes are available both for RX and TX

- **Direct mode through FIFO (SPI)**
  - In the direct mode through FIFO the data are continuously read from the TX FIFO and transmitted without any processing of the packet handler for the transmitter and the data are continuously received in the RX FIFO without any processing.
- **Direct mode through GPIO**
  - In the direct mode through GPIO the data are sampled by the device on the rising edge of the clock signal and send on air without any processing of the packet handler for the transmitter and the data are continuously written to one GPIO together with the clock in another GPIO.
- **PN9 mode (for TX)**
  - A pseudo-random binary sequence is generated internally for test purpose only.



SPIRIT1 Automatic Packet Filtering

Embedded automatic packet filtering

- **CRC** (Packet discarded if CRC check do not pass)
- **Destination address** (My own address, Broadcast, Multicast)
- **Source address** (reference address in AND bitwise with the source mask)
- **Control field** (reference address in AND bitwise with the control mask)

The automatic packet filtering engine works in STack and BASIC packet formats

More than one automatic filtering feature can be enabled at the same time

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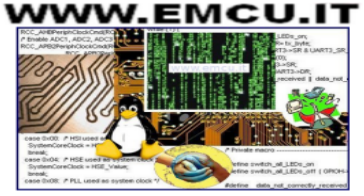
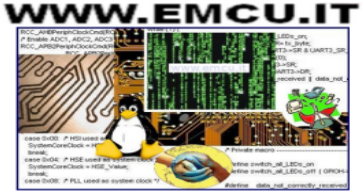


SPIRIT1 Link Layer Protocol

Available through the STack packet format, with following features

- **Automatic acknowledgment**
  - The receiver sends an ACK packet, if a packet is received with success and bit NO_ACK = 0. The transmitter goes in RX state to wait the ACK packet. If the transmitter does not receive any ACK packet when it should, the packet transmitted before is considered lost.
- **Automatic acknowledgment with piggybacking**
  - The receiver can fill the ACK packet with data (as payload field of the packet). The data to send is stored in the TX FIFO (up to 96 bytes without any additional interaction from the MCU !!!)
- **Automatic retransmission**
  - If the transmitter does not receive the ACK packet within the RX timeout programmed, it can be configured to do another transmission. Up to 15 retransmissions.

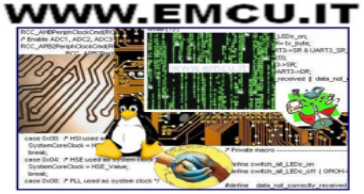


SPIRIT1 Data coding and integrity check

Error correction and detection methods

- **FEC/Viterbi and interleaving**
  - Convolutional coding in transmitter and on the receiver side - error correction is performed using soft Viterbi decoding
  - Controls errors in data transmission over unreliable/noisy communication channels. The number of transmitted bits is roughly doubled, hence the on-air packet duration in time is roughly doubled as well (~1dB link budget increase)
- **Data whitening/ dewhitening**
  - To prevent short repeating sequences that create spectral lines, which may complicate symbol tracking at the receiver or interferer with other transmissions
- **CRC (Cyclic Redundancy Check)**
  - CRC polynomials can be selected (4 options). Programmable to 8, 16, or 24 bits

CRC and whitening is applied over all fields excl. preamble and synchronization word

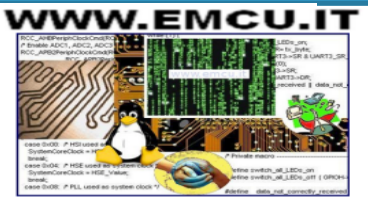


Power consumption Efficient use of the **RX timeout mechanism [1/3]**

In order to reduce power consumption, many automatic RX timeout modes are supported

- **Infinite timeout** – RX stops when the packet ends or when the SABORT SPI command comes from the microcontroller
- **Carrier sense (CS) timeout** - RX is aborted if the RSSI never exceeds a programmed threshold within preset timeout (TIMER)
- **SQI timeout** - RX is aborted if the synchronization quality indicator (SQI) does not exceed a programmed threshold within preset timeout
- **PQI timeout** - RX is aborted if the preamble quality indicator (PQI) does not exceed the programmed threshold within preset timeout

The value of the Time out can be programmed up to ~3 seconds

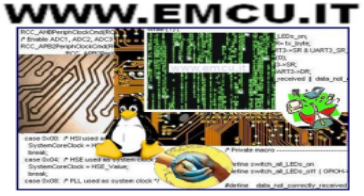


Power consumption Efficient use of the **RX timeout mechanism [2/3]**

- CS, SQI and PQI can be combined together, both '**AND**' or '**OR**' Boolean relationships among them are allowed to avoid the reception to be interrupted

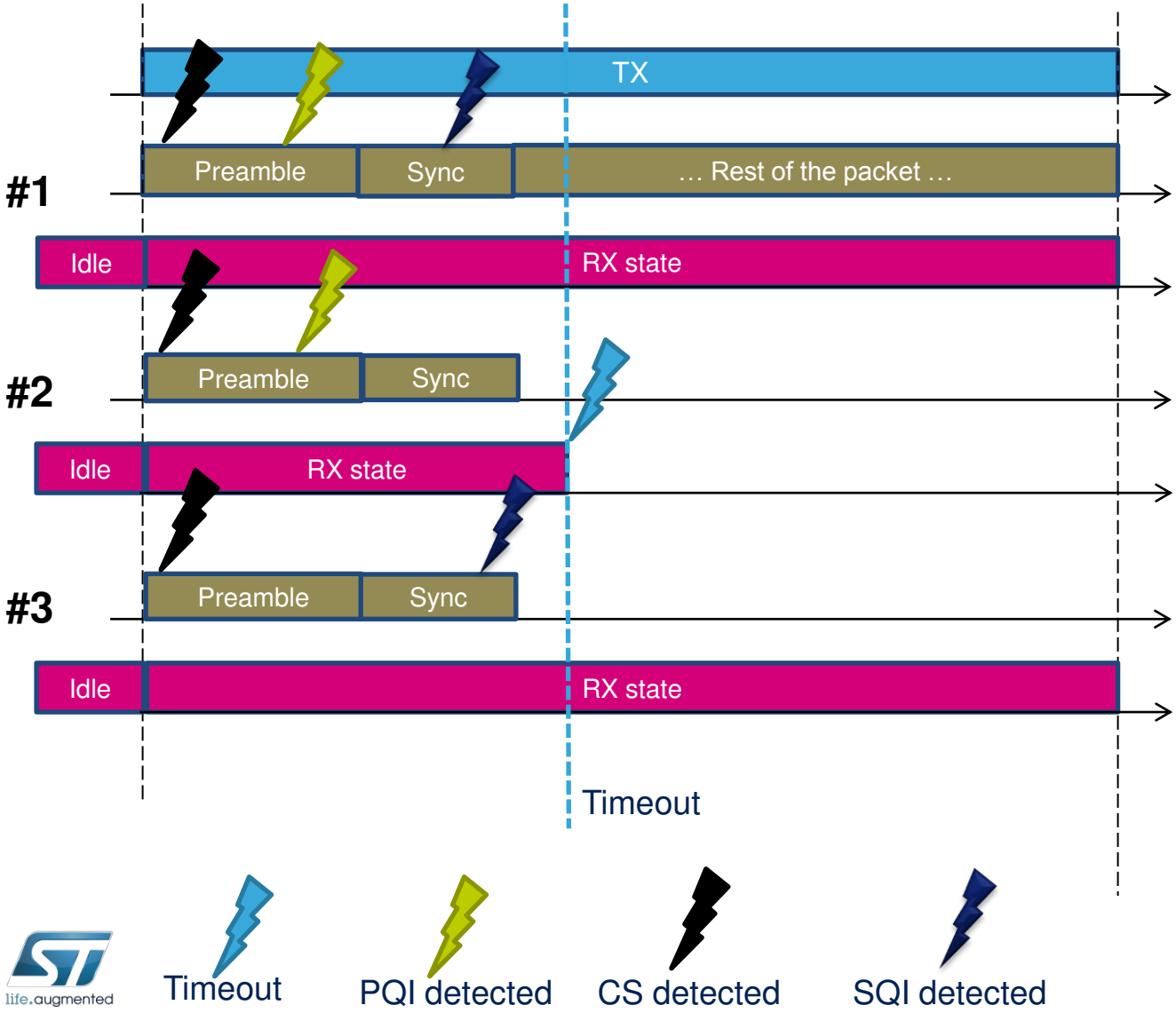
- It is up to the programmer to effectively set the timeout value (time) according to the application needs (i.e. preamble and sync word length, data rate etc.)

AND / OR SELECT	CS	SQI	PQI	Description
0	0	0	0	Time out not stopped
1	0	0	0	Timeout always stopped (default)
x	1	0	0	CS (RSSI above threshold)
x	0	1	0	SQI above threshold
x	0	0	1	PQI above threshold
0 (AND)	1	1	0	Both RSSI AND SQI above threshold
0 (AND)	1	0	1	Both RSSI AND PQI above threshold
0 (AND)	0	1	1	Both SQI AND PQI above threshold
0 (AND)	1	1	1	ALL above threshold
1 (OR)	1	1	0	RSSI OR SQI above threshold
1(OR)	1	0	1	RSSI OR PQI above threshold
1(OR)	0	1	1	SQI OR PQI above threshold
1(OR)	1	1	1	ANY above threshold



Power consumption Efficient use of the **RX timeout mechanism [3/3]**

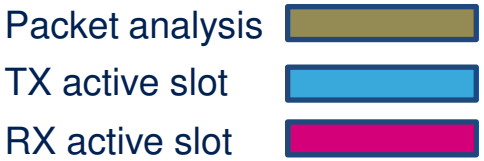
3 examples



1# CS, PQI, SQI being tested in the app. All above threshold, timeout stopped. Packet received.

#2 CS, PQI, SQI being tested in the app. SQI below threshold, timeout was not stopped. Packet not received - demodulation stopped .

#3 CS, SQI above threshold, timeout was stopped. PQI test was not set in the app. Packet received.



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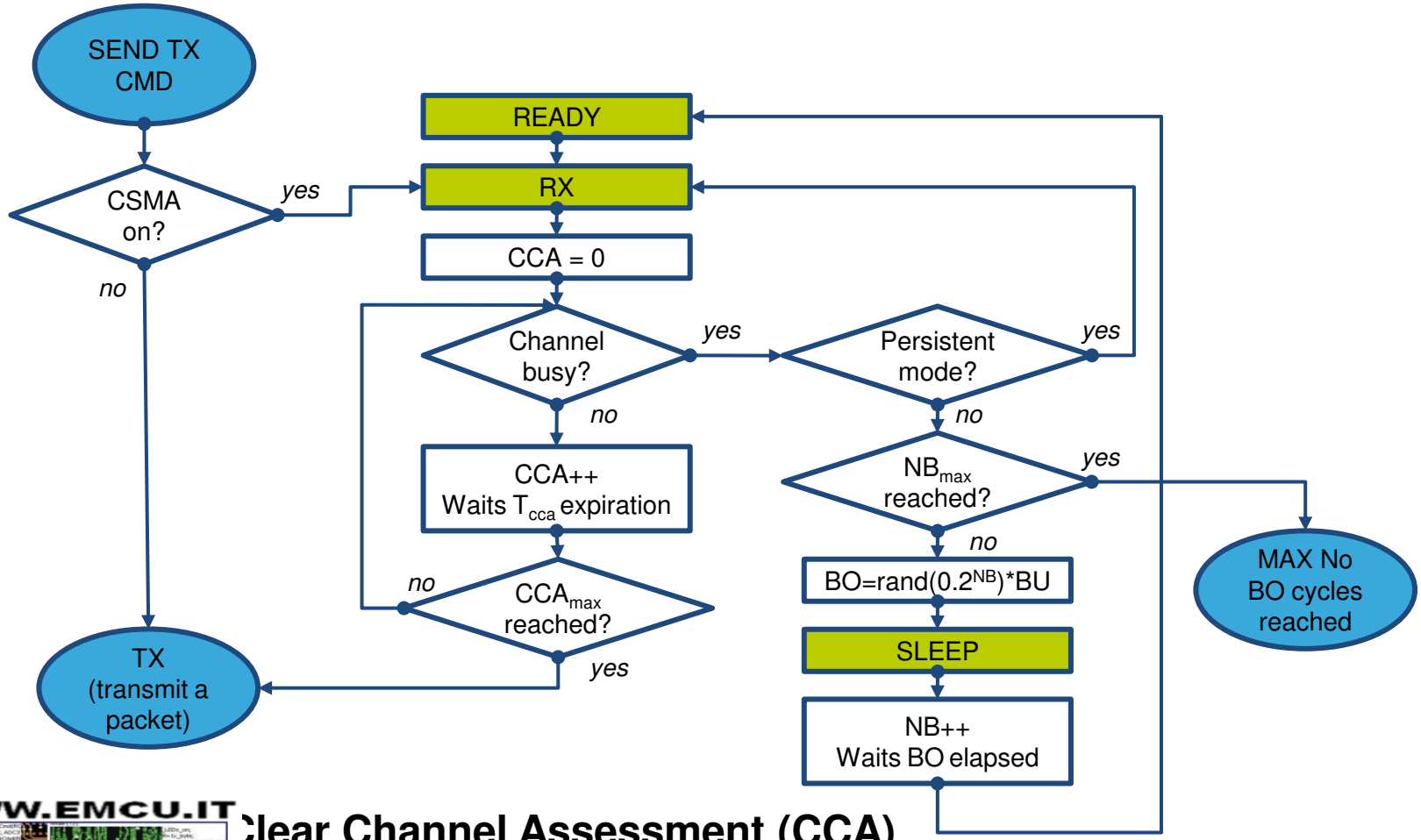
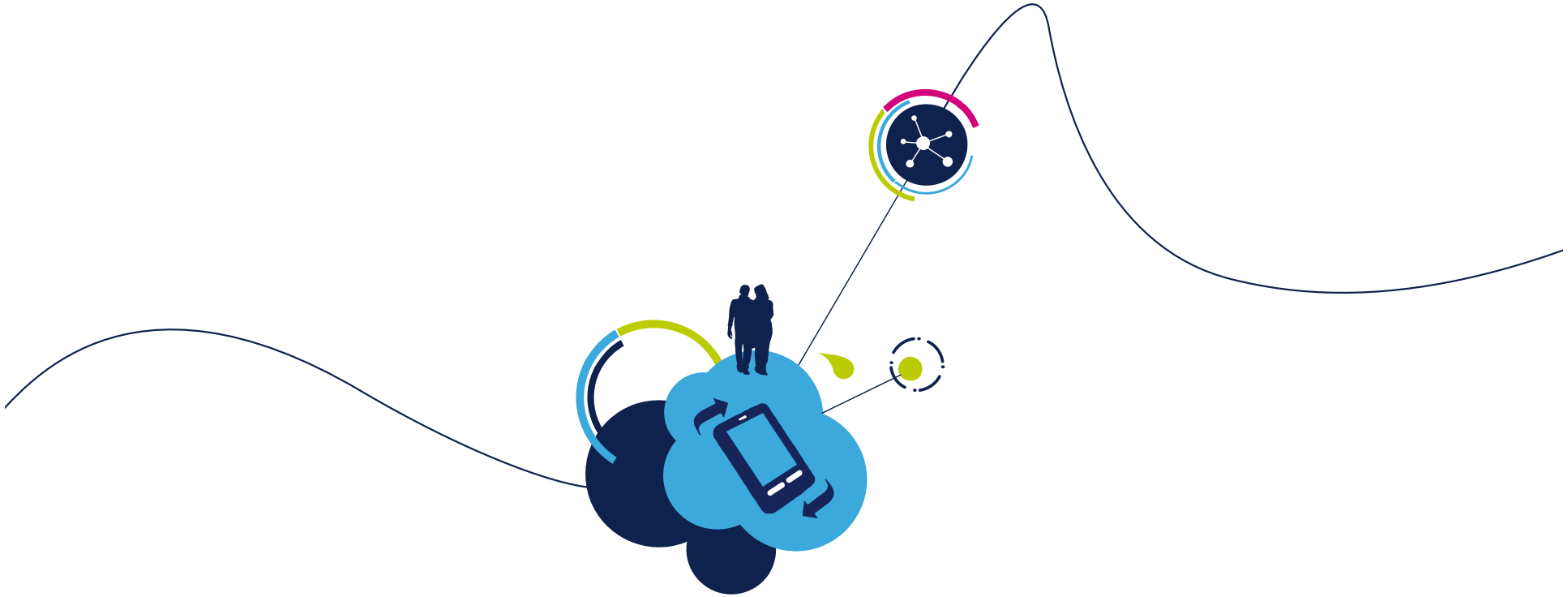
SPIRIT1 CSMA/CA Engine

The CSMA/CA engine is a channel access mechanism based on the LBT rule "listen before talk". This avoids the simultaneous use of the channel by different transmitters



Clear Channel Assessment (CCA)



SPIRIT1 @ 868MHz with external PA for +27dBm Output Power

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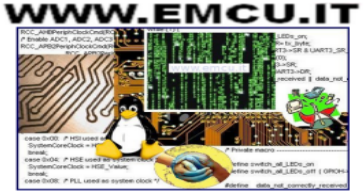
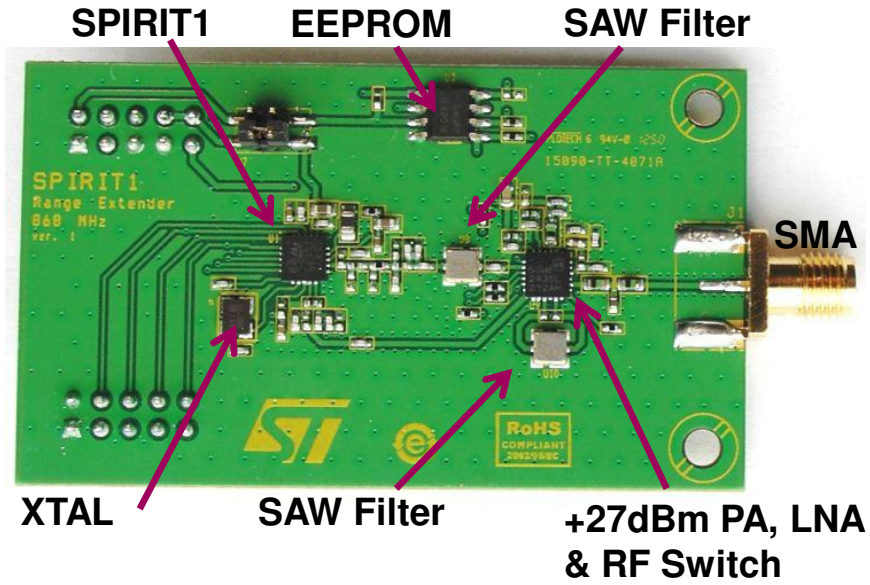


STEVAL-IKR001V8D

SPIRIT1 @868MHz with +27dBm output

- **STEVAL-IKR001V8D demo kit RF board content**
  - SPIRIT1 RF transceiver
  - Tai-Saw Technology – TA801A 868 MHz SAW filter
  - FEM (PA + LNA + RF Switch) - Skyworks SE2435L
  - EEPROM – M95640



PA = Power Amplifier
LNA = Low Noise Amplifier
SAW = Surface Acoustic Wave (selective filter)
FEM = Front End Module